

853S01

Input Interface Termination with AC Coupling Examples

Abstract

This document provides examples of input interface termination with AC coupling. The 853S01 clock input is used for demonstration purposes in this document. These examples can also be used in the receiver with input specification. The driver can be LVPECL, CML, LVDS, HCSL, or other driver that provides a different switching clock signal.

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1. Driver Examples

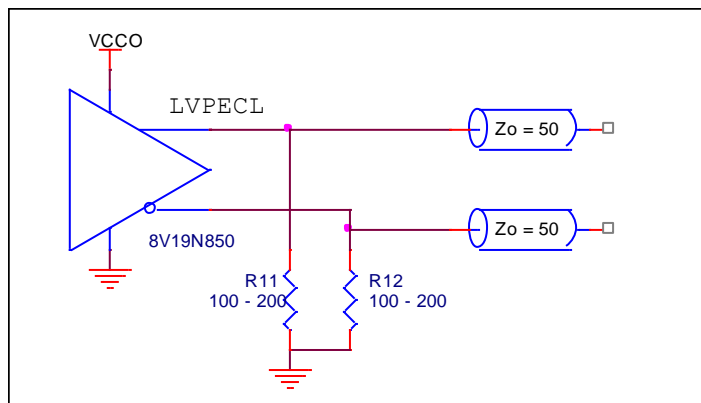


Figure 1. LVPECL Driver Example

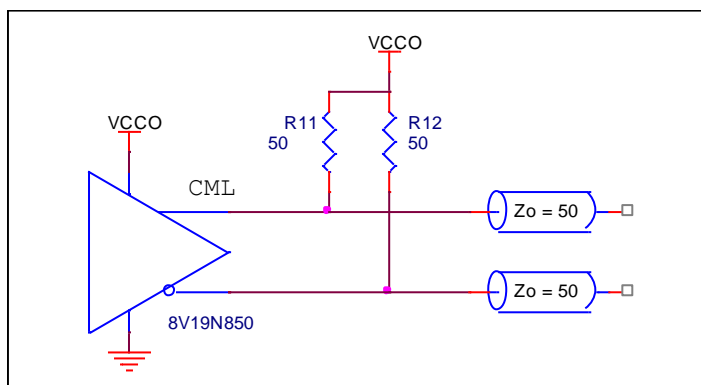


Figure 2. CML Driver Example

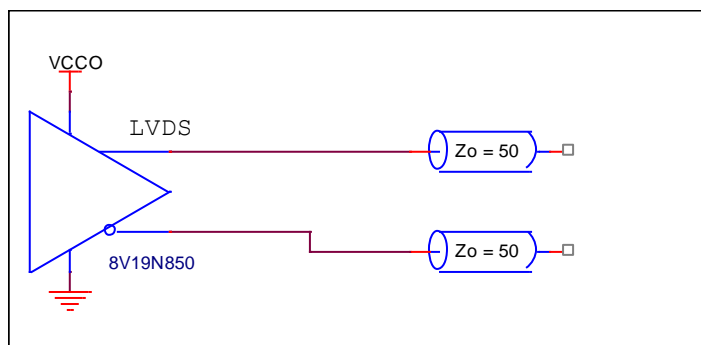


Figure 3. LVDS Driver Example

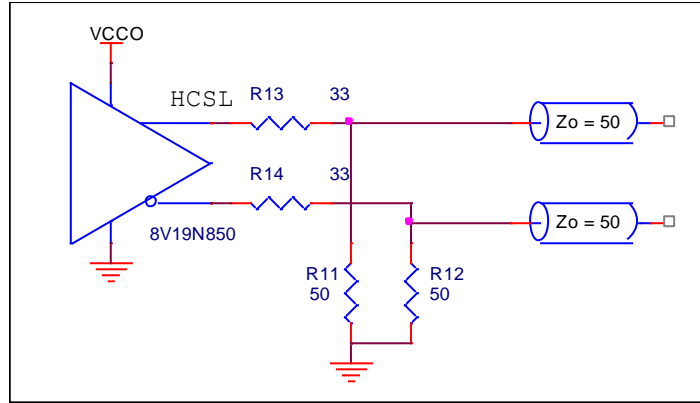


Figure 4. HCSL Driver Example

2. 853S01 Input Requirement

Table 4D. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$; $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, PCLK1, nPCLK0, nPCLK1 $V_{CC} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	PCLK0, PCLK1 $V_{CC} = 3.465V, V_{IN} = 0V$	-10			μA
		nPCLK0, nPCLK1 $V_{CC} = 3.465V, V_{IN} = 0V$	-150			μA
V_{PP}	Peak-to-Peak Voltage; NOTE 1		150		1200	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		1.2		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3		$V_{CC} - 1.125$		$V_{CC} - 0.875$	V
V_{OL}	Output Low Voltage; NOTE 3		$V_{CC} - 1.895$		$V_{CC} - 1.62$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.495		0.975	V
V_{BB}	Bias Voltage		1.695		2.145	V

NOTE 1: V_{IL} should not be less than $V_{EE} - 0.3V$.

NOTE 2: Common mode input voltage is defined as V_{IH} .

NOTE 3: Outputs terminated with 50Ω to $V_{CC} - 2V$.

Table 4E. LVPECL DC Characteristics, $V_{CC} = 2.5V \pm 5\%$; $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, PCLK1, nPCLK0, nPCLK1 $V_{CC} = V_{IN} = 2.625V$			150	μA
I_{IL}	Input Low Current	PCLK0, PCLK1 $V_{CC} = 2.625V, V_{IN} = 0V$	-10			μA
		nPCLK0, nPCLK1 $V_{CC} = 2.625V, V_{IN} = 0V$	-150			μA
V_{PP}	Peak-to-Peak Voltage; NOTE 1		150		1200	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		1.2		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3		$V_{CC} - 1.125$		$V_{CC} - 0.875$	V
V_{OL}	Output Low Voltage; NOTE 3		$V_{CC} - 1.895$		$V_{CC} - 1.62$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.495		0.975	V
V_{BB}	Bias Voltage		0.935		1.305	V

NOTE 1: V_{IL} should not be less than $V_{EE} - 0.3V$.
 NOTE 2: Common mode input voltage is defined as V_{IH} .
 NOTE 3: Outputs terminated with 50Ω to $V_{CC} - 2V$.

3. Input Interface with AC Coupling

3.1 Example 1

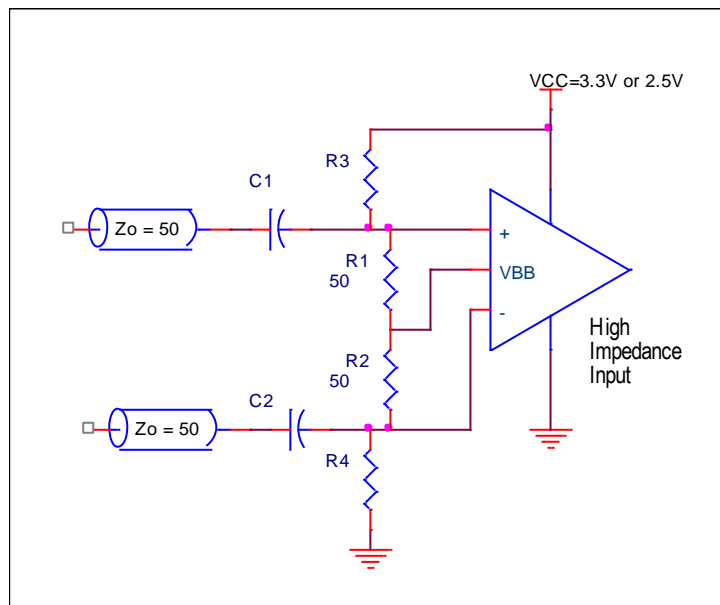


Figure 5. Example 1 – 853S01 Input Interface

R3 and R4 is optional. Suggest spare footprint for Self-oscillation Prevention.

	VCC = 2.5V	VCC = 3.3V
R3 (Ohm)	2.2k	2.2k
R4 (Ohm)	2.2k	3.6k

3.2 Example 2

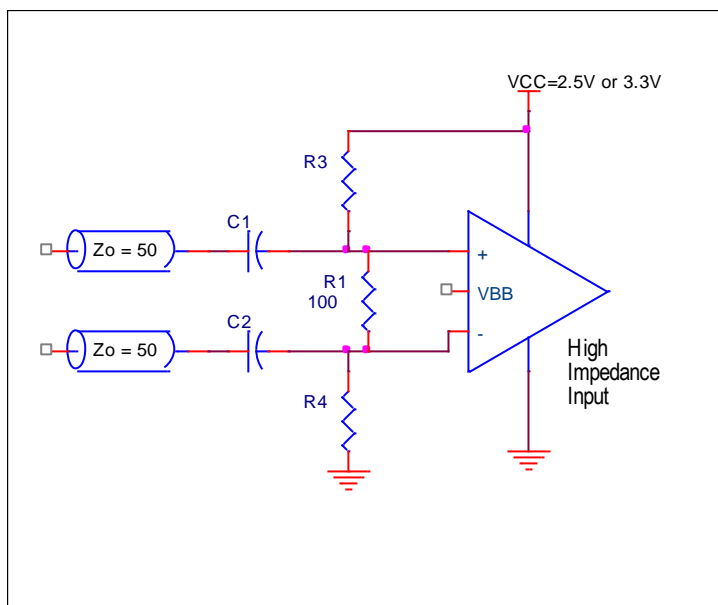


Figure 6. Example 2 – 853S01 Input Interface

R3 and R4 is optional. Suggest spare footprint for Self-oscillation Prevention.

	VCC = 2.5V	VCC = 3.3V
R3 (Ohm)	2.2k	2.2k
R4 (Ohm)	2.2k	3.6k

3.3 Example 3

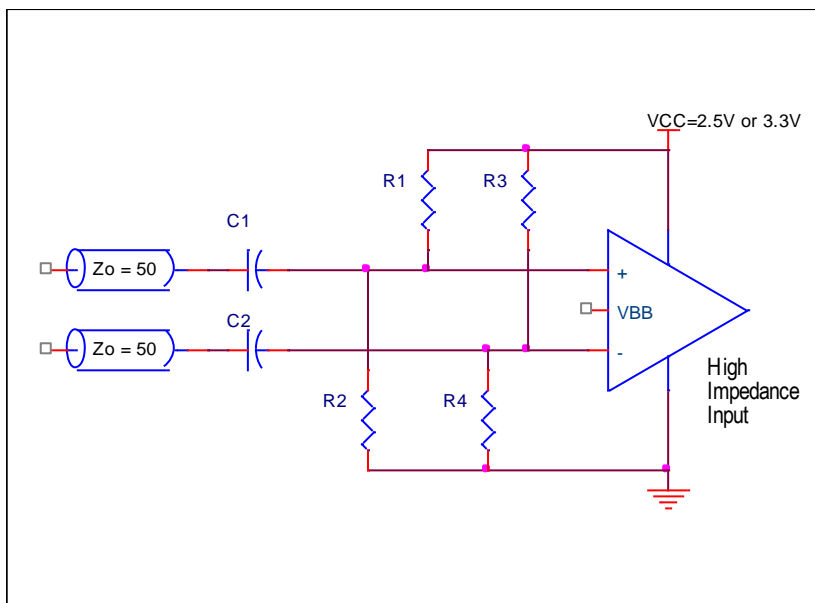


Figure 7. Example 3 – 853S01 Input Interface

	VCC = 2.5V	VCC = 3.3V
R1 (Ohm)	100	133
R3 (Ohm)	100	133
R2 (Ohm)	100	82.5
R4 (Ohm)	100	82.5

4. Revision History

Revision	Date	Description
1.0	Oct.28.20	Initial release.

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