Introduction

This application note addresses the possible self oscillation of the differential input due to external termination in certain board level design. Examples of solutions to prevent this type of oscillation are provided. The IDT Netcom product differential clock input is designed to receive signals from high speed differential clock drivers for examples LVDS, LVPECL, LVHSTL, SSTL, and HCSL drivers. To prevent input oscillation when the input pins are floating, the true clock input CLK has a built-in ~51KΩ pull-up resistor and the complement clock input nCLK has a built-in 51KΩ pull-down (or both pull-up and pull-down resistor). Therefore, the CLK pin is held at logic low and the nCLK pin is held at logic high. Using these high impedance internal pull-down/pull-up resistors does not affect the external termination values required by the various driver types.

In general, high speed differential clock drivers require matched load termination near the differential input. The termination generates equal DC potential at the differential input when the clock signal is absent due to tri-stated outputs or floating inputs. This equal potential can cause oscillation at high frequencies which will be prevented by placing a small DC offset input voltage between CLK and nCLK. Several termination examples of self oscillation prevention for various types of termination are provided.

LVDS Interface

A general LVDS interface is shown in Figure 1. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across the CLK/nCLK pair. In this case, the LVDS output forces CLK to a logic high and the complementary LVDS output forces nCLK to a logic low, or vice versa. The load termination typically provides sufficient voltage difference to prevent oscillation.

If the CLK/nCLK inputs are driven by a tri-stated output, the 100Ω is negligible compared to the 51KΩ pull-up and pull-down resistors. The voltage drop across R1 is very close to 0V. Therefore, high frequency oscillation at the input circuitry can occur when the driver is tri-stated. This oscillation can be prevented by introduce the DC offset between the CLK and nCLK inputs without affecting the matched load. Figure 2 shows how to add the external pull-up resistor R2 and the external pull-down resistor R3 to increase the DC voltage between CLK and nCLK. Effectively, this prevents oscillation. However, setting this swing too wide will increase the offset between the CLK and nCLK signals during normal operation when the clock signal is present. General equations to determine the R1, R2 and R3 values are provided below. The board designer should consider these trade-offs when choosing the voltage across R1.

R1, R2 and R3 can be determined by using the following equations:

$$R2 = R3 = Zo\_diff * VDD / (2 * VR1) \qquad (1)$$
$$R1 = VR1 * (2 * R2) / (VDD - VR1) \qquad (2)$$

where,

Zo_diff is the differential characteristic impedance of the transmission line.

VR1 is the DC voltage drop across R1.

For example, if the DC voltage across R1 is 100mV and the differential characteristic of the transmission line is 100Ω, then the following values for R1, R2, and R3 are chosen.

Zo_diff = 100Ω, VR1 = 50mV, VDD = 3.3V

From equation (1), R2 = R3 = 100Ω * 3.3V / (2 * 50mV) = 3.3KΩ.

Substitute R2 to equation (2), R1 = 50mV * (2 * 3.3KΩ) / (3.3V - 50mV) = 101.5Ω.

Figure 1. General LVDS to Differential Input Interface

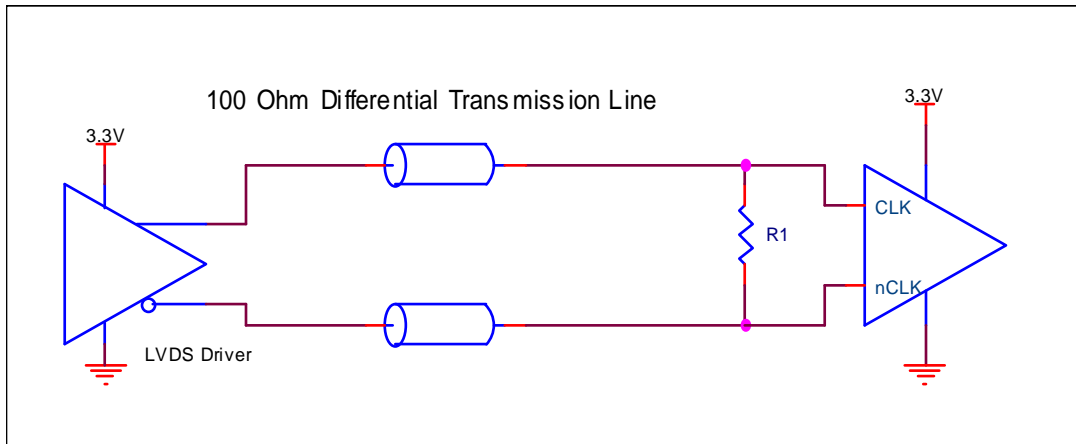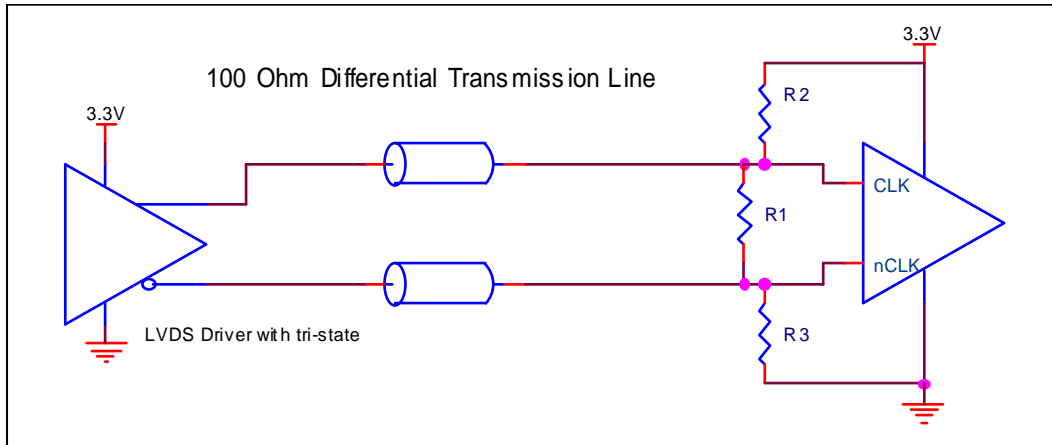100 Ohm Differential Transmission Line

3.3V

3.3V

CLK

R1

nCLK

LVDS Driver

Figure 2. LVDS Driver with Tri-state to Differential Input Interface. Add small DC offset between CLK and nCLK to prevent oscillation.

3.3V

100 Ohm Differential Transmission Line

R2

3.3V

CLK

R1

nCLK

R3

LVDS Driver with tri-state

LVPECL Interface

A general 3.3V LVPECL driver to differential input interface is shown in Figure 3. In a 50Ω single ended or 100Ω differential transmission line environment, LVPECL drivers require a matched load termination of 50Ω to VCC-2V = 1.3V for each output. In this case, the LVPECL driver output forces CLK to logic high and the complementary LVPECL output forces nCLK to logic low or vice versa. The CLK and nCLK typically have sufficient potential difference to prevent oscillation.

For the CLK/nCLK inputs driven by a tri-state output, the bias resistor will generate the same potential of 1.3V at both CLK and nCLK pins. The voltage between CLK and nCLK is very close to 0V. As a result, high frequency oscillation at the input circuitry can occur when the driver is tri-stated. This oscillation will be prevented by placing a minimum peak-to-peak input voltage between the CLK and nCLK inputs which does not affect the matched load. Figure 4 shows the method for changing the bias resistor values at the CLK input. General equations to determine the R3 and R1 values are provided below. Effectively, this prevents oscillation. However, setting this swing too wide will increase the offset between the CLK and nCLK signals. The board designer should consider these trade-offs when choosing the voltage between CLK and nCLK.

R1 and R3 can be determined by using the following equations:

R3 = Zo * VDD / (VDD - 2 - Voffset)   (3)
R1 = R3 * Zo / (R3 - Zo)   (4)

where,

Zo is characteristic impedance of the transmission line.

Voffset is the DC voltage between CLK and nCLK.

For example, if the DC voltage between CLK and nCLK is set to 100mV and the characteristic impedance of the transmission line is 50Ω, then the values for R3 and R1 are as follows:

R3 = 50Ω * 3.3V / (3.3V - 2V - 100mV) = 137Ω

R1 = 50Ω * 137Ω / (137Ω - 50Ω) = 78Ω

Figure 5 shows general termination for an LVPECL driver with AC coupling. When the clock signal is absent, the bias resistors R1, R2, R3 and R4 will create an equal DC potential for the CLK and nCLK input pair. To prevent oscillation, the small offset described above can be introduced by using equations (3) and (4). An example is shown in Figure 6.

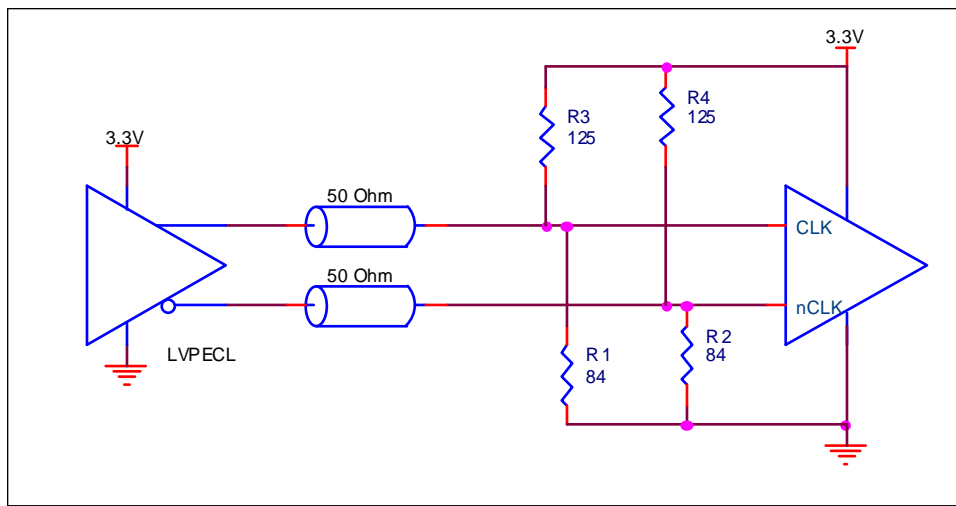**Figure 3.   General LVPECL to Differential Input Interface**

Figure 4.   LVPECL Driver with Tri-state to Differential Input Interface. Add a small offset between CLK and nCLK to prevent oscillation.
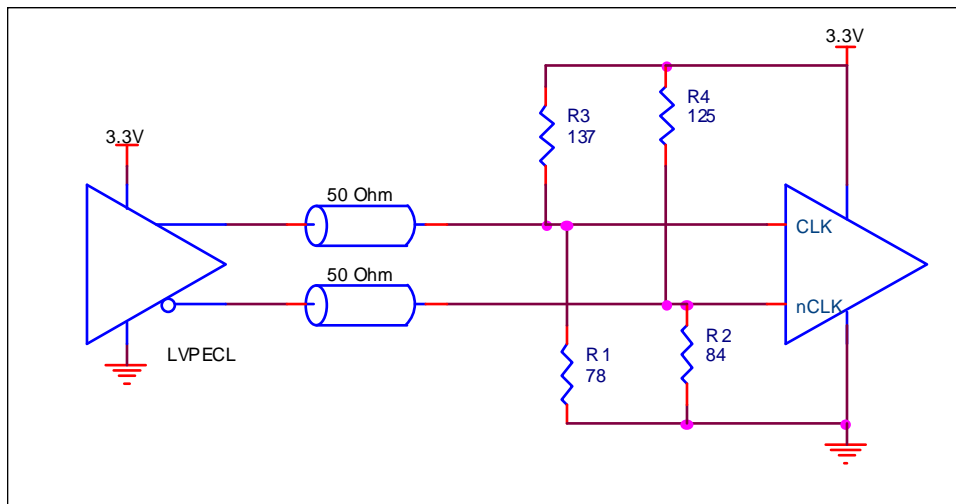
Figure 5.   General LVPECL Driver with AC couple to Differential Input Interface
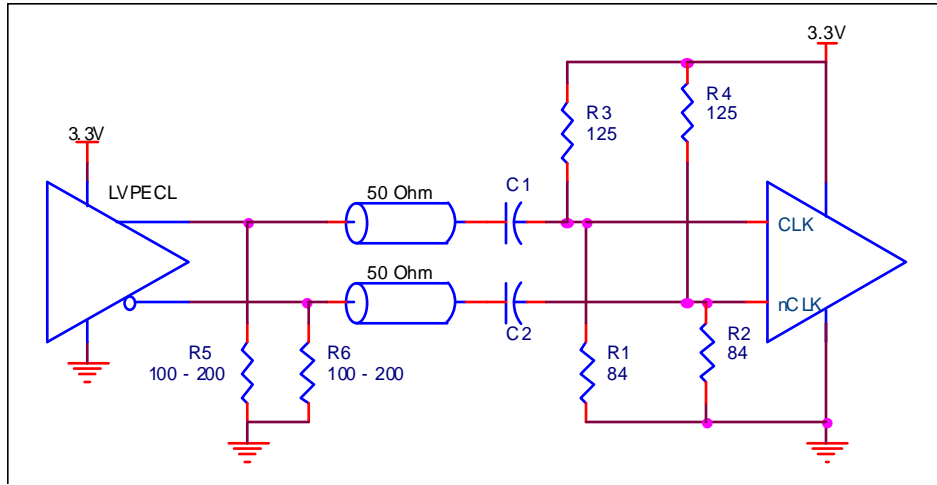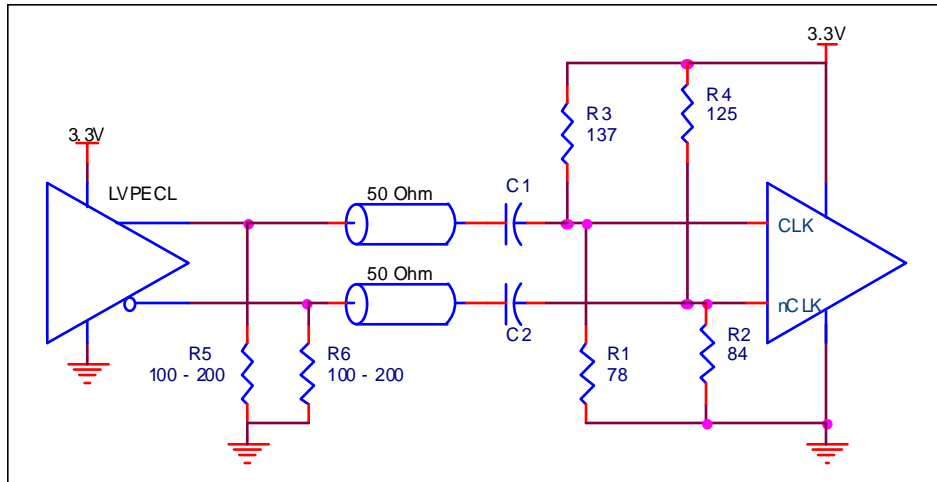

Figure 6.   LVPECL Driver AC couple to Differential Input Interface with a small offset at the CLK and nCLK to prevent oscillation.

LVHSTL Interface

Figure 7 and Figure 8 show general and AC coupled terminations for an open source LVHSTL interface. Typically, open source LVHSTL drivers do not have tri-state capability. The driver will force one side high and the other side low during reset. If the clock signal is absent for the interface with AC coupling (as shown in Figure 8), oscillation may occur. A small offset between the CLK and nCLK pair can be introduced using equations (3) and (4). An example of this interface is shown in Figure 9.

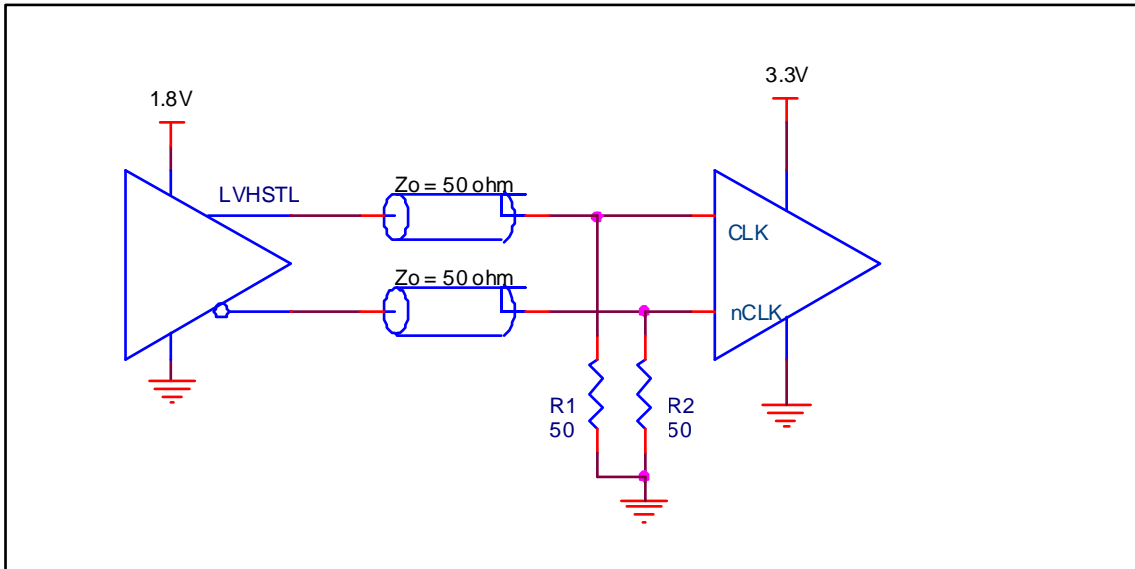**Figure 7. General LVHSTL to Differential Input Interface**

Figure 8. General LVHSTL Driver to Differential Input Interface with AC Coupling
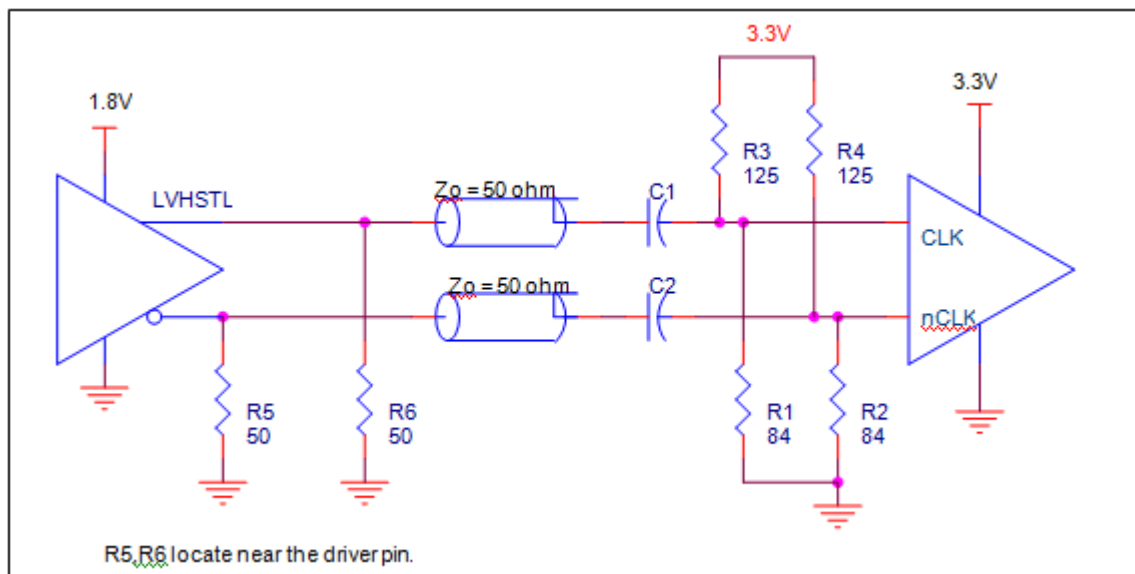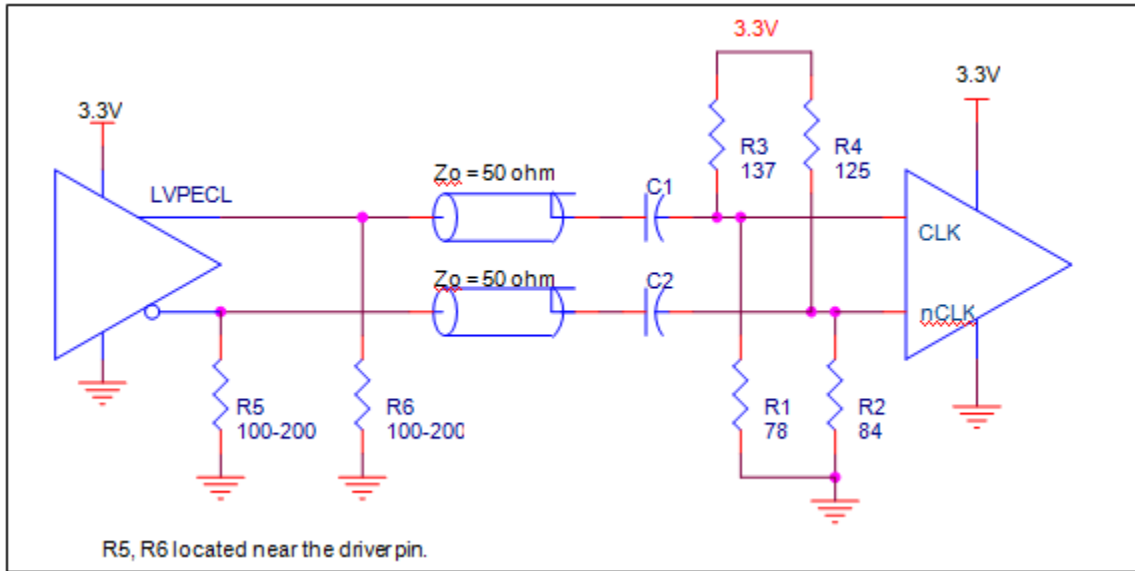
Figure 9. LVHSTL Driver AC coupled to Differential Input Interface with a small DC offset between the CLK and nCLK to prevent oscillation.

Conclusion

The application note shows how the introduction of a small DC offset voltage between CLK and nCLK was used to prevent oscillation when the input clock signal is absent and the input is floating. Wider DC offset input voltage provides more margin to prevent oscillation. However, setting this DC offset too wide will increase the offset between the true and complementary input signals during normal operation. Board designers should consider these trade-offs when choosing the DC offset voltage.

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