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# 78K0R/Kx3 Microcontroller

# Sample Program

# Operation Manual

## (Multiple PWM Output (Timer Array Unit), C Source)

This software is for reference only and NEC Electronics does not guarantee its operation.
Thoroughly evaluate this software on your set prior to use.

ZUD-CC-07-0086-E
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1st Product Solution Group, Multipurpose Microcomputer Systems Division,
Microcomputer Operations Unit
NEC Electronics Corporation

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**CONTENTS**

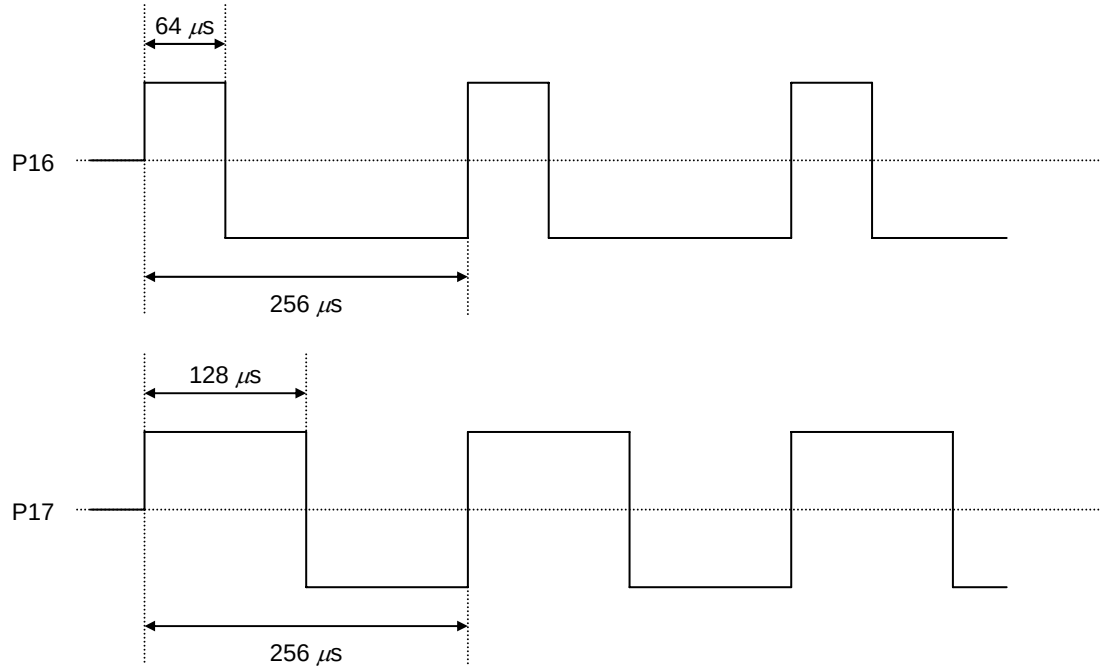
## 1. OVERVIEW

This manual explains the sample program functions of multiple PWM output for the 78K0R/Kx3 microcontroller.

In this sample program, timer channels 0, 1, and 2 are used and multiple PWM signals are output.

Channel 0 is used as the master, and channels 1 and 2 are used as the slaves.

The output pins are P16 and P17. P16 outputs a signal with a pulse cycle of 256 $\mu$s and a duty factor of 25%. P17 outputs a signal with a pulse cycle of 256 $\mu$s and a duty factor of 50%.



## 2. RESOURCES USED

| Resource | Description | Remark |
|---|---|---|
| Main clock specification | Internal high-speed oscillator used (8 MHz (TYP.)) | Supplied to CPU and peripheral hardware |
| | High-speed system clock used (20 MHz) | Oscillated by initial processing |
| Subclock | XT1 (32.768 kHz) | Oscillated by initial processing |
| Related hardware | Peripheral enable register 0 (PER0) | Controls the input clock of the timer array unit. |
| | Timer clock select register 0 (TPS0) | Operation clock: CK01 (1/2), 4 MHz (0.25 μs) |
| | Timer mode register 00 (TMR00) | Operation clock: CK01, 8 MHz<br>Master channel |
| | Timer mode registers 01, 02 (TMR01, TMR02) | Operation clock: CK01, 8 MHz<br>Slave channels |
| | Timer data register 00 (TDR00) | Pulse cycle: 256 μs |
| | Timer data register 01 (TDR01) | Duty factor: 25% |
| | Timer data register 02 (TDR02) | Duty factor: 50% |
| | Timer output mode register 0 (TOM0) | Channel 0: Toggle mode<br>Channel 1: Combination operation mode with channel 0<br>Channel 2: Combination operation mode with channel 0 |
| | Timer output level register 0 (TOL0) | Channels 1, 2 positive logic output (active high) |
| | Timer output register 0 (TO0) | Timer output values of channels 1 and 2 are “0”. |
| | Timer output enable register 0 (TOE0) | Enables the operation of TO01 and TO02 by counting operation. |
| | Timer channel start register 0 (TS00) | |
| | Timer channel stop register 0 (TT0) | |
| | Port mode register (P1) | |
| | Port register (P1) | |
| I/O | Output: TO01 (P16), TO02 (P17) | |
| Interrupt | Timer channels 0, 1, 2 | |
| Others | Not used | |

## 3. SOFTWARE CONFIGURATION

Files

| File Name | Processing Outline |
|---|---|
| K0R_def.h | Definition file |
| K0R_init.c | Initialization processing |
| K0R_ext.h | External declaration |
| K0R_main.c | Main processing |
| K0R_sfr_set.c | Multiple PWM output |

## 4. FUNCTION EXPLANATIONS

[File name]

K0R_main.c

Function

| Function Name | Processing Outline | Argument | Return Value |
|---|---|---|---|
| main | Multiple PWM output main processing | None | None |

Function explanations

| Function name | main |
|---|---|
| Processing | Multiple PWM output main processing |
| Argument | – |
| Return value | – |
| Description | Executes initialization processing and then starts multiple PWM output main processing. |
| Remark | – |

[File name]

K0R_sfr_set.c

Functions

| Function Name | Processing Outline | Argument | Return Value |
|---|---|---|---|
| STM_MINI | Initializes multiple PWM output. | None | None |
| STM_MSTT | Starts multiple PWM output operation. | None | None |
| STM_MSTP | Stops multiple PWM output operation. | None | None |

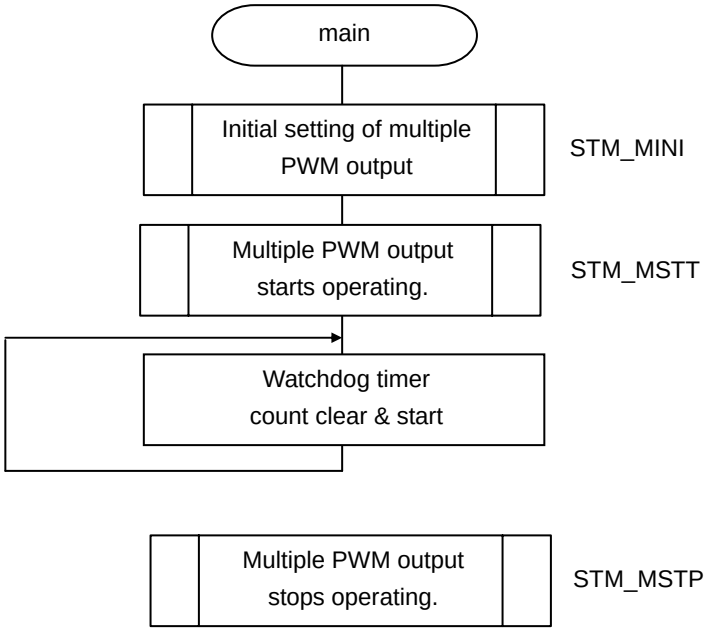
Function explanations

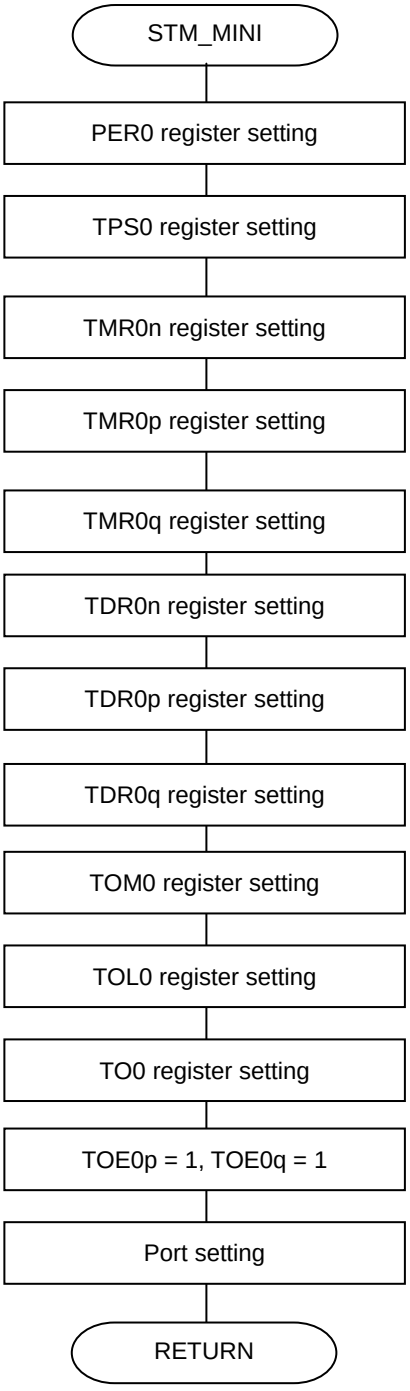
| Function name | STM_MINI |
|---|---|
| Processing | Initializes multiple PWM output. |
| Argument | – |
| Return value | – |
| Description | Initializes the timer array unit.<br>• Supplies a timer array unit input clock.<br>• Sets the clock frequency to 0.25 μs.<br>Initializes timer channel 0 (master).<br>• Operation mode: Operation clock CK01, master channel, interval timer mode<br>• Output mode: Toggle operation mode<br>• Sets the pulse cycle to 256 μs (0.25 μs × 1,024).<br>Initializes timer channel 1 (slave).<br>• Operation mode: Operation clock CK01, slave channel, one-count mode<br>• Output mode: Combination operation mode<br>• Sets the duty factor to 25% ((256/1,024) × 100).<br>• Enables output.<br>Initializes timer channel 2 (slave).<br>• Operation mode: Operation clock CK01, slave channel, one-count mode<br>• Output mode: Combination operation mode<br>• Sets the duty factor to 50% ((512/1,024) × 100).<br>• Enables output.<br>Sets P16 and P17 to the output mode. |
| Remark | – |

| Function name | STM_MSTT |
|---|---|
| Processing | Starts multiple PWM output operation. |
| Argument | – |
| Return value | – |
| Description | Enables the output operation of timer channels 1 and 2 (slave).<br>Starts operation of timer channels 0, 1, and 2. |
| Remark | – |

| | |
|---|---|
| Function name | STM_MSTP |
| Processing | Stops multiple PWM output operation. |
| Argument | – |
| Return value | – |
| Description | Stops operation of timer channels 0, 1, and 2.<br>Disables the output operation of timer channels 1 and 2 (slave). |
| Remark | – |

## 5. FLOWCHARTS






Supplies a timer array unit input clock.

Determines the clock frequency (CK01 used).
Sets the clock cycle of CK01 to 0.25 $\mu$s.

CK01 used, master channel, interval timer mode

CK01 used, slave channel, one-count mode, trigger input valid

CK01 used, slave channel, one-count mode, trigger input valid

Sets the timer data register.
Pulse cycle: 256 $\mu$s

Sets the timer data register.
Duty factor: 25%

Sets the timer data register.
Duty factor: 50%

Sets the timer output mode register.

Sets the timer output level register.

Sets the timer output register.

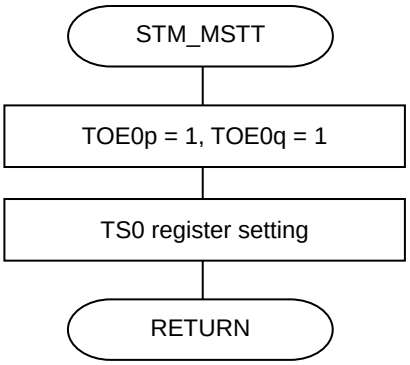
Enables TO01 output operation (slave).
Enables TO02 output operation (slave).

Validates data output of the target channel by setting the port register and port mode register.

**Remark** n = 0, 2, 4 can be set.

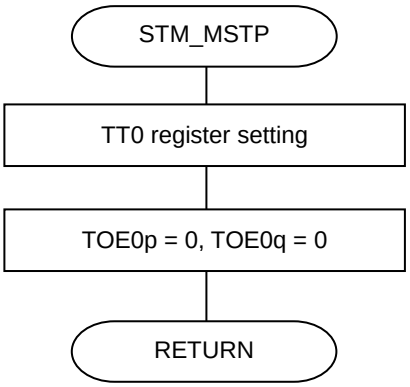
p = n + 1, q = n + 2

n = 0, p = 1, q = 2 for this sample program.




Enables TO0p output operation (slave).
Enables TO0q output operation (slave).

Enables timer channel n, p, and q operation.




Stops timer channel n, p, and q operation.

Disables TO0p output operation (slave).
Disables TO0q output operation (slave).

**Remark** n = 0, 2, 4 can be set.

p = n + 1, q = n + 2

n = 0, p = 1, q = 2 for this sample program.