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7560 Group

Interrupt

1. Abstract

The following document describes the interrupt in the 7560 group.

2. Introduction

The application example described in this document is applied to the following conditions:
Applicable MCU: 7560 Group

3. Contents

3.1 Interrupt Source

In the 7560 group, an interrupt is generated by 16 sources among 17 sources : 7 external, 9 internal and 1 software. Since these are vector interrupts with a fixed priority, the higher-priority interrupt is acknowledged first when two or more interrupt are requested during the same sampling. This priority is stabled by hardware, but the priority process can be performed by a program, using the interrupt enable bit and an interrupt disable flag. Table 3.1 shows the Interrupt Sources, Vector Addresses and Interrupt Priority

Table 3.1 Interrupt Sources, Vector Addresses and Interrupt Priority

Interrupt Source	Priority	Vector Addresses (NOTE 1)		Interrupt Request Generating Conditions	Remark
		High	Low		
Reset (NOTE 2)	1 High	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (polarity programmable)
INT1	3	FFF916	FFF816	At detection of either rising or falling edge of INT1 input	External interrupt (polarity programmable)
Receive Serial I/O1	4	FFF716	FFF616	At completion of serial I/O1 data receive	Valid when serial I/O1 is selected
Transmit Serial I/O1	5	FFF516	FFF416	At completion of serial I/O1 transmit shift or when transmit buffer is empty	Valid when serial I/O1 is selected
Timer X	6	FFF316	FFF216	At timer X underflow	
Timer Y	7	FFF116	FFF016	At timer Y underflow	
Timer 2	8	FFEF16	FFEE16	At timer 2 underflow	
Timer 3	9	FFED16	FFEC16	At timer 3 underflow	
CNTR0	10	FFEB16	FFEA16	At detection of either rising or falling edge of CNTR0 input	External interrupt (polarity programmable)
CNTR1	11	FFE916	FFE816	At detection of either rising or falling edge of CNTR1 input	External interrupt (polarity programmable)
Timer 1	12	FFE716	FFE616	At timer 1 underflow	
INT2	13	FFE516	FFE416	At detection of either rising or falling edge of INT2 input	External interrupt (polarity programmable)
Serial I/O2	14	FFE316	FFE216	At completion of serial I/O2 data receive/ transmit	Valid when serial I/O2 is selected
Key Input (Key-on wake up)	15	FFE116	FFE016	At falling edge of conjunction of input level for port P2 (at input mode)	External interrupt (valid at falling edge)
ADT	16	FFDF16	FFDE16	At falling edge of ADT pin input	Valid when ADT interrupt is selected External interrupt (Valid at falling edge)
A/D Conversion				At completion of A/D conversion	Valid when A/D interrupt is selected
BRK Instruction	17 Low	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

NOTES:
1. Vector addresses contain interrupt jump destination addresses.
2. Reset is not an interrupt. Reset has the higher priority than all interrupts.

3.2 Interrupt Control

The acknowledgement of all interrupts, excluding the BRK instruction, can be controlled by the interrupt request bit, interrupt enable bit and an interrupt disable flag, as described in detail below. Figure 3.1 shows the Interrupt Control Diagram.

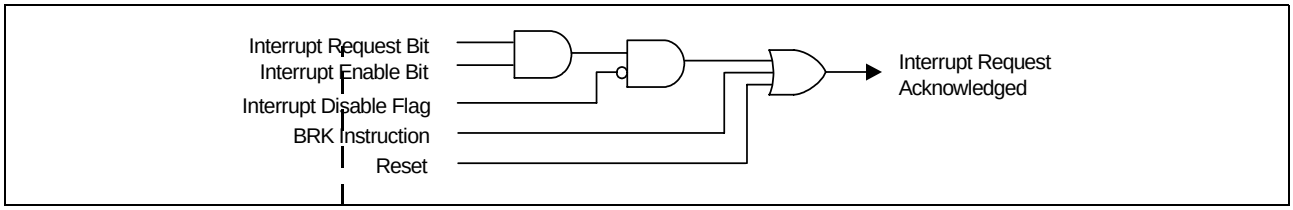

Figure 3.1 Interrupt Control Diagram

The interrupt request bit, interrupt enable bit and interrupt disable flag function independently and do not affect each other. An interrupt request is acknowledged when all the following conditions are met.

- Interrupt disable flag "0"
- Interrupt request bit "1"
- Interrupt enable bit "1"

Although the interrupt priority is stabled by hardware, the priority process can be performed by a program using the above bits and flag.

3.2.1 Interrupt Disable Flag

The interrupt disable flag is allocated to the bit 2 in the processor status register. The interrupt disable flag controls the acknowledgement of interrupt request, excluding the BRK instruction. When this flag is set to "1", the acknowledgement of the interrupt request is disabled. When this flag is set to "0", the acknowledgement of the interrupt request is enabled. This flag is set to "1" with the SEI instruction and is set to "0" with the CLI instruction. When an interrupt request is acknowledged, the processor status register is stored and the interrupt disable flag remains "0". After that, this flag is automatically set to "1" and multiple interrupts are disabled. To use multiple interrupts, set this flag to "0" with the CLI instruction within the interrupt routine. The processor status register is returned with the RTI instruction.

3.2.2 Interrupt Request Bit

Once an interrupt request is generated, the applicable interrupt request bit is set to "1" and remains "1" until the interrupt request is acknowledged. When the interrupt request is acknowledged, this bit is automatically set to "0". Each interrupt request bit can be set to "0", but cannot be set to "1" by a program.

3.2.3 Interrupt Enable Bit

The interrupt enable bits control the acknowledgement of the applicable interrupt request. When an interrupt enable bit is set to "0", the acknowledgement of the interrupt request is disabled. If an interrupt request is generated when the interrupt request bit is set to "1", the interrupt request cannot be acknowledged. In this case, unless the interrupt request bit is set to "0" by a program, the interrupt request bit remains "1". When an interrupt enable bit is set to "1", the acknowledgement of the interrupt request is enabled. If an interrupt request is generated when setting the interrupt request bit to "1", the interrupt request is acknowledged (When interrupt disable flag = 0). Each interrupt enable bit can be set to "0" or "1" by a program. Set the interrupt enable bit of the interrupt which is not used to "0".

3.3 Interrupt Operation

When an interrupt request is acknowledged, the contents immediately before the acknowledgement of the interrupt requests of registers shown below are automatically stored into the stack area in the order of (1), (2) and (3).

(1) High-order contents of program counter (PC_H)
(2) Low-order contents of program counter (PC_L)
(3) Contents of processor status register (PS)

After the contents of the above registers are stored into the stack area, the program will be branched to the jump destination address of the acknowledged interrupt. When the RTI instruction is executed, the contents of the above registers stored into the stack area are returned in the order of (3), (2) and (1) and the routine before the acknowledgement of the interrupt request is continued. Figure 3.2 shows the Interrupt Operation Diagram.

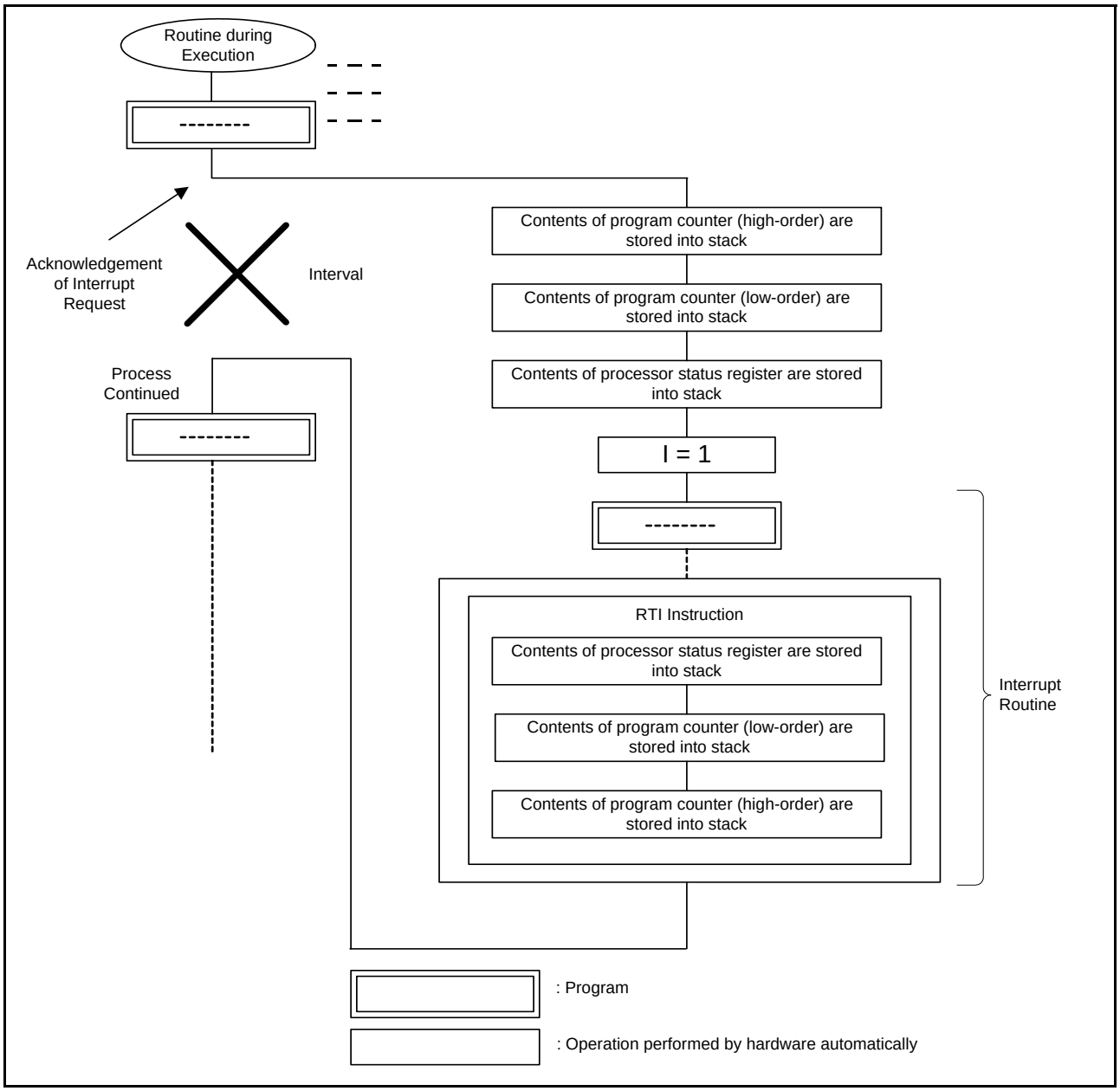

Figure 3.2 Interrupt Operation Diagram

3.3.1 Processing upon Acknowledgement of Interrupt Request

Upon acknowledgement of an interrupt request, the following operations are automatically performed.
(1) When the process being executed is terminated, the interrupt request is acknowledged.
(2) The contents of the program counter and the processor status register are stored into the stack area. Figure 3.3 shows the Changes of the Stack Pointer and Program Counter upon Acknowledgement of Interrupt Request.
(3) At the same time the contents are stored into the stack area, the jump destination address (the beginning address of the interrupt routine) of an acknowledged interrupt is transferred to the program counter from an interrupt vector.
(4) The interrupt request bit of the acknowledged interrupt is set to "0". The interrupt disable flag is set to "1" so that multiple interrupts are disabled.
(5) The interrupt routine is executed.

Therefore, it is necessary to set the stack pointer and the jump destination address in the vector applicable to each interrupt for executing the interrupt routine.

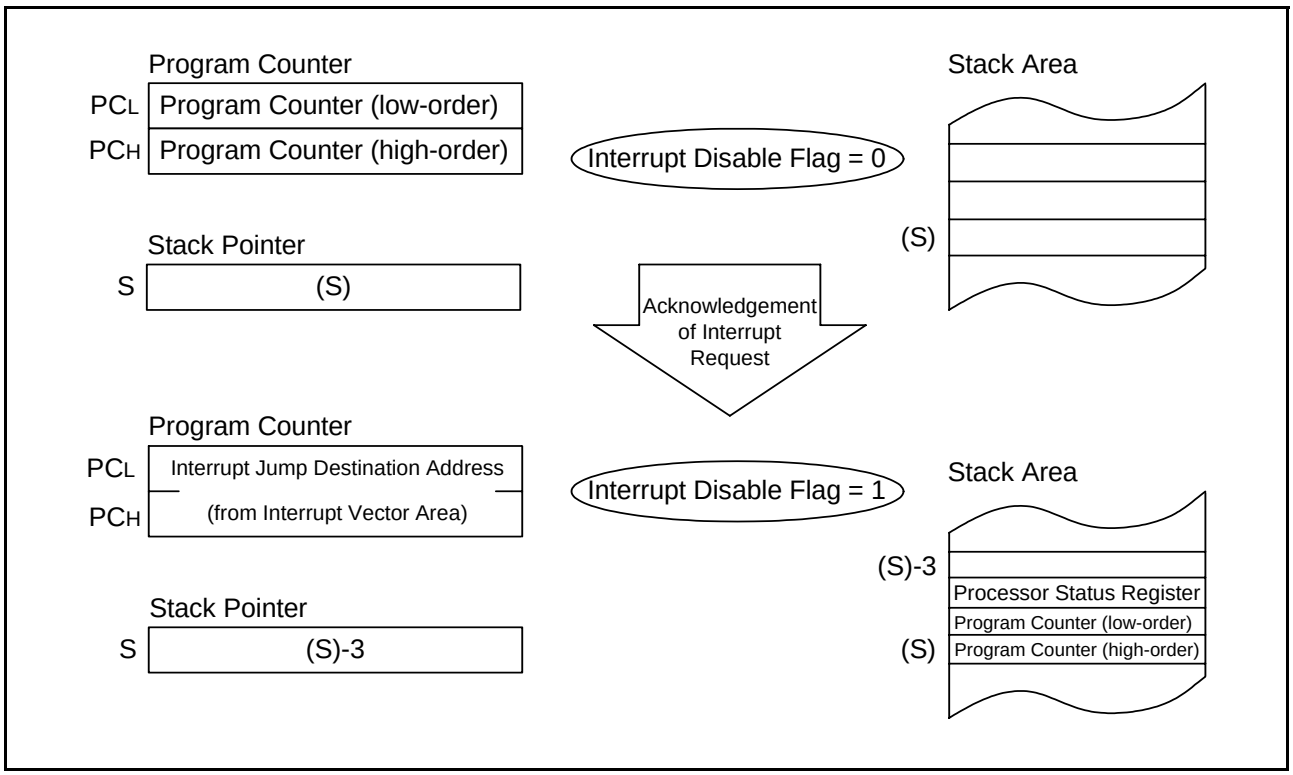

Figure 3.3 Changes of the Stack Pointer and Program Counter upon Acknowledgement of Interrupt Request

3.3.2 Acknowledged Timing of Interrupt Request

Here describes the process until an interrupt routine is executed after an interrupt request is generated. If an interrupt request is generated, an interrupt request is acknowledged after the instruction under execution at the time is terminated, and an interrupt process starts. Figure 3.4 shows the Time up to Execution of Interrupt Routine and Figure 3.8 shows the Timing Chart of Interrupt Process.

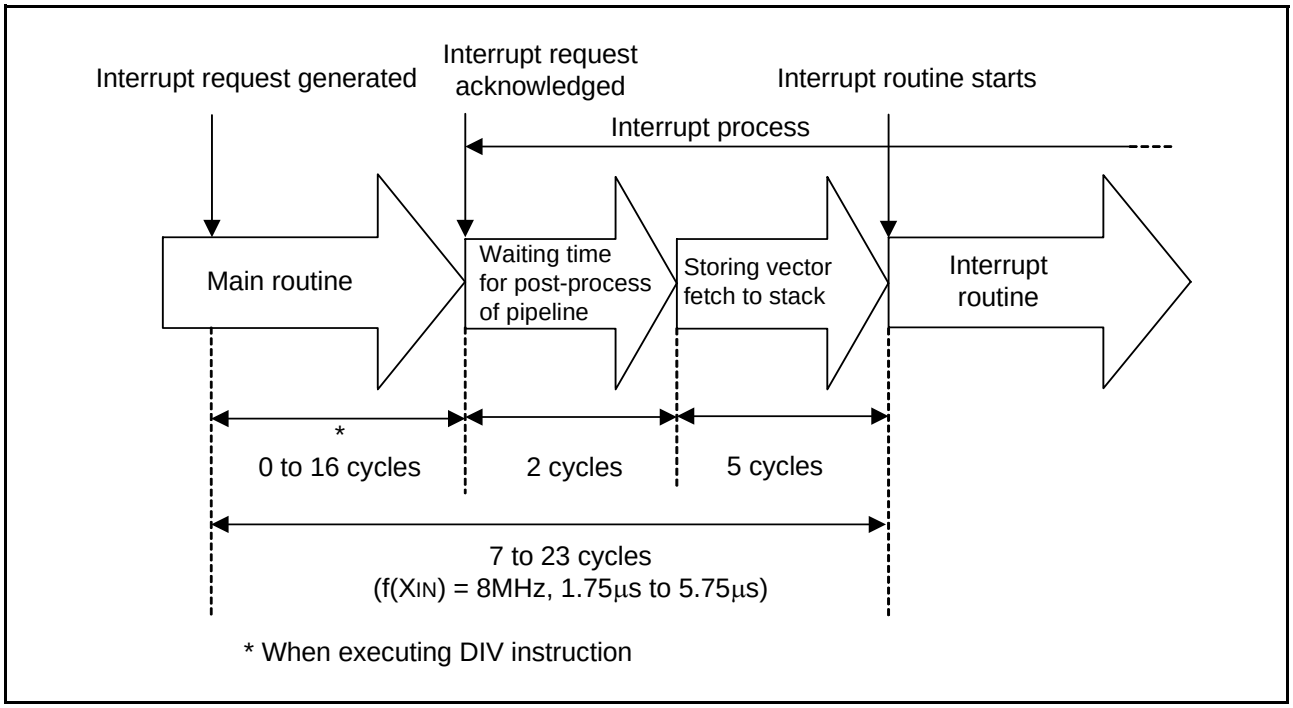

Figure 3.4 Time up to Execution of Interrupt Routine

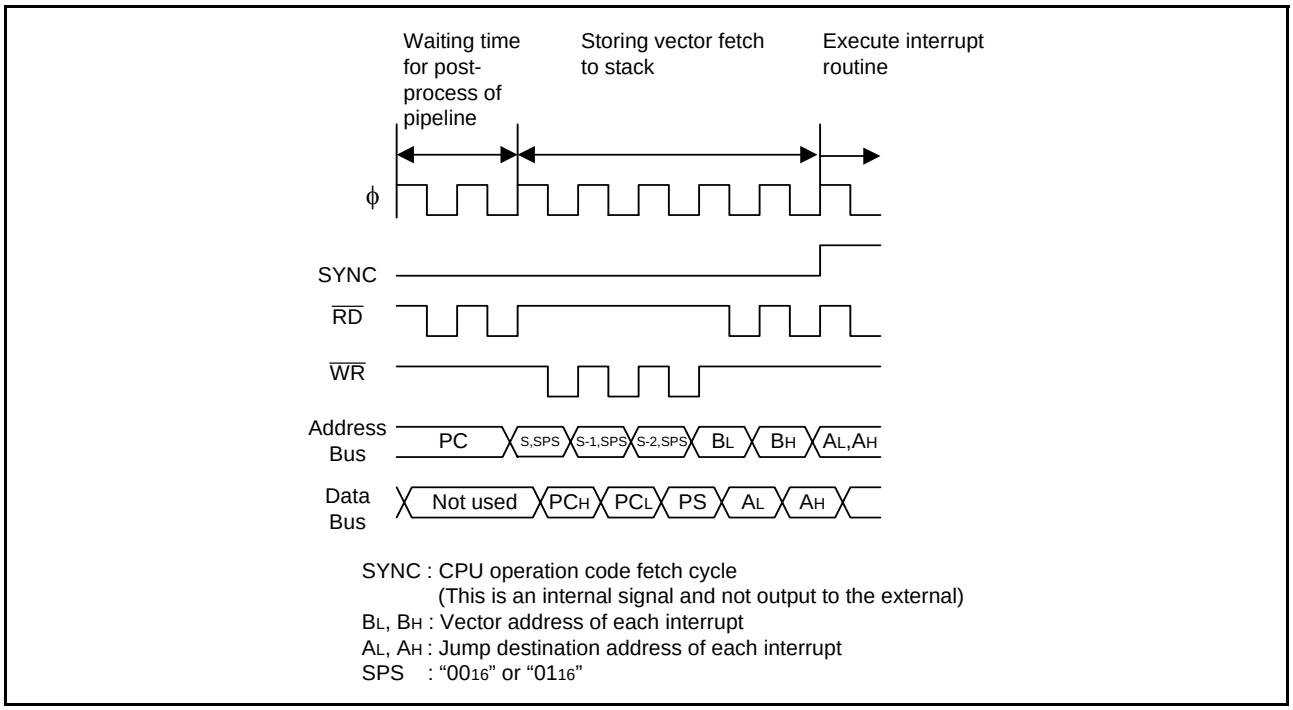

Figure 3.5 Timing Chart of Interrupt Process

3.4 Multiple Interrupts

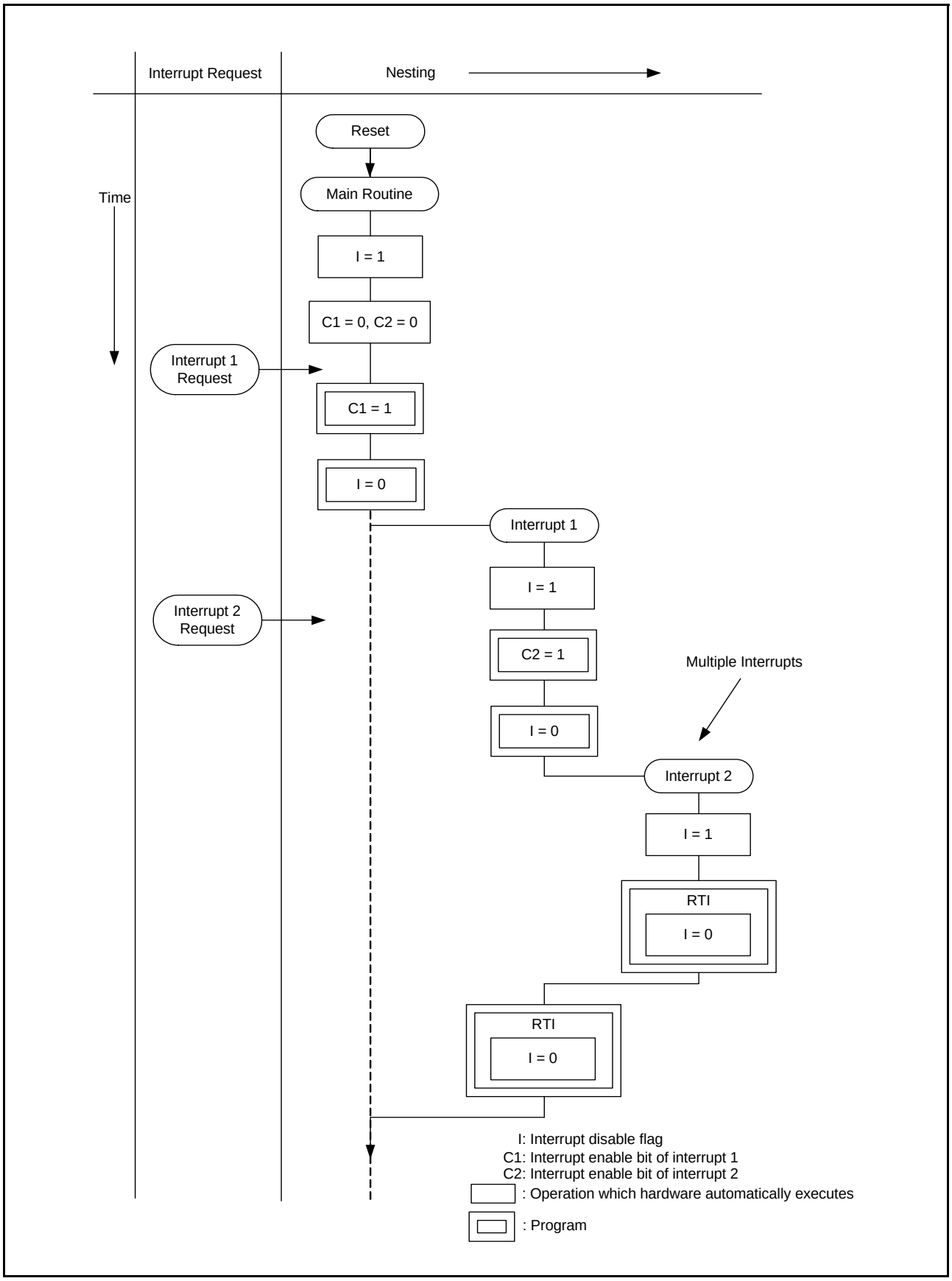

Figure 3.6 Example of Multiple Interrupts

3.5 INTi Interrupt

The INTi (i=0 to 2) interrupt generates an interrupt request by detecting a level change of each INTi pin. The INTi pins are shared with I/O ports. When using as the INTi pin, set the direction register of the sharing port to input mode. Figure 3.7 shows the Relevant Registers Setting.

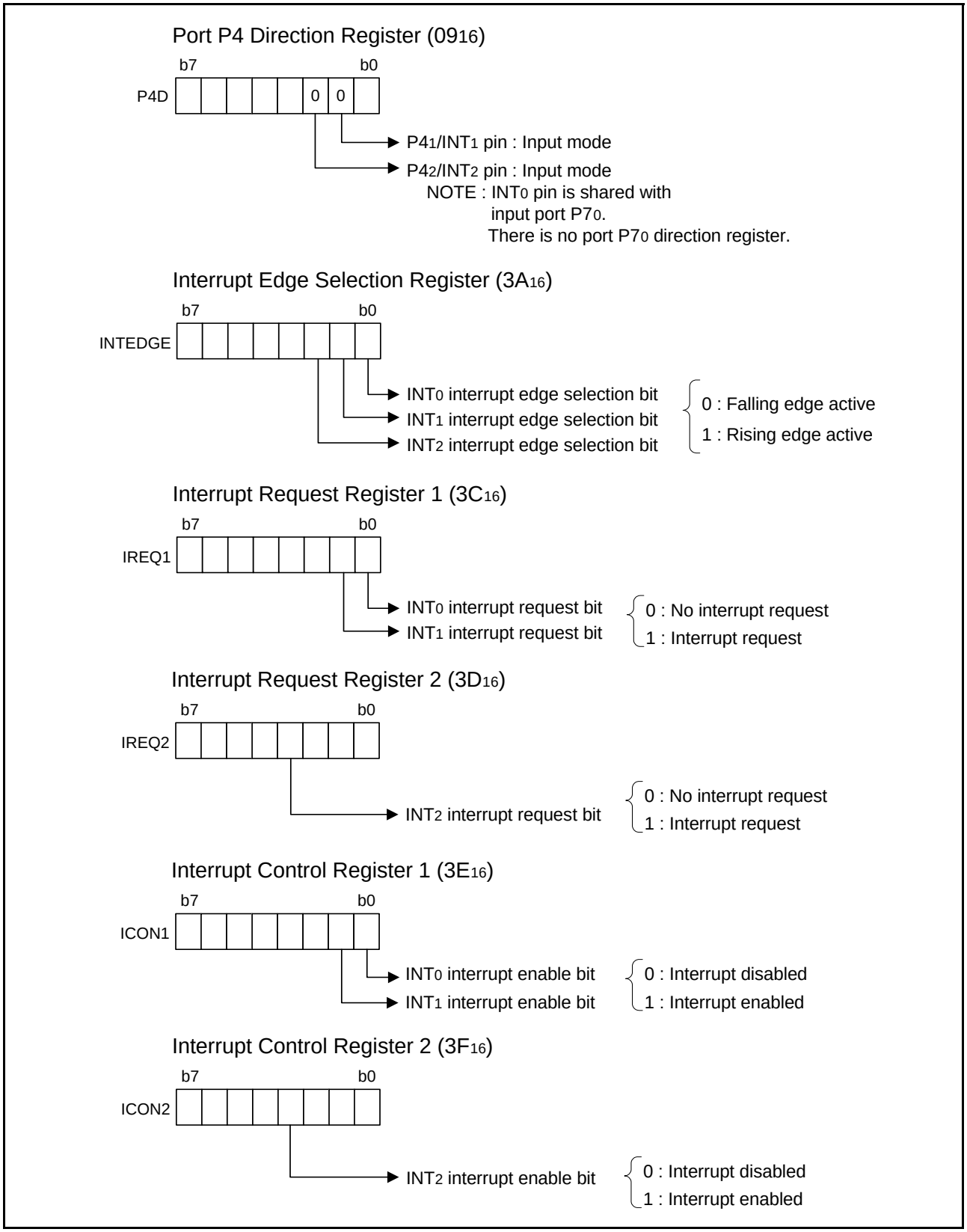

Figure 3.7 Relevant Registers Setting

3.6 CNTRi Interrupt

The CNTRi (i=0, 1) generates an interrupt request by detecting a level change of each CNTRi pin. The CNTRi pins are shared with I/O ports. When using as the CNTRi pin, set the direction register of the sharing port to input mode. Figure 3.8 shows the Relevant Registers Setting.

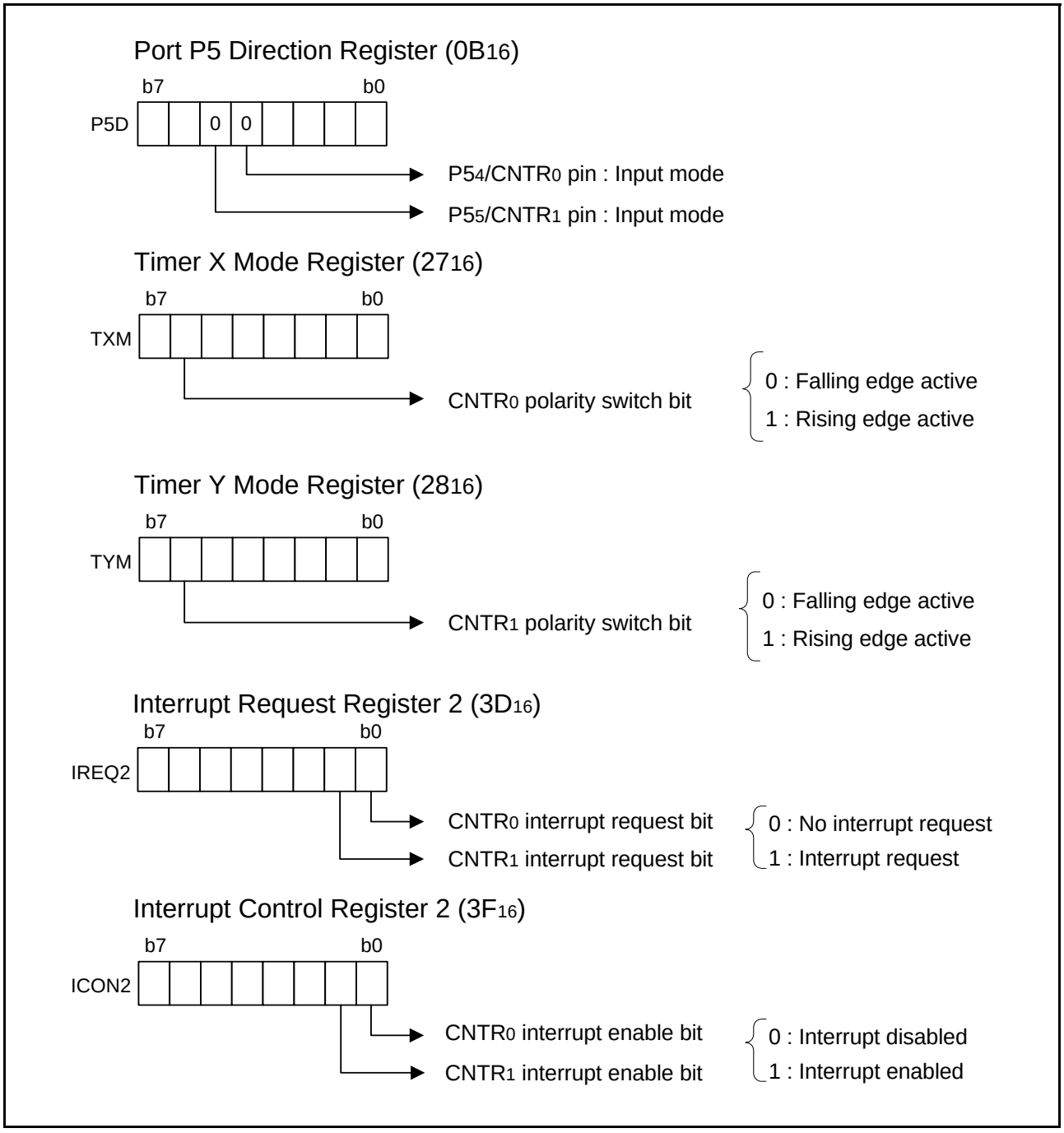

Figure 3.8 Relevant Registers Setting

3.7 ADT Interrupt

The ADT interrupt generates an interrupt request by detecting the falling edge of the ADT pin. The ADT pin is shared with the I/O pin. When using as the ADT pin, set the direction register of the sharing port to input mode. The interrupt vector address is shared with the A/D conversion interrupt. When using the ADT interrupt, set the interrupt source selection bit (bit 6 in the A/D control register (34_{16})) to "1". The falling edge of the ADT pin can be used as an A/D conversion start trigger. When it is not used as an A/D conversion start trigger, set the A/D external trigger valid bit (bit 5 in the A/D control register) to "0". Figure 3.9 shows the Relevant Registers Setting.

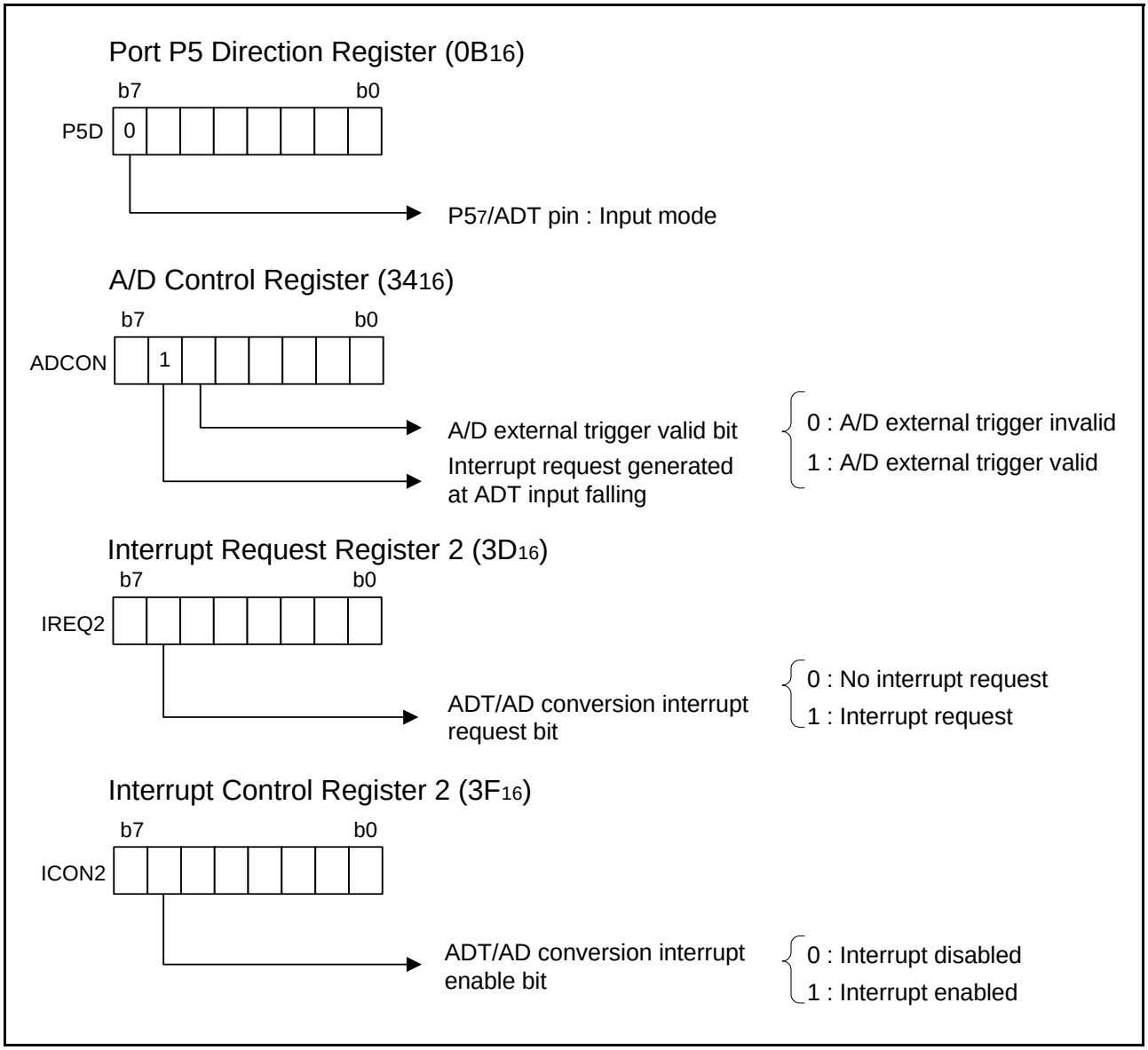

Figure 3.9 Relevant Registers Setting

4. Reference

Data Sheet
7560 Group (A version) Data sheet
7560 Group Data sheet

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REVISION HISTORY	7560 Group Interrupt

Rev.	Date	Description	
		Page	Summary
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