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7546 Group
List of Registers

1. Abstract

This documents describes the 7546 Group registers.

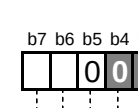
2. Introduction

The registers described in this document are applied to the following:

MCU: 7546 Group

3. Register Configuration

The following shows an example of a control register configuration diagram in this application note, and the definitions of the symbols and terms used in the diagram.



..... register (....)

[Address ....h]

b	Name	Function	*2 After Reset	*3 RW
0	.....bits	0 0: 0 1:	0	RW
1		1 0: ..... 1 1: Not available	0	RW
2	.....bit	0: 1:	0	RW
3	When read, the content is 0. If necessary, set to 0.		0	RO
4	When read, the content is undefined. If necessary, set to 0.		Undefined	-
5	Set to 0.		0	R/W
6	.....flag	0: 1:	0	RW
7	.....bit	0: 1:	0	RW

*1

Blank	: Set to 0 or 1 according to the application.
0	: Set to 0.
1	: Set to 1.
×	: This bit is not used in the specific mode or state. Set to either 0 or 1.
	: Nothing is assigned.

*2

0	: 0 after reset
1	:1 after reset
Undefined	: Undefined after reset

*3

RW	: Read and Write.
RO	: Read only. When written, the content depends on each bit.
WO	: Write only. When read, the content is undefined.
-	: When read, the content is undefined. When written, the content depends on each bit.

4. List of Registers

Port P0 register

b7 b6 b5 b4 b3 b2 b1 b0

Port P0 register (P0)

[Addresses 00h]

b	Name	Function	After Reset	RW
0	Port $P0_0$	•In output mode	Undefined	RW
1	Port $P0_1$	Write: Port latch	Undefined	RW
2	Port $P0_2$	Read: Port latch	Undefined	RW
3	Port $P0_3$	•In input mode	Undefined	RW
4	Port $P0_4$	Write: Port latch	Undefined	RW
5	Port $P0_5$	Read: Pin value	Undefined	RW
6	Port $P0_6$		Undefined	RW
7	Port $P0_7$		Undefined	RW

Fig. 4.1 Configuration of Port P0 register

Port P0 direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port P0 direction register (P0D)

[Addresses 01h]

b	Name	Function	After Reset	RW
0	Port $P0_0$ direction register	0: Input mode 1: Output mode	0	WO
1	Port $P0_1$ direction register	0: Input mode 1: Output mode	0	WO
2	Port $P0_2$ direction register	0: Input mode 1: Output mode	0	WO
3	Port $P0_3$ direction register	0: Input mode 1: Output mode	0	WO
4	Port $P0_4$ direction register	0: Input mode 1: Output mode	0	WO
5	Port $P0_5$ direction register	0: Input mode 1: Output mode	0	WO
6	Port $P0_6$ direction register	0: Input mode 1: Output mode	0	WO
7	Port $P0_7$ direction register	0: Input mode 1: Output mode	0	WO

Note: In the port set to output mode, the pull-up control bit is disabled and the pull-up resistor is not connected.

Fig. 4.2 Configuration of Port P0 direction register

Port P1 register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 □ □ □ □ □

Port P1 register (P1)

[Address 02h]

b	Name	Function	After Reset	RW
0	Port $P1_0$	•In output mode Write: Port latch	Undefined	RW
1	Port $P1_1$	Read: Port latch or	Undefined	RW
2	Port $P1_2$	peripheral function output (Note)	Undefined	RW
3	Port $P1_3$	•In input mode Write: Port latch	Undefined	RW
4	Port $P1_4$	Read: Pin value	Undefined	RW
5	When read, the content is undefined. If necessary, set to 0.		Undefined	-
6			Undefined	-
7			Undefined	-

Note: When the shared output function is selected for $P1_4$/$CNTR_0$, the output value is read.

Fig. 4.3 Configuration of Port P1 register

Port P1 direction register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 □ □ □ □ □

Port P1 direction register (P1D)

[Address 03h]

b	Name	Function	After Reset	RW
0	Port $P1_0$ direction register	0: Input mode 1: Output mode	0	WO
1	Port $P1_1$ direction register	0: Input mode 1: Output mode	0	WO
2	Port $P1_2$ direction register	0: Input mode 1: Output mode	0	WO
3	Port $P1_3$ direction register	0: Input mode 1: Output mode	0	WO
4	Port $P1_4$ direction register	0: Input mode 1: Output mode	0	WO
5	When read, the content is undefined. If necessary, set to 0.		Undefined	-
6			Undefined	-
7			Undefined	-

Fig. 4.4 Configuration of Port P1 direction register

Port P2 register

b7	b6	b5	b4	b3	b2	b1	b0
0	0						

Port P2 register (P2)

[Address 04h]

b	Name	Function		After Reset	RW
0	Port $P2_0$	•In output mode	Write: Port latch	Undefined	RW
1	Port $P2_1$		Read: Port latch	Undefined	RW
2	Port $P2_2$	•In input mode	Write: Port latch	Undefined	RW
3	Port $P2_3$		Read: Pin value	Undefined	RW
4	Port $P2_4$			Undefined	RW
5	Port $P2_5$			Undefined	RW
6	If necessary, set to 0.			Undefined	RW
7				Undefined	RW

Fig. 4.5 Configuration of Port P2 register

Port P2 direction register

b7	b6	b5	b4	b3	b2	b1	b0
1	1						

Port P2 direction register (P2D)

[Address 05h]

b	Name	Function	After Reset	RW
0	Port $P2_0$ direction register	0: Input mode 1: Output mode	0	WO
1	Port $P2_1$ direction register	0: Input mode 1: Output mode	0	WO
2	Port $P2_2$ direction register	0: Input mode 1: Output mode	0	WO
3	Port $P2_3$ direction register	0: Input mode 1: Output mode	0	WO
4	Port $P2_4$ direction register	0: Input mode 1: Output mode	0	WO
5	Port $P2_5$ direction register	1: Input mode 1: Output mode	0	WO
6	Always set to 1.		0	WO
7			0	WO

Fig. 4.6 Configuration of Port P2 direction register

Port P3 register

b7 b6 b5 b4 b3 b2 b1 b0
0 0

Port 3 register (P3)

[Address 06h]

b	Name	Function		After Reset	RW
0	Port $P1_0$	•In output mode	Write: Port latch	Undefined	RW
1	Port $P1_1$		Read: Port latch	Undefined	RW
2	Port $P1_2$	•In input mode	Write: Port latch	Undefined	RW
3	Port $P1_3$		Read: Pin value	Undefined	RW
4	Port $P1_4$			Undefined	RW
5	If necessary, set to 0.			Undefined	RW
6				Undefined	RW
7		•In output mode	Write: Port latch	Undefined	RW
			Read: Port latch		
		•In input mode	Write: Port latch		
			Read: Pin value		

Fig. 4.7 Configuration of Port P3 register

Port P3 direction register

b7 b6 b5 b4 b3 b2 b1 b0
1 1

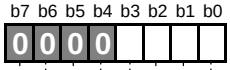
Port P3 direction register (P3D)

[Address 07h]

b	Name	Function	After Reset	RW
0	Port $P3_0$ direction register	0: Input mode 1: Output mode	0	WO
1	Port $P3_1$ direction register	0: Input mode 1: Output mode	0	WO
2	Port $P3_2$ direction register	0: Input mode 1: Output mode	0	WO
3	Port $P3_3$ direction register	0: Input mode 1: Output mode	0	WO
4	Port $P3_4$ direction register	0: Input mode 1: Output mode	0	WO
5	Always set to 1.		0	WO
6			0	WO
7	Port $P3_7$ direction register	0: Input mode 1: Output mode	0	WO

Fig. 4.8 Configuration of Port P3 direction register

Interrupt source set register

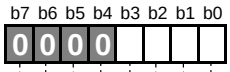


[Address 0Ah]

b	Name	Function	After Reset	RW
0	Key-on wakeup interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
1	UART1 bus collision detection interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
2	A/D conversion interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
3	Timer 1 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
4	When read, the content is 0. If necessary, set to 0.		0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.9 Configuration of Interrupt source set register

Interrupt source discrimination register



[Address 0Bh]

b	Name	Function	After Reset	RW
0	Key-on wakeup interrupt discrimination bit	0: No interrupt request 1: Interrupt requested	0	RW
1	UART1 bus collision detection interrupt discrimination bit	0: No interrupt request 1: Interrupt requested	0	RW
2	A/D conversion interrupt discrimination bit	0: No interrupt request 1: Interrupt requested	0	RW
3	Timer 1 interrupt discrimination bit	0: No interrupt request 1: Interrupt requested	0	RW
4	When read, the content is 0. If necessary, set to 0.		0	RO
5			0	RO
6			0	RO
7			0	RO

Note: Use the LDM instruction to clear the interrupt discrimination bit.
LDM #$0n, $0B
Set the following values to n.
0: Interrupt discrimination bit to be cleared
1: Other interrupt discrimination bits
Ex.) When the key-on wakeup interrupt discrimination bit is cleared;
LDM #00001110B, $0B.

Fig. 4.10 Configuration of Interrupt source discrimination register

Capture register i (low-order)

b7 b6 b5 b4 b3 b2 b1 b0

Capture register i (CAPiL) (i = 0, 1)

[Addresses 0Ch, 0Eh]

b	Name	Function	After Reset	RW
0		• The capture register i (CAPiL) is used to read the timer count value (low-order) by capture input. • Reading from the register for each channel is controlled by setting the value of the capture register read pointer. Reading from each register is in the following order; 1. Set the value of the corresponded input capture channel to the capture register read pointer. 2. Read from the capture register (low-order) and the capture register (high-order). • If a capture trigger is input while the capture registers (low-order/high-order) are read, their values result in values captured at different timings. The results should be compared by reading multiple times via software.	Undefined	RO
1			Undefined	RO
2			Undefined	RO
3			Undefined	RO
4			Undefined	RO
5			Undefined	RO
6			Undefined	RO
7			Undefined	RO

Fig.4.11 Configuration of Capture register i (low-order)

Capture register i (high-order)

b7 b6 b5 b4 b3 b2 b1 b0

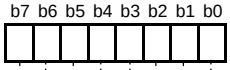
Capture register i (CAPiH) (i = 0, 1)

[Addresses 0Dh, 0Fh]

b	Name	Function	After Reset	RW
0		• The capture register i (CAPiH) is used to read the timer count value (high-order) by capture input. • Reading from the register for each channel is controlled by setting the value of the capture register read pointer. Reading from each register is in the following order; 1. Set the value of the corresponded input capture channel to the capture register read pointer. 2. Read from the capture register (low-order) and the capture register (high-order). • If a capture trigger is input while the capture registers (low-order/high-order) are read, their values result in values captured at different timings. The results should be compared by reading multiple times via software.	Undefined	RO
1			Undefined	RO
2			Undefined	RO
3			Undefined	RO
4			Undefined	RO
5			Undefined	RO
6			Undefined	RO
7			Undefined	RO

Fig.4.12 Configuration of Capture register i (high-order)

Compare register (low-order)



Compare register (CMPL)

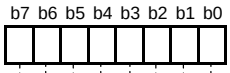
[Address 10h]

b	Name	Function	After Reset	RW
0		• The compare register (CMPL) is used to set the timer count value (low-order) by compare output. • Writing to the register for each channel is controlled by the setting value of the compare register write pointer. Write to each register in the following order: 1. Set the value of corresponded output compare channel to the compare register write pointer. 2. Write a value to the compare register (low-order) and compare register (high-order).	0	WO
1			0	WO
2			0	WO
3			0	WO
4			0	WO
5			0	WO
6			0	WO
7			0	WO

Notes 1: When the selected source timer of each compare channel is stopped, written data to compare register is loaded to the compare latch simultaneously.
2: Do not write the same value to compare latch x0 and x1 (x = 0, 1, 2, 3).
3: When the setting value of the compare latch is larger than the timer setting value, no compare match signal is generated. This allows the output waveform to be fixed to "L" or "H" level.
However, when the setting value of another compare latch is smaller than the timer setting value, the compare match signal is generated so that the compare match interrupt occurs.

Fig.4.13 Configuration of Compare register (low-order)

Compare register (high-order)



Compare register (CMPH)

[Address 11h]

b	Name	Function	After Reset	RW
0		• The compare register (CMPH) is used to set the timer count value (high-order) by compare output. • Writing to the register for each channel is controlled by the setting value of the compare register write pointer. Write to each register in the following order: 1. Set the value of corresponded output compare channel to the compare register write pointer. 2. Write a value to the compare register (low-order) and compare register (high-order).	0	WO
1			0	WO
2			0	WO
3			0	WO
4			0	WO
5			0	WO
6			0	WO
7			0	WO

Notes 1: When the selected source timer of each compare channel is stopped, written data to compare register is loaded to the compare latch simultaneously.
2: Do not write the same value to both compare latch x0 and x1 (x = 0, 1, 2, 3).
3: When the setting value of the compare latch is larger than the timer setting value, no compare match signal is generated. This allows the output waveform to be fixed to "L" or "H" level.
However, when the setting value of another compare latch is smaller than the timer setting value, the compare match signal is generated so that the compare match interrupt occurs.

Fig.4.14 Configuration of Compare register (high-order)

Capture/compare register R/W pointer

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0

Capture/compare register R/W pointer (CCRP)

[Address 12h]

b	Name	Function	After Reset	RW
0	Compare register R/W pointer	b2 b1 b0 0 0 0: Compare latch 00 0 0 1: Compare latch 01 0 1 0: Compare latch 10 0 1 1: Compare latch 11 1 0 0: Compare latch 20 1 0 1: Compare latch 21 1 1 0: Compare latch 30 1 1 1: Compare latch 31	0	RW
1			0	RW
2			0	RW
3	When read, the content is 0. If necessary, set to 0.		0	RO
4	Capture register 0 R/W pointer	0: Capture latch 00 1: Capture latch 01	0	RW
5	Capture register 1 R/W pointer	0: Capture latch 10 1: Capture latch 11	0	RW
6	When read, the content is 0. If necessary, set to 0.		0	RO
7			0	RO

Fig. 4.15 Configuration of Capture/compare register R/W pointer

Capture software trigger register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0

Capture software trigger register (CSTR)

[Address 13h]

b	Name	Function	After Reset	RW
0	Capture latch 00 software trigger bit	Each software trigger occurs by setting 1 to the corresponding bit. (When read, the content is 0.)	0	RW
1	Capture latch 01 software trigger bit		0	RW
2	Capture latch 10 software trigger bit		0	RW
3	Capture latch 11 software trigger bit		0	RW
4	When read, the content is 0. If necessary, set to 0.		0	RO
5			0	RO
6			0	RO
7			0	RO

Note: The value of the capture x status bit is undefined when the input capture is performed simultaneously to the two capture latches (x0 and x1) in the same channel as follows:
- 1 is written to the capture latch y software trigger bit of the capture latches (x0 and x1) at the same time, or
- 1 is written to the capture latch y software trigger bit of one of the capture latches (x0 or x1) and an external trigger is input to the other capture latch at the same time (x = 0 or 1, y = 00, 01, 10, 11).

Fig. 4.16 Configuration of Capture software trigger register

Compare register re-load register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 | | | |

Compare register re-load register (CMPR)

[Address 14h]

b	Name	Function	After Reset	RW
0	Compare latch 00, 01 re-load bit	0: Re-load disabled 1: Re-load at next underflow	0	RW
1	Compare latch 10, 11 re-load bit	0: Re-load disabled 1: Re-load at next underflow	0	RW
2	Compare latch 20, 21 re-load bit	0: Re-load disabled 1: Re-load at next underflow	0	RW
3	Compare latch 30, 31 re-load bit	0: Re-load disabled 1: Re-load at next underflow	0	RW
4	When read, the content is 0. If necessary, set to 0.		0	RO
5			0	RO
6			0	RO
7			0	RO

Note: When 1 is set to the compare latch y re-load bit, the value set in the compare register is loaded to the compare latch corresponding to each channel at the next timer underflow (y = 00, 01, 10, 11, 20, 21, 30, 31).

Fig. 4.17 Configuration of Compare register re-load register

Port P0P3 drive capacity control register

b7 b6 b5 b4 b3 b2 b1 b0
| | | | | | | | |

Port P0P3 drive capacity control register (DCCR)

[Address 15h]

b	Name	Function	After Reset	RW
0	Port $P0_0$ drive capacity bit	0: Low 1: High	0	RW
1	Port $P0_1$, $P0_2$ drive capacity bit	0: Low 1: High	0	RW
2	Port $P0_3$-$P0_7$ drive capacity bit	0: Low 1: High	0	RW
3	Port $P3_0$ drive capacity bit	0: Low 1: High	0	RW
4	Port $P3_1$, $P3_2$ drive capacity bit	0: Low 1: High	0	RW
5	Port $P3_3$ drive capacity bit	0: Low 1: High	0	RW
6	Port $P3_4$ drive capacity bit	0: Low 1: High	0	RW
7	Port $P3_7$ drive capacity bit	0: Low 1: High	0	RW

Note: The maximum number of available ports (drive capacity: High) is eight.

Fig. 4.18 Configuration of Port P0P3 drive capacity control register

Pull-up control register

b7 b6 b5 b4 b3 b2 b1 b0

Pull-up control register (PULL)

[Address 16h]

b	Name	Function	After Reset	RW
0	$P0_0$ pull-up control bit	0: Pull-up Off 1: Pull-up On	0	RW
1	$P0_1$, $P0_2$ pull-up control bit	0: Pull-up Off 1: Pull-up On	0	RW
2	$P0_3$-$P0_7$ pull-up control bit	0: Pull-up Off 1: Pull-up On	0	RW
3	$P3_0$ pull-up control bit	0: Pull-up Off 1: Pull-up On	0	RW
4	$P3_1$, $P3_2$ pull-up control bit	0: Pull-up Off 1: Pull-up On	0	RW
5	$P3_3$ pull-up control bit	0: Pull-up Off 1: Pull-up On	0	RW
6	$P3_4$ pull-up control bit	0: Pull-up Off 1: Pull-up On	0	RW
7	$P3_7$ pull-up control bit	0: Pull-up Off 1: Pull-up On	0	RW

Note: The pin set to output mode is disconnected from pull-up control.

Fig. 4.19 Configuration of Pull-up control register

Port P1P3 control register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 0 0 0

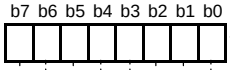
Port P1P3 control register (P1P3C)

[Address 17h]

b	Name	Function	After Reset	RW
0	$P3_7$/INT_0 input level selection bit	0: CMOS level 1: TTL level	0	RW
1	If necessary, set to 0.		0	RW
2	$P1_0$,$P1_2$,$P1_3$ input level selection bit	0: CMOS level 1: TTL level	0	RW
3	When read, the content is 0. If necessary, set to 0.		0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.20 Configuration of Port P1P3 control register

Transmit buffer register 1



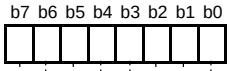
Transmit buffer register 1 (TB1)

[Address 18h]

b	Function	After Reset	RW
0	The transmission data is written to this buffer register. Write transmission data to this register.	Undefined	WO
1		Undefined	WO
2		Undefined	WO
3		Undefined	WO
4		Undefined	WO
5		Undefined	WO
6		Undefined	WO
7		Undefined	WO

Note: This register is assigned to the same address as the receive buffer register. Unreadable.

Receive buffer register 1



Receive buffer register 1 (RB1)

[Address 18h]

b	Function	After Reset	RW
0	The receive data is read from this buffer register. Read receive data from this register.	Undefined	RO
1		Undefined	RO
2		Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

Note: This register is assigned to the same address as the transmit buffer register. Unwritable.

Fig.4.21 Configuration of Transmit buffer register 1/Receive buffer register 1

Serial I/O1 status register

b7 b6 b5 b4 b3 b2 b1 b0

1 | | | | | | | |

Serial I/O1 status register (SIO1STS)

[Address 19h]

b	Name	Function	After Reset	RW
0	Transmit buffer empty flag (TBE)	0: Buffer full 1: Buffer empty	0	RO
1	Receive buffer full flag (RBF) (Note 1, 2)	0: Buffer empty 1: Buffer full	0	RO
2	Transmit shift completion flag (TSC)	0: Transmit shift in progress 1: Transmit shift completed	0	RO
3	Overrun error flag (OE) (Note 3)	0: No error 1: Overrun error	0	RO
4	Parity error flag (PE) (Note 3)	0: No error 1: Parity error	0	RO
5	Parity error flag (FE) (Note 3)	0: No error 1: Framing error	0	RO
6	Summing error flag (SE) (Note 3)	0: (OE)U(PE)U(FE) = 0 1: (OE)U(PE)U(FE) = 1	0	RO
7	When read, the content is 1. If necessary, set to 1.		1	RO

Notes 1: If necessary, set to 0.
2: This flag is cleared to 0 by reading the receive buffer register.
3: This flag is cleared to 0 by writing to this register. If necessary, set to 0.

Fig. 4.22 Configuration of Serial I/O1 status register

Serial I/O1 control register

b7 b6 b5 b4 b3 b2 b1 b0

| | | | | | | | |

Serial I/O1 control register (SIO1CON)

[Address 1Ah]

b	Name	Function	After Reset	RW
0	BRG count source selection bit (CSS)	0: f(X_{IN}) 1: f(X_{IN})/4	0	RW
1	Serial I/O1 synchronous clock selection bit (SCS)	0: BRG output divided by 4 when clock synchronous serial I/O is selected, BRG output divided by 16 when UART is selected. 1: External clock input when clock synchronous serial I/O is selected, external clock input divided by 16 when UART is selected.	0	RW
2	$\overline{SRDY1}$ output enable bit (SRDY)	0: Out put disabled (P13 pin as I/O port) 1: Output enabled (P13 pin as $\overline{SRDY1}$ output pin)	0	RW
3	Transmit interrupt source selection bit (TIC)	0: Interrupt when transmit buffer has emptied (TBE = 1) 1: Interrupt when transmit shift operation is completed (TSC = 1)	0	RW
4	Transmit enable bit (TE)	0: Transmit disabled 1: Transmit enabled	0	RW
5	Receive enable bit (RE)	0: Receive disabled 1: Receive enabled	0	RW
6	Serial I/O1 mode selection bit (SIOM)	0: Clock asynchronous (UART) serial I/O 1: Clock synchronous serial I/O	0	RW
7	Serial I/O1 enable bit (SIOE)	0: Serial I/O1 disabled (pins $P1_0$ to $P1_3$ as I/O pins) 1: Serial I/O1 enabled (pins $P1_0$ to $P1_3$ as serial I/O pins)	0	RW

Fig. 4.23 Configuration of Serial I/O1 control register

UART1 control register

b7 b6 b5 b4 b3 b2 b1 b0

1 1 1 | | | | | |

UART1 control register (UART1CON)

[Address 1Bh]

b	Name	Function	After Reset	RW
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	RW
1	Parity enable bit (PARE)	0: Parity check disabled 1: Parity check enabled	0	RW
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	RW
3	Stop bit length selection bit (STPS)	0:1 stop bit 1: 2 stop bits	0	RW
4	$P1_1$/TXD_1 P-channel output disable bit (POFF)	0: CMOS output (in output mode) 1: N-channel open drain output (in output mode) In input mode, this bit is disabled.	0	RW
5	When read, the content is 0. If necessary, set to 0.		1	RO
6			1	RO
7			1	RO

Fig. 4.24 Configuration of UART1 control register

Baud rate generator 1

b7 b6 b5 b4 b3 b2 b1 b0

| | | | | | | | |

Baud rate generator 1 (BRG1)

[Address 1Ch]

b	Name	Function	After Reset	RW
0	Set the divided value of the BRG count source.		Undefined	RW
1	The baud rate generator divides the frequency of the count source by		Undefined	RW
2	1/(n+1), where n is the value written to the baud rate generator.		Undefined	RW
3			Undefined	RW
4			Undefined	RW
5			Undefined	RW
6			Undefined	RW
7			Undefined	RW

Note: Only write to this register while transmit/receive operation is stopped.

Fig.4.25 Configuration of Baud rate generator 1

Timer A, B mode register

b7 b6 b5 b4 b3 b2 b1 b0

0 0

Timer A, B mode register (TABM)

[Address 1Dh]

b	Name	Function	After Reset	RW
0	Timer A write control bit	0: Write to latch and timer simultaneously 1: Write to only latch	0	RW
1	Timer A count stop bit	0: Count start 1: Count stop	0	RW
2	Timer B write control bit	0: Write to latch and timer simultaneously 1: Write to only latch	0	RW
3	Timer B count stop bit	0: Count start 1: Count stop	0	RW
4	When read, the content is 0. If necessary, set to 0.		0	RO
5			0	RO
6	Compare 0, 1 modulation mode bit	0: Disabled 1: Enabled	0	RW
7	Compare 2, 3 modulation mode bit	0: Disabled 1: Enabled	0	RW

Note: When the timer A (B) write control bit is set to 1 "write to only latch", written data to timer register is set to only the latch even if the timer is stopped. To set the initial value to the timer while it is stopped, set the timer A (B) write control bit to 0 "write to latch and timer simultaneously" beforehand.

Fig.4.26 Configuration of Timer A, B mode register

Capture/Compare port register

b7 b6 b5 b4 b3 b2 b1 b0

0

Capture/Compare port register (CCPR)

[Address 1Eh]

b	Function		After Reset	RW
0	Capture 0 input port bits	b1 b0 0 0: Capture from $P0_0$ 0 1: Capture from $P1_0$ 1 0: Ring/512 1 1: Not available	0	RW
1			0	RW
2	Compare 0 output port bit	0: $P0_1$ is I/O port 1: $P0_1$ is Compare 0	0	RW
3	Compare 1 output port bit	0: $P0_2$ is I/O port 1: $P0_2$ is Compare 1	0	RW
4	Capture 1 input port bit	0: Capture from $P3_0$ 1: Ring/512	0	RW
5	Compare 2 output port bit	0: $P3_1$ is I/O port 1: $P3_1$ is Compare 2	0	RW
6	Compare 3 output port bit	0: $P3_2$ is I/O port 1: $P3_2$ is Compare 3	0	RW
7	When read, the content is 0. If necessary, set to 0.		0	RO

Fig.4.27 Configuration of Capture/Compare port register

Timer source selection register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 | | | | | | |

Timer source selection register (TMSR)

[Address 1Fh]

b	Name	Function	After Reset	RW
0	Compare 0 timer source bit	0: Timer A 1: Timer B	0	RW
1	Compare 1 timer source bit	0: Timer A 1: Timer B	0	RW
2	Compare 2 timer source bit	0: Timer A 1: Timer B	0	RW
3	Compare 3 timer source bit	0: Timer A 1: Timer B	0	RW
4	Capture 0 timer source bit	0: Timer A 1: Timer B	0	RW
5	Capture 1 timer source bit	0: Timer A 1: Timer B	0	RW
6	When read, the content is 0. If necessary, set to 0.		0	RO
7			0	RO

Notes 1: Timer A cannot be used as the capture input source timer in the following:
CPU operating clock source: X_{IN} oscillation
Timer A count source: On-chip oscillator output
2: Timer B cannot be used as the capture input source timer in the following:
CPU operating clock source: X_{IN} oscillation
Timer B count source: Timer A underflow
Timer A count source: On-chip oscillator output

Fig.4.28 Configuration of Timer source selection register

Capture mode register

b7 b6 b5 b4 b3 b2 b1 b0

| | | | | | | | |

Capture mode register (CAPM)

[Address 20h]

b	Function		After Reset	RW
0	Capture 0 interrupt edge selection bits	b1 b0 0 0: Rising and falling edge 0 1: Rising edge 1 0: Falling edge 1 1: Not available	0	RW
1			0	RW
2	Capture 1 interrupt edge selection bits	b3 b2 0 0: Rising and falling edge 0 1: Rising edge 1 0: Falling edge 1 1: Not available	0	RW
3			0	RW
4	Capture 0 noise filter clock selection bits	b5 b4 0 0: No filter 0 1: f(X_{IN}) 1 0: f(X_{IN})/8 1 1: f(X_{IN})/32	0	RW
5			0	RW
6	Capture 1 noise filter clock selection bits	b7 b6 0 0: No filter 0 1: f(X_{IN}) 1 0: f(X_{IN})/8 1 1: f(X_{IN})/32	0	RW
7			0	RW

Notes 1: When setting the interrupt edge selection bit and noise filter clock selection bit of the external interrupt CAP0, CAP1, the interrupt request bit may be set to 1.
If no interrupt synchronized with these settings is necessary,
perform the following procedure:
(1) Set the corresponding interrupt enable bit to 0 (disabled).
(2) Set the interrupt edge selection bit or noise filter clock selection bit.
(3) Set the corresponding interrupt request bit to 0 after one or more instructions have been executed.
(4) Set the corresponding interrupt enable bit to 1 (enabled).
2: When the capture interrupt is used as the interrupt for return from stop mode, set the capture x noise filter clock selection bits to 00 "no filter" (x = 0 or 1).

Fig.4.29 Configuration of Capture mode register

Compare output mode register

b7 b6 b5 b4 b3 b2 b1 b0

Compare output mode register (CMOM)

[Address 21h]

b	Name	Function	After Reset	RW
0	Compare 0 output level latch	0: Positive 1: Negative	0	RW
1	Compare 1 output level latch	0: Positive 1: Negative	0	RW
2	Compare 2 output level latch	0: Positive 1: Negative	0	RW
3	Compare 3 output level latch	0: Positive 1: Negative	0	RW
4	Compare 0 trigger enable bit	0: Disabled 1: Enabled	0	RW
5	Compare 1 trigger enable bit	0: Disabled 1: Enabled	0	RW
6	Compare 2 trigger enable bit	0: Disabled 1: Enabled	0	RW
7	Compare 3 trigger enable bit	0: Disabled 1: Enabled	0	RW

Note: When the compare x trigger enable bit is cleared to 0 (disabled), a match trigger to the waveform output circuit is disabled, and the output waveform can be fixed to "L" or "H" level. However, a compare match signal is generated even in this condition, allowing a compare match interrupt to occur (x = 0, 1, 2, 3).

Fig.4.30 Configuration of Compare output mode register

Capture/Compare status register

b7 b6 b5 b4 b3 b2 b1 b0

0 0

Capture/Compare status register (CCSR)

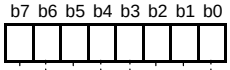
[Address 22h]

b	Function		After Reset	RW
0	Compare 0 output status bit	0: "L" level output 1: "H" level output	0	RW
1	Compare 1 output status bit	0: "L" level output 1: "H" level output	0	RW
2	Compare 2 output status bit	0: "L" level output 1: "H" level output	0	RW
3	Compare 3 output status bit	0: "L" level output 1: "H" level output	0	RW
4	Capture 0 status bit	0: Latch 00 captured 1: Latch 01 captured	0	RW
5	Capture 1 status bit	0: Latch 10 captured 1: Latch 11 captured	0	RW
6	When read, the content is 0. If necessary, set to 0.		0	RO
7			0	RO

Note: The compare output status ("H"/"L" level) can be confirmed by reading the compare x output status bit (x = 0, 1, 2, 3).

Fig.4.31 Configuration of Capture/Compare status register

Compare interrupt source register



Compare interrupt source register (CISR)

[Address 23h]

b	Name	Function	After Reset	RW
0	Compare latch 00 interrupt source bit	0: Disabled 1: Enabled	0	RW
1	Compare latch 01 interrupt source bit	0: Disabled 1: Enabled	0	RW
2	Compare latch 10 interrupt source bit	0: Disabled 1: Enabled	0	RW
3	Compare latch 11 interrupt source bit	0: Disabled 1: Enabled	0	RW
4	Compare latch 20 interrupt source bit	0: Disabled 1: Enabled	0	RW
5	Compare latch 21 interrupt source bit	0: Disabled 1: Enabled	0	RW
6	Compare latch 30 interrupt source bit	0: Disabled 1: Enabled	0	RW
7	Compare latch 31 interrupt source bit	0: Disabled 1: Enabled	0	RW

Note: A compare output interrupt can be generated when the values of the compare latch and the timer count match.
An interrupt request signal from each compare latch can be disabled or enabled by setting the compare latch y interrupt source bit (y = 00, 01, 10, 11, 20, 21, 30, 31).

Fig.4.32 Configuration of Compare interrupt source register

Timer A high-order register, Timer A low-order register

b7 b6 b5 b4 b3 b2 b1 b0

Timer A high-order register (TAH), Timer A low-order register (TAL)

[Addresses 25h, 24h]

b	Name	Function	After Reset	RW
0	Set the timer A count value.		1	RW
1	[Write]		1	RW
2	Writing to "latch only" or "latch and timer A" can be selected by		1	RW
3	the setting value of the timer A write control bit.		1	RW
4	Write to the both registers in the order from TAL to TAH.		1	RW
5	[Read]		1	RW
6	The timer A count value is read by reading these registers.		1	RW
7	Read from the both registers in the order from TAL to TAH.		1	RW

Note: Write to/read from timer A while it is stopped in the following:
- CPU operating clock source: XIN oscillation
- Timer A count source: On-chip oscillator output

Fig.4.33 Configuration of Timer A high-order register, Timer A low-order register

Timer B high-order register, Timer B low-order register

b7 b6 b5 b4 b3 b2 b1 b0

Timer B high-order register (TBH), Timer B low-order register (TBL)

[Addresses 27h, 26h]

b	Name	Function	After Reset	RW
0	Set the timer B count value.		1	RW
1	[Write]		1	RW
2	Writing to "latch only" or "latch and timer B" can be selected by		1	RW
3	the setting value of the timer B write control bit.		1	RW
4	Write to the both registers in the order from TBL to TBH.		1	RW
5	[Read]		1	RW
6	The count value of timer B is read by reading this register.		1	RW
7	Read from the both registers in the order from TBH to TBL.		1	RW

Note: Write to/read from timer B while it is stopped in the following:
- CPU operating clock source: XIN oscillation
- Timer B count source: Timer A underflow
- Timer A count source: On-chip oscillator output

Fig.4.34 Configuration of Timer B high-order register, Timer B low-order register

Prescaler 1

b7 b6 b5 b4 b3 b2 b1 b0

Prescaler 1 (PRE1)

[Address 28h]

b	Name	Function	After Reset	RW
0	Set the prescaler 1 count value.		1	RW
1	[Write]		1	RW
2	Write data to both the timer 1 latch and timer 1 simultaneously.		1	RW
3	[Read]		1	RW
4	The count value of prescaler 1 is read by reading this register.		1	RW
5			1	RW
6			1	RW
7			1	RW

Fig.4.35 Configuration of Prescaler 1

Timer 1 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 1 register (T1)

[Address 29h]

b	Function	After Reset	RW
0	Set the timer 1 count value.	1	RW
1	[Write]	0	RW
2	Write data to both the timer 1 latch and timer 1 simultaneously.	0	RW
3	[Read]	0	RW
4	The count value of timer 1 is read by reading this register.	0	RW
5		0	RW
6		0	RW
7		0	RW

Fig.4.36 Configuration of Timer 1 register

Timer count source set register

b7 b6 b5 b4 b3 b2 b1 b0

Timer count source set register (TCSS)

[Address 2Ah]

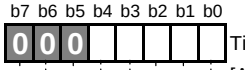
b	Name	Function	After Reset	RW
0	Timer X count source selection bits	b1b0 0 0: f(XIN)/16 0 1: f(XIN)/2 1 0: f(XIN) (Note 1) 1 1: Not available	0	RW
1			0	RW
2	Timer A count source selection bits	b4 b3 b2 0 0 0: f(XIN)/16 0 0 1: f(XIN)/2 0 1 0: f(XIN)/32 0 1 1: f(XIN)/64 1 0 0: f(XIN)/128 1 0 1: f(XIN)/256 1 1 0: On-chip oscillator output (Note 2) 1 1 1: Not available	0	RW
3			0	RW
4			0	RW
5	Timer B count source selection bits	b7 b6 b5 0 0 0: f(XIN)/16 0 0 1: f(XIN)/2 0 1 0: f(XIN)/32 0 1 1: f(XIN)/64 1 0 0: f(XIN)/128 1 0 1: f(XIN)/256 1 1 0: Timer A underflow 1 1 1: Not available	0	RW
6			0	RW
7			0	RW

Notes 1: f(XIN) can be selected as the timer X count source when a ceramic or on-chip oscillator is used. Do not select $f(X_{IN})$ when an RC oscillator is used.

2: The on-chip oscillator is used as the count source by setting the oscillation enabled by the on-chip oscillation control bit (bit 3) in the CPU mode register (CPUM).

Fig.4.37 Configuration of Timer count source set register

Timer X mode register



Timer X mode register (TXM)
[Address 2Bh]

b	Name	Function	After Reset	RW
0	Timer X operating mode bits	b1 b0 0 0: Timer mode 0 1: Pulse output mode 1 0: Event counter mode 1 1: Pulse width measurement mode	0	RW
1			0	RW
2	CNTR0 active edge switch bit	The function depends on the operating mode of Timer X. (Refer to Table 4.1.)	0	RW
3	Timer X count stop bit	0: Count start 1: Count stop	0	RW
4	P03/TXOUT output enable bit	0: Output disabled (I/O port) 1: Output enabled (inverted CNTR0 output)	0	RW
5	When read, the content is 0. If necessary, set to 0.		0	RO
6			0	RO
7			0	RO

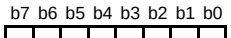
Note: When setting the CNTR0 active edge switch bit, the interrupt request bit may be set to 1.
If no interrupt synchronized with this setting is necessary,
perform the following procedure:
(1) Set the corresponding interrupt enable bit to 0 (disabled).
(2) Set the active edge switch bit.
(3) Set the corresponding interrupt request bit to 0 after 1 or more instructions have been executed.
(4) Set the corresponding interrupt enable bit to 1 (enabled).

Fig.4.38 Configuration of Timer X mode register

Table 4.2 CNTR0 active edge switch bit function

Timer X operation mode	Set value	Timer function selection	CNTR0 interrupt request occurrence source
Timer mode	0	—	CNTR0 input signal falling edge (no influence to timer count)
	1	—	CNTR0 input signal rising edge (no influence to timer count)
Pulse output mode	0	Pulse output start from "H"	Output signal falling edge
	1	Pulse output start from "L"	Output signal rising edge
Event counter mode	0	Count at rising edge	Input signal falling edge
	1	Count at falling edge	Input signal rising edge
Pulse width measurement mode	0	Measure "H" pulse width	Input signal falling edge
	1	Measure "L" pulse width	Input signal rising edge

Prescaler X



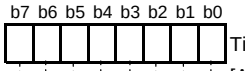
Prescaler X (PREX)

[Address 2Ch]

b	Name	Function	After Reset	RW
0	Set the prescaler X count value.		1	RW
1	[Write]		1	RW
2	The setting value of this register is written to both		1	RW
3	prescaler X and the prescaler X latch.		1	RW
4	[Read]		1	RW
5	The count value of prescaler X is read by reading this register.		1	RW
6			1	RW
7			1	RW

Fig.4.39 Configuration of Prescaler X

Timer X register



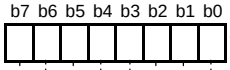
Timer X register (TX)

[Address 2Dh]

b	Function	After Reset	RW
0	Set the timer X count value.	1	RW
1	[Write]	1	RW
2	The setting value of this register is written to both	1	RW
3	timer X and the timer X latch.	1	RW
4	[Read]	1	RW
5	The count value of timer X is read by reading this register.	1	RW
6		1	RW
7		1	RW

Fig.4.40 Configuration of Timer X register

Transmit buffer register 2



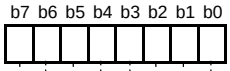
Transmit buffer register 2 (TB2)

[Address 2Eh]

b	Function	After Reset	RW
0	The transmission data is written to this buffer register.	Undefined	WO
1	Write transmission data to this register.	Undefined	WO
2		Undefined	WO
3		Undefined	WO
4		Undefined	WO
5		Undefined	WO
6		Undefined	WO
7		Undefined	WO

Note: This register is assigned to the same address as the receive buffer register. Unreadable.

Receive buffer register 2



Receive buffer register 2 (RB2)

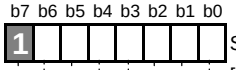
[Address 2Eh]

b	Function	After Reset	RW
0	The receive data is read from this buffer register.	Undefined	RO
1	Read receive data from this register.	Undefined	RO
2		Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

Note: This register is assigned to the same address as the transmit buffer register. Unwritable.

Fig.4.41 Configuration of Transmit buffer register 2/Receive buffer register 2

Serial I/O2 status register



Serial I/O2 status register (SIO2STS)

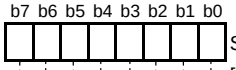
[Address 2Fh]

b	Name	Function	After Reset	RW
0	Transmit buffer empty flag (TBE) (Note 1)	0: Buffer register full 1: Buffer register empty	0	RO
1	Receive buffer full flag (RBF) (Notes 1, 2)	0: Buffer register empty 1: Buffer register full	0	RO
2	Transmit shift completion flag (TSC)(Note1)	0: Transmit shift in progress 1: Transmit shift completed	0	RO
3	Overrun error flag (OE) (Note 3)	0: No error 1: Overrun error	0	RO
4	Parity error flag (PE) (Note 3)	0: No error 1: Parity error	0	RO
5	Framing error flag (FE) (Note 3)	0: No error 1: Framing error	0	RO
6	Summing error flag (SE) (Note 3)	0: (OE)U(PE)U(FE) = 0 1: (OE)U(PE)U(FE) = 1	0	RO
7	When read, the content is 1. If necessary, set to 1.		1	RO

Notes 1: If necessary, set to 0.
2: This bit is set to 0 by reading the receive buffer register.
3: This bit is set to 0 by writing to this register. If necessary, set to 0.

Fig.4.42 Configuration of Serial I/O2 status register

Serial I/O2 control register



Serial I/O2 control register (SIO2CON)

[Address 30h]

b	Name	Function	After Reset	RW
0	BRG count source selection bit (CSS)	0: f(XIN) 1: f(XIN)/4	0	RW
1	Serial I/O synchronous clock selection bit (SCS)	0: BRG output divided by 4 when clock synchronous serial I/O is selected, BRG output divided by 16 when UART is selected. 1: External clock input when clock synchronous serial I/O is selected, external clock input divided by 16 when UART is	0	RW
2	$\overline{SRDY2}$ output enable bit (SRDY)	0: Output disabled (P07 pin as I/O port) 1: Output enabled (P07 pin as $\overline{SRDY2}$ output pin)	0	RW
3	Transmit interrupt source selection bit (TIC)	0: Interrupt when transmit buffer has emptied (TBE = 1) 1: Interrupt when transmit shift operation is completed (TSC = 1)	0	RW
4	Transmit enable bit (TE)	0: Transmit disabled 1: Transmit enabled	0	RW
5	Receive enable bit (RE)	0: Receive disabled 1: Receive enabled	0	RW
6	Serial I/O mode selection bit (SIOM)	0: Clock asynchronous (UART) serial I/O 1: Clock synchronous serial I/O	0	RW
7	Serial I/O2 enable bit (SIOE)	0: Serial I/O2 disabled (pins P04 to P07 as I/O pins) 1: Serial I/O2 enabled (pins P04 to P07 as serial I/O pins)	0	RW

Fig.4.43 Configuration of Serial I/O2 control register

UART2 control register

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	0				

UART2 control register (UART2CON)

[Address 31h]

b	Name	Function	After Reset	RW
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	RW
1	Parity enable bit (PARE)	0: Parity checking disabled 1: Parity checking enabled	0	RW
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	RW
3	Stop bit length selection bit (STPS)	0:1 stop bit 1: 2 stop bits	0	RW
4	When read, the content is 0. If necessary, set to 0. Do not set to 1.		0	RW
5	When read, the content is 1. If necessary, set to 1.		1	RO
6			1	RO
7			1	RO

Fig.4.44 Configuration of UART2 control register

Baud rate generator 2

b7	b6	b5	b4	b3	b2	b1	b0

Baud rate generator 2 (BRG2)

[Address 32h]

b	Name	Function	After Reset	RW
0	Set the divided value of BRG count source. The baud rate generator divides the frequency of the count source by 1/(n+1), where n is the value written to the baud rate generator.		Undefined	RW
1			Undefined	RW
2			Undefined	RW
3			Undefined	RW
4			Undefined	RW
5			Undefined	RW
6			Undefined	RW
7			Undefined	RW

Note: Only write to this register while transmit/receive operation is stopped.

Fig.4.45 Configuration of Baud rate generator 2

A/D control register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 | | | | | |

A/D control register (ADCON)

[Address 34h]

b	Name	Function	After Rese	RW
0	Analog input pin selection bits	b2 b1 b0 0 0 0: AN_0 0 0 1: AN_1 0 1 0: AN_2 0 1 1: AN_3 1 0 0: AN_4 1 0 1: AN_5 1 1 0: Not available 1 1 1: Not available	0	RW
1			0	RW
2			0	RW
3	A/D conversion clock selection bit (Note)	0: $f(X_{IN})/2$ 1: $f(X_{IN})$	0	RW
4	AD conversion completion bit	0: Conversion in progress 1: Conversion completed	1	RW
5	When read, the content is 0. If necessary, set to 0.		0	RO
6			0	RO
7			0	RO

Note: The A/D conversion clock = $f(X_{IN})$ can be selected only when a ceramic or on-chip oscillator is used. Select $f(X_{IN})/2$ when an RC oscillator is used.

Fig.4.46 Configuration of A/D control register

A/D conversion low-order register

b7 b6 b5 b4 b3 b2 b1 b0

A/D conversion low-order register (ADL)

[Address 35h]

b	Name	Function	After Reset	RW
0	The A/D conversion register is a read-only register that stores the result of A/D conversion.	At 8-bit read (read only address 0035h) b7 b0 b9 b8 b7 b6 b5 b4 b3 b2 At 10-bit read (read in the order from address 0036h, 0035h) b7 b0 b7 b6 b5 b4 b3 b2 b1 b0	Undefined	RO
1			Undefined	RO
2			Undefined	RO
3			Undefined	RO
4			Undefined	RO
5			Undefined	RO
6			Undefined	RO
7			Undefined	RO

Fig.4.47 Configuration of A/D conversion low-order register

A/D conversion high-order register

b7 b6 b5 b4 b3 b2 b1 b0

A/D conversion high-order register (ADH)

[Address 36h]

b	Function	After Reset	RW
0	The A/D conversion register is a read-only register that stores the result of A/D conversion. At 10-bit read b7 b0 (b9 b8)	Undefined	RO
1		Undefined	RO
2	When read, the content is 0.	Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

Note: At 10-bit read, read in the order from address 0036h, 0035h.

Fig.4.48 Configuration of A/D conversion high-order register

On-chip oscillation division ratio selection register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

On-chip oscillation division ratio selection register (RODR)

[Address 37h]

b	Function		After Reset	RW
0	On-chip oscillator division ratio selection bits	b1 b0 0 0: On-chip oscillator double-speed mode (ROSC/1) 0 1: On-chip oscillator high-speed mode (ROSC/2)	0	RW
1		1 0: On-chip oscillator middle-speed mode (ROSC/8) 1 1: On-chip oscillator low-speed mode (ROSC/128)	1	RW
2	When read, the content is 0. If necessary, set to 0.		0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Fig.4.49 Configuration of On-chip oscillation division ratio selection register

MISRG

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

MISRG register (MISRG)

[Address 38h]

b	Name	Function	After Reset	RW
0	Oscillation stabilization time set bit after release of the STP instruction	0: Set 01h in timer 1, and FFh in prescaler 1 automatically 1: Not set automatically	0	RW
1	Ceramic/quartz-crystal or RC oscillation stop detection function active bit	0: Detection function inactive 1: Detection function active	0	RW
2	Oscillation stop reset bit	0: Oscillation stop reset disabled 1: Oscillation stop reset enabled	0	RW
3	Oscillation stop detection status bit	0: Oscillation stop not detected 1: Oscillation stop detected	0	RW
4	When read, the content is 0. If necessary, set to 0.		0	RO
5	Reserved bits. If necessary, set to 0.		0	RW
6	Do not set to 1.		0	RW
7			0	RW

Notes 1: The ceramic or RC oscillation stop detection function active bit is not initialized by the oscillation stop internal reset.
This allows the oscillation stop detection circuit to be in active when the MCU is returned from a reset occurred on oscillation stop detection.

2: The oscillation stop detection status bit is initialized in the following:
- External reset
- Write 0 to the ceramic or RC oscillation stop detection function active bit

3: The oscillation stop detection circuit is not included in the emulator MCU “M37542RSS”.

Fig.4.50 Configuration of MISRG

Watchdog timer control register

b7 b6 b5 b4 b3 b2 b1 b0

Watchdog timer control register (WDTCON)

[Address 39h]

b	Name	Function	After Reset	RW
0	Watchdog timer H (read only for high-order 6-bit)		1	RO
1			1	RO
2			1	RO
3			1	RO
4			1	RO
5			1	RO
6	STP instruction function selection bit (Note 1)	0: Enter to stop mode at STP instruction execution 1: Internal reset at STP instruction execution	0	RW
7	Watchdog timer H count source selection bit (Note 2)	0: Watchdog timer L underflow 1: On-chip oscillator/16 or f(XIN)/16 (Note 3)	0	RW

Notes 1: This bit can be written to only once after releasing reset. After writing, a write to this bit is disabled because it is locked.
The function of this bit can also be set using bit 3 of the function set ROM data 2 (FSROM2).
If used, this bit value is fixed to the same as the bit 3 value and cannot be changed by a program.
Also, a value set by bit 3 changes the initial value of this bit after reset.

2: The function of this bit can also be set using bit 2 of FSROM2.
If used, this bit value is fixed to the same as the bit 2 value and cannot be changed by a program.
Also, a value set by bit 2 changes the initial value of this bit after reset.

3: When double-speed mode, high-speed mode, or middle-speed mode is selected by the clock division ratio selection bits (bits 7, 6 in CPU mode register), the count source clock of the watchdog timer H is set to f(XIN)/16.
When the supply from on-chip oscillator is selected, it is set to the on-chip oscillator output/16.

4: After reset, this register sets the watchdog timer to FFFFh and start counting.
Counting can be automatically started by bit 1 of FSROM2 after reset.

Fig.4.51 Configuration of Watchdog timer control register

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 1

Interrupt edge selection register (INTEDGE)

[Address 3Ah]

b	Name	Function	After Reset	RW
0	INT_0 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
1	Always set to 1.	0: Falling edge active 1: Rising edge active	0	RW
2	Set 1 to this bit certainly.		0	RW
3	When read, the content is 0. If necessary, set to 0.		0	RO
4			0	RO
5	$P0_0$ key-on wakeup enable bit	0: Key-on wakeup enabled 1: Key-on wakeup disabled	0	RW
6	$P0_4$ key-on wakeup enable bit	0: Key-on wakeup enabled 1: Key-on wakeup disabled	0	RW
7	$P0_6$ key-on wakeup enable bit	0: Key-on wakeup enabled 1: Key-on wakeup disabled	0	RW

Fig.4.52 Configuration of Interrupt edge selection register

CPU mode register

b7 b6 b5 b4 b3 b2 b1 b0

CPU mode register (CPUM)

[Address 3Bh]

b	Name	Function	After Reset	RW
0	Processor mode bits (Note 1)	b1 b0 0 0: Single-chip mode 0 1: Not available 1 0: Not available 1 1: Not available	0	RW
1			0	RW
2	Stack page selection bit	0: 0 page 1:1 page	0	RW
3	On-chip oscillator oscillation control bit (Note 2)	0: On-chip oscillator oscillation enabled 1: On-chip oscillator oscillation stop	0	RW
4	X_{IN} oscillation control bit	0: Ceramic or RC oscillation enabled 1: Ceramic or RC oscillation stop	0	RW
5	Oscillation mode selection bit (Note 1, Note 3)	0: Ceramic oscillation 1: RC oscillation	0	RW
6	Clock division ratio selection bits	b7 b6 0 0: f(φ) = f(X_{IN})/2 (high-speed mode) 0 1: f(φ) = f(X_{IN})/8 (middle-speed mode) 1 0: Supply from on-chip oscillator 1 1: f(φ) = f(X_{IN}) (double-speed mode) (Note 4)	0	RW
7			1	RW

Notes 1: This bit can be written to only once after releasing reset. After writing, a write to this bit is disabled because it is locked. A reset initializes this bit and enables rewriting.
(This bit is not locked when the emulator MCU "M37542RSS" is used.)

2: This bit value can be fixed to 0 using bit 4 of the function set ROM data 2 (FSROM2).
This condition disables writing 1 and keeps the on-chip oscillator operating.
The oscillation does not stop even in stop mode, increasing the current consumption in the mode.

3: The function of this bit can also be set using bit 5 of FSROM2.
If used, this bit value is fixed to the same as the bit 5 value and cannot be changed by a program.
Also, a value set by bit 5 changes the initial value of this bit after reset.

4: Available only when a ceramic oscillator is selected.
Do not use when an RC oscillator is selected.

Fig.4.53 Configuration of CPU mode register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1)

[Address 3Ch]

b	Name	Function	After Reset	RW
0	Serial I/O1 receive interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
1	Serial I/O1 transmit interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
2	Serial I/O2 receive interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
3	Serial I/O2 transmit interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
4	INT_0 interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
5	INT_1 interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
6	Key-on wake up/UART1 bus collision detection interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
7	$CNTR_0$ interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)

Note: This bit can be set to 0, but not to 1 by a program.

Fig.4.54 Configuration of Interrupt request register 1

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2 (IREQ2)

[Address 3Dh]

b	Name	Function	After Reset	RW
0	Capture 0 interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
1	Capture 1 interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
2	Compare interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
3	Timer X interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
4	Timer A interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
5	Timer B interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
6	A/D conversion/Timer 1 interrupt request bit	0: No interrupt request 1: Interrupt requested	0	RW (Note)
7	When read, the content is 0. If necessary, set to 0.		0	RO

Note: This bit can be set to 0, but not to 1 by a program.

Fig.4.55 Configuration of Interrupt request register 2

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1)

[Address 3Eh]

b	Name	Function	After Reset	RW
0	Serial I/O1 receive interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
1	Serial I/O1 transmit interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
2	Serial I/O2 receive interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
3	Serial I/O2 transmit interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
4	INT_0 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
5	INT_1 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
6	Key-on wake up/UART1 bus collision detection interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
7	$CNTR_0$ interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW

Fig.4.56 Configuration of Interrupt control register 1

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

Interrupt control register 2 (ICON2)

[Address 3Fh]

b	Name	Function	After Reset	RW
0	Capture 0 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
1	Capture 1 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
2	Compare interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
3	Timer X interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
4	Timer A interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
5	Timer B interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
6	A/D conversion/Timer 1 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
7	If necessary, set to 0. Do not set to 1.		0	RW

Fig.4.57 Configuration of Interrupt control register 2

The function set ROM data 0, 1 and 2 are used to set peripheral functions by writing data to QzROM and cannot be set by a program.
Data written to these areas become valid after releasing reset.
Regardless of the use of peripheral functions, always set a value according to the system.

Function set ROM data 0

b7	b6	b5	b4	b3	b2	b1	b0
1	0	0	0		0		

Function set ROM data 0 (FSROM0)

[Address FFD8h]

b	Name	Function
0	Function set ROM disable bit (Note 1)	0: Setting of bit 5 to bit 0 of function set ROM data 2 enabled 1: Setting of bit 5 to bit 0 of function set ROM data 2 disabled
1	Low voltage detection circuit enable bit	0: Low voltage detection circuit disabled 1: Low voltage detection circuit enabled
2	Set 0 to this bit certainly.	
3	Low voltage detection circuit disable bit in the stop mode (Note 2)	0: Low voltage detection circuit enabled in stop mode 1: Low voltage detection circuit disabled in stop mode
4	Set to 0.	
5		
6		
7	Set to 1.	

Notes 1: When 1 is set to this bit, the setting values of bit 5 to bit 0 of the function ROM data 2 (FSROM2) become invalid. These functions can be set by a program.
(This bit does not affect on bits other than bit 5 to bit 0 of FSROM2)
2: When the low voltage detection circuit is set to be enabled in stop mode, the current consumption in the mode increases.

Fig.4.58 Configuration of Function set ROM data 0

Function set ROM data 1

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0

Function set ROM data 1 (FSROM1)

[Address FFD9h]

b	Function
0	Set to 0.
1	
2	
3	
4	
5	
6	
7	

Fig.4.59 Configuration of Function set ROM data 1

Function set ROM data 2

b7 b6 b5 b4 b3 b2 b1 b0

0	0						

Function set ROM data 2 (FSROM2)

[Address FFDAh]

b	Name	Function
0	Watchdog timer source clock selection bit (Note 1)	0: On-chip oscillator/16 1: On-chip oscillator/16 or f(XIN)/16 (Note 2)
1	Watchdog timer start selection bit (Note 3)	0: Watchdog timer starts automatically after reset 1: Watchdog timer is inactive after reset
2	Watchdog timer H count source selection bit (Note 4)	0: Watchdog timer L underflow 1: Watchdog timer L count source (Clock selected by the watchdog timer source clock selection bit (bit 0))
3	STP instruction function selection bit (Note 5)	0: Enter to stop mode at STP instruction execution 1: Internal reset at STP instruction execution
4	On-chip oscillator control bit (Notes 6)	0: Stop of on-chip oscillator disabled 1: Stop of on-chip oscillator enabled
5	Oscillation mode selection bit (Note 7)	0: Ceramic oscillation 1: RC oscillation
6	Set to 0.	
7		

Notes 1: This bit is enabled when the function set ROM disable bit (bit 0 of FSROM0) is set to 0.
When the function set ROM disable bit is set to 1 (disabled), the watchdog timer source clock is set to f(XIN)/16.

2: When double-speed mode, high-speed mode, or middle-speed mode is selected by the clock division ratio selection bits (bits 7, 6 of CPUM), the watchdog timer source clock is set to f(XIN)/16.
When the supply from the on-chip oscillator is selected, it is set to the on-chip oscillator output/16.

3: This bit is enabled when the function set ROM disable bit is set to 0.
When the function set ROM disable bit is set to 1 (disabled), the watchdog timer is stopped after reset.
The watchdog timer starts counting by writing to the watchdog timer control register.

4: This bit is enabled when the function set ROM disable bit is set to 0.
When the function set ROM disable bit is set to 1 (disabled), the watchdog timer H count source is selected by bit 7 of the watchdog timer control register (address 0039h).

5: This bit is enabled when the function set ROM disable bit is set to 0.
When the function set ROM disable bit is set to 1 (disabled), the STP instruction function is selected by bit 6 of the watchdog timer control register (address 0039h).

6: This bit is enabled when the function set ROM disable bit is set to 0.
Setting 0 to this bit fixes bit 3 of the CPU mode register to 0 (on-chip oscillator oscillation enabled) and the on-chip oscillator cannot be stopped.
The oscillation does not stop even in stop mode, increasing the current consumption in the mode.
When the function set ROM disable bit is set to 1 (disabled), the on-chip oscillator operation is selected by bit 3 of the CPU mode register (address 003Bh).

7: This bit is enabled when the function set ROM disable bit is set to 0.
When the function set ROM disable bit is set to 1 (disabled), the oscillation method is selected by bit 5 of the CPU mode register (address 003Bh).

Fig.4.60 Configuration of Function set ROM data 2

5. Reference Documents

Datasheet
7546 Group Datasheet
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology Corporation website

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Feb 20, 2007	—	First edition issued

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