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7544 Group

Clock Synchronous Serial I/O

1. Abstract

The following article introduces and shows an application example of clock synchronous of serial I/O.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: 7544 Group

3. Contents

For clock synchronous serial I/O, the transmitter and the receiver use the same clock. Synchronizing with this clock, the transmit operation of the transmitter and the receive operation of the receiver are executed at the same time. If an internal clock is used as the operation clock, transfer is started by a write signal to the TB/RB.

3.1 Data Transfer Rate

The synchronous clock frequency is calculated by the following formula;

- When the internal clock is selected (when baud rate generator is used)

$$\text{Synchronous clock frequency [Hz]} = \frac{f(X_{IN})}{\text{Division ratio } *1 \times (\text{BRG setting value } *2 + 1) \times 4}$$

Division ratio*1 : “1” or “4” is selected (set by bit 0 of serial I/O control register)
BRG setting value*2 : 0 to 255 (00_{16} to FF_{16}) is set

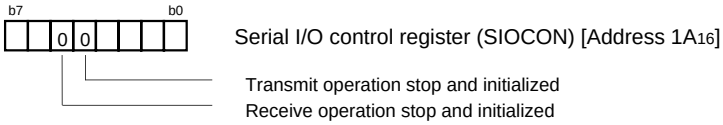
- When the external clock is selected

Synchronous clock frequency [Hz] = Clock input to S_{CLK} pin

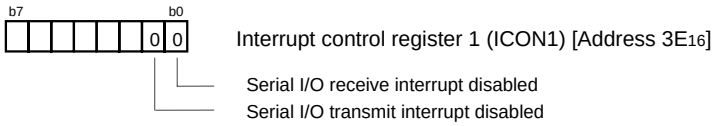
3.2 Clock Synchronous Serial I/O Setting Method

Figure 1 and Figure 2 show the setting method for the clock synchronous serial I/O.

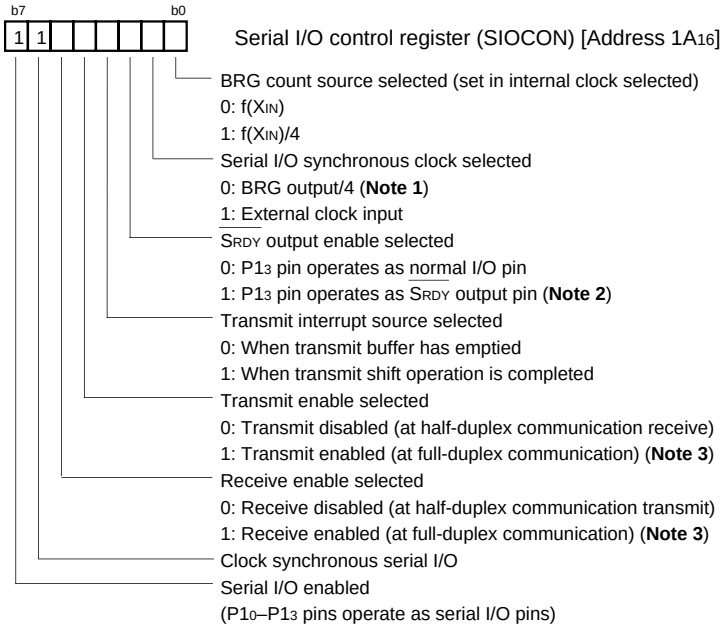
Process 1: Stop and initialize serial I/O.



Process 2: Disable serial I/O transmit/receive interrupt.



Process 3: Set serial I/O control register.



Note 1: Setting of serial I/O synchronous selection bit is as follows:
"0": P12 pin is set to be an output pin of the synchronous clock.
"1": P12 pin is set to be an input pin of the synchronous clock.

2: When an external clock input is selected as the synchronous clock, and the receiver performs the SRDY output, set "1" to the transmit enable bit in addition to the receive enable bit and SRDY output enable bit.

3: When data transmission is executed at the state that an external clock input is selected as the synchronous clock, set "1" to the transmit enable bit while the SCLK is "H" state.

Process 4: When BRG output/4 is selected as synchronous clock, set value to baud rate generator.

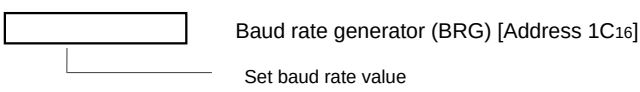
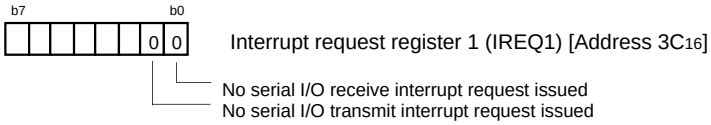
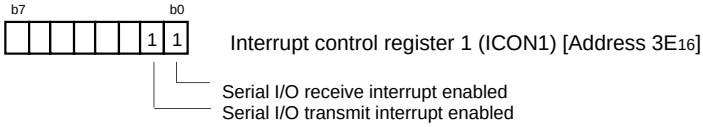


Figure 1 Setting method for clock synchronous serial I/O (1)

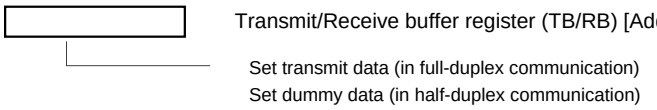
Process 5: In order not to execute the no requested interrupt processing, set “0” (no requested) to the serial I/O transmit/receive interrupt request bit.



Process 6: When the interrupt is used, set “1” (interrupt enabled) to the serial I/O transmit/receive interrupt enable bit.



Process 7: Transmit/Receive of serial data (**Notes 1, 2**).



Notes 1: When data transmission is executed at the state that an external clock input is selected as the synchronous clock, set the transmit data while the SCLK is “H” state.
2: When inputting the SRDY signal, set used pins to to the input mode before transmitting data.

Figure 2 Setting method for clock synchronous serial I/O (2)

3.3 Communication Using Clock Synchronous Serial I/O (Transmit/Receive)

Outline : 2-byte data is transmitted and received, using the clock synchronous serial I/O. $\overline{SRDY}$ signal is used for communication control.

Specifications : •The serial I/O (clock synchronous serial I/O selected) is used.
•Synchronous clock frequency : 125 kHz; f(X_{IN}) = 4 MHz divided by 32
•The receiver outputs the $\overline{SRDY}$ signal at 2 ms intervals which the timer generates, and 2-byte data is transferred from the transmitter to the receiver.

Figure 3 shows a connection diagram, Figure 4 shows a timing chart, Figure 5 shows the control procedure of transmitter, and Figure 6 shows an example of control procedure of receiver.

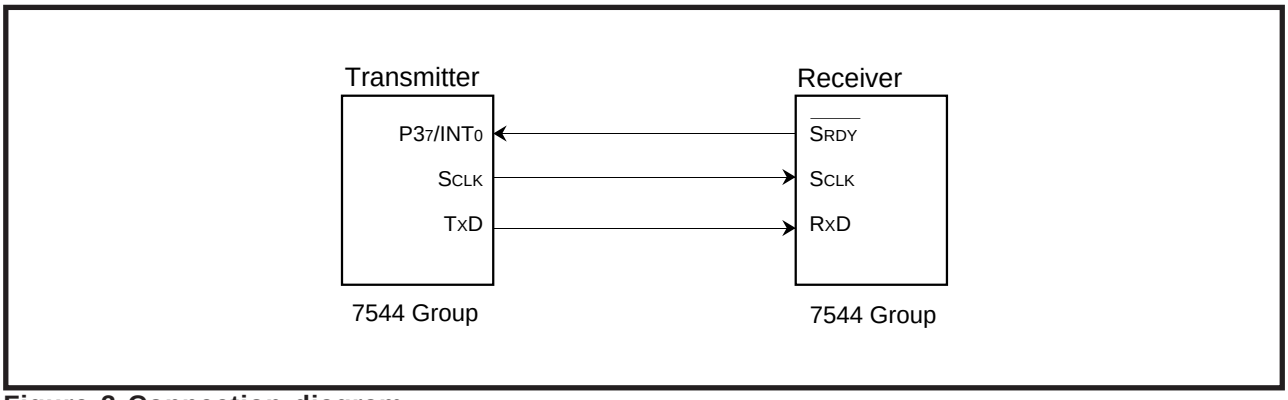


Figure 3 Connection diagram

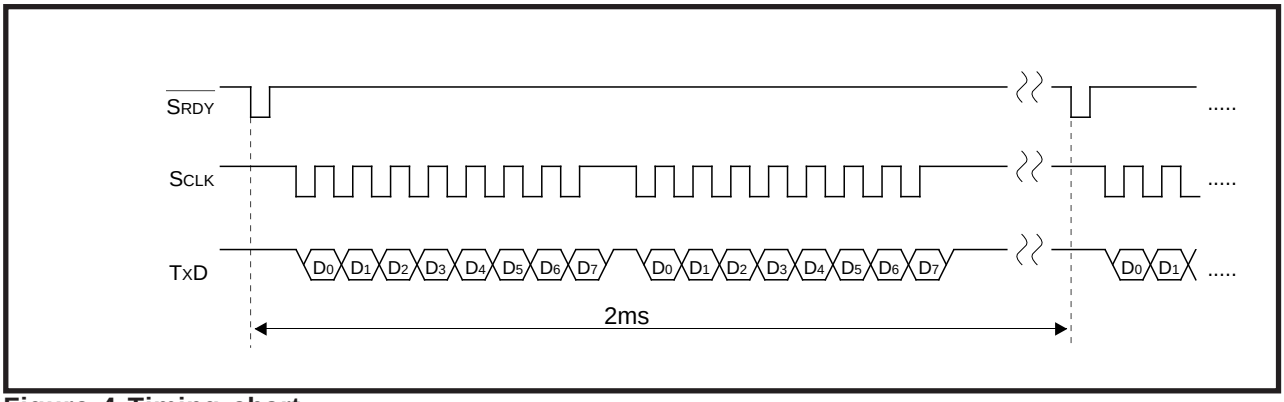


Figure 4 Timing chart

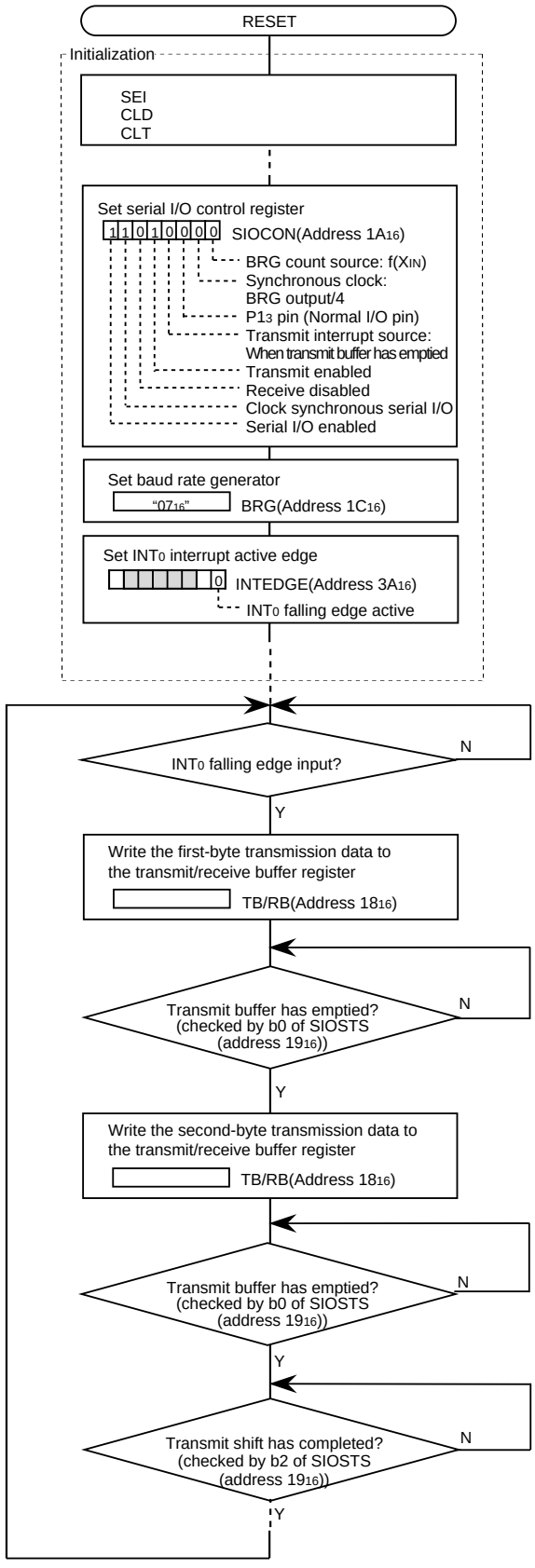


Figure 5 Control procedure of transmitter

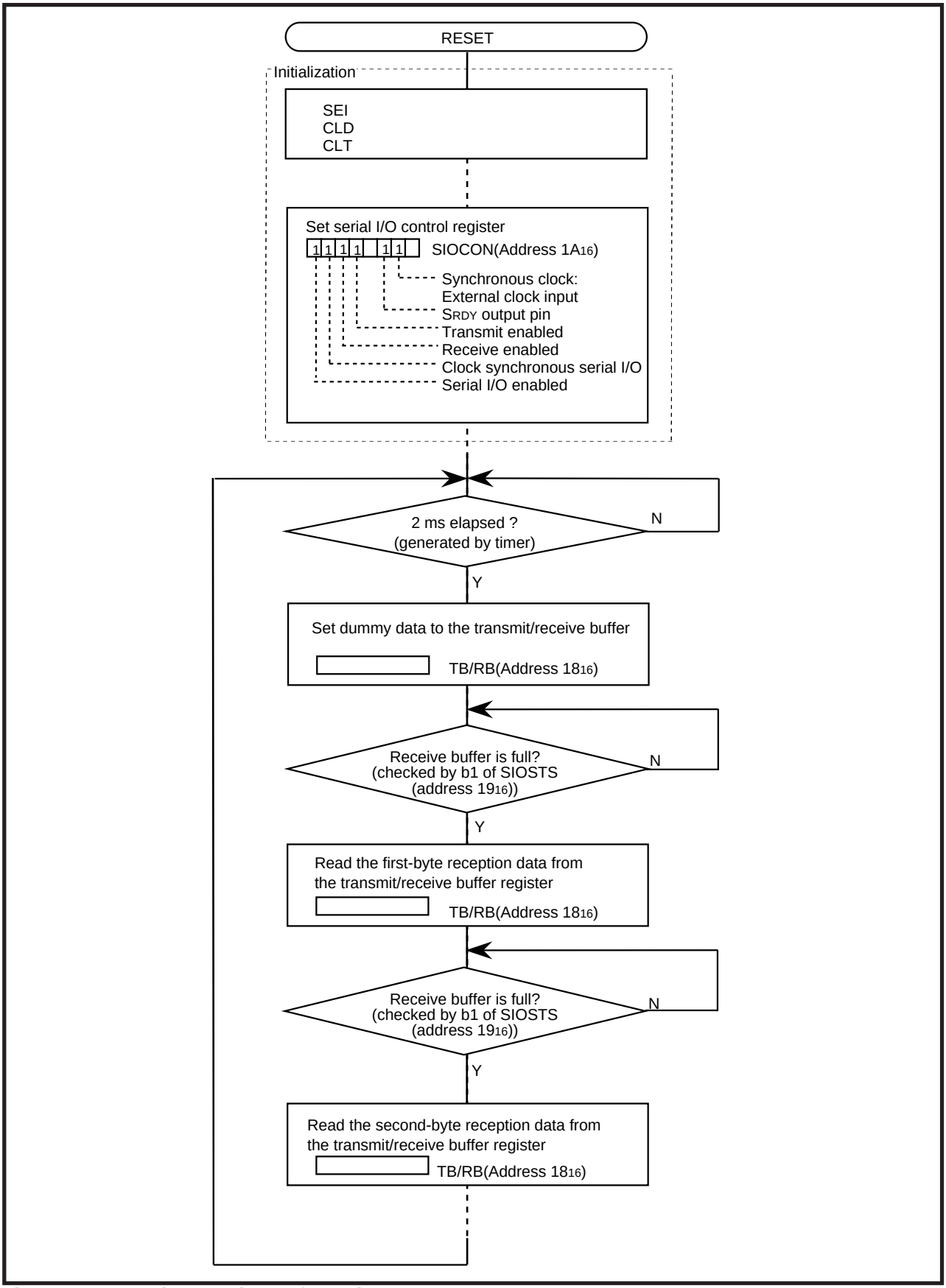


Figure 6 Control procedure of receiver

4. Sample Programming Code

```
[Reset Start ••• Main Routine Process]

RESET:
          SEI                       ; Interrupt disable
          CLD
          CLT
;
          LDX  #$FF                 ; Set stack bottom
          TXS
;
          LDM  #%10000000,CPUM      ; Set CPU mode register
;
; Wait f(XIN) oscillation stabilizing time
;
          LDM  #%00000000,CPUM      ; Set CPU mode register
;
          LDA  #0
          LDX  #>RAM_top
RAM_clear:STA  $00,X
          INX
          BNE  RAM_clear
;
Sio_initial:
          LDM  #%11010000,SIOCON    ; BRG count source : f(Xin)
                                    ; synchronous clock : divided 4
                                    ; P1_3 function : normal I/O pin
                                    ; interrupt request factor : transmit buffer is empty
                                    ; enable transmit
                                    ; disable receive
                                    ; serial I/O mode : synchronous serial I/O mode
                                    ; enable serial I/O
          LDM  #$07,BRG             ; set baud rate

          CLB  0,INTEDGE            ; INT0 falling edge active

          LDM  #$055,SEND_DATA
          LDM  #$0AA,SEND_DATA+1

;
;
;-------------------------------------------------------------------------------
__MAIN:
          BBC  2,IREQ1,__MAIN       ; input INT0 falling edge
          CLB  2,IREQ1

          LDA  SEND_DATA
          STA  TBRB                 ; Send data write

__MAIN00:
          BBC  0,SIOSTS,__MAIN00    ; data send? -> no
;
          LDA  SEND_DATA+1
          STA  TBRB                 ; Next send data write

__MAIN01:
          BBC  0,SIOSTS,__MAIN01    ; data send? -> no
;
__MAIN02:
          BBC  2,SIOSTS,__MAIN02    ; Shift end check ? -> no
;
          BRA  __MAIN
;
```

Figure 7 Sample Programming Code (Transmit Side)

[Reset Start ••• Main Routine Process]

```
RESET:
          SEI                       ; Interrupt disable
          CLD
          CLT
;
          LDX  #$FF                 ; Set stack bottom
          TXS
;
          LDM  #%10000000,CPUM      ; Set CPU mode register
;
; Wait f(XIN) oscillation stabilizing time
;
          LDM  #%00000000,CPUM      ; Set CPU mode register
;
          LDA  #0
          LDX  #>RAM_top
RAM_clear:STA  $00,X
          INX
          BNE  RAM_clear
;
Sio_initial:
          LDM  #%11110110,SIOCON    ; synchronous clock : external clock
                                    ; P1_3 pin function : SRDY output pin
                                    ; enable transmit
                                    ; enable receive
                                    ; serial I/O mode : synchronous serial I/O mode
                                    ; enable serial I/O

          LDM  #$00,TCSS2           ; select timer 1 count source : f(Xin)/16
          LDM  #65-1,PRE1           ; Set Prescaler 1
          LDM  #8-1,T1              ; Set Timer 1
          CLB  5,IREQ2              ; clear timer 1 interrupt request
          NOP

;
;-------------------------------------------------------------------------------
__MAIN:
          BBC  5,IREQ2,__MAIN       ; 2ms?
          CLB  5,IREQ2

          LDA  #$00                 ; write dummy data
          STA  TBRB

__MAIN_00:
          BBC  1,SIOSTS,__MAIN_00   ; data receive ? -> no
;
          LDA  TBRB
          STA  Receive_Data         ; store receive data

          LDA  #$00                 ; write dummy data
          STA  TBRB

__MAIN01:
          BBC  1,SIOSTS,__MAIN01    ; data receive ? -> no
;
          LDA  TBRB
          STA  Receive_Data+1       ; store next receive data

          BRA  __MAIN
;
```

Figure 8 Sample Programming Code (Receive Side)

5. Reference

Data Sheet
7544 Group Data sheet
7544 Group Data sheet (QzROM Version)

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REVISION HISTORY	7544 Group Clock Synchronous Serial I/O

Rev.	Date	Description	
		Page	Summary
1.00	Apr 01, 2003	-	First Edition issued
2.00	Nov 12, 2004	8-9	Sample Programming Code added.

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