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April 1st, 2010
Renesas Electronics Corporation

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7542 Group

Clock Synchronous Serial I/O

1.0 Abstract

The following article introduces and shows an application example of clock synchronous of serial I/O1.

2.0 Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: 7542 Group

3.0 Contents

For clock synchronous serial I/O1, the transmitter and the receiver use the same clock. Synchronizing with this clock, the transmit operation of the transmitter and the receive operation of the receiver are executed at the same time. If an internal clock is used as the operation clock, transfer is started by a write signal to the TB/RB.
Also, as for the serial I/O2, since it has an equivalent function to serial I/O1, the application example of the following serial I/O1 is applicable for serial I/O2.

3.1 Data Transfer Rate

The synchronous clock frequency is calculated by the following formula;

- When the internal clock is selected (when baud rate generator is used)

$$\text{Synchronous clock frequency [Hz]} = \frac{f(X_{IN})}{\text{Division ratio } *1 \times (\text{BRG1 setting value } *2 + 1) \times 4}$$

Division ratio*1 : “1” or “4” is selected (set by bit 0 of serial I/O1 control register)
BRG1 setting value*2 : 0 to 255 (00_{16} to FF_{16}) is set

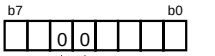
- When the external clock is selected

Synchronous clock frequency [Hz] = Clock input to S_{CLK} pin

3.2 Clock Synchronous Serial I/O1 Setting Method

Figure 1 and Figure 2 show the setting method for the clock synchronous serial I/O1.

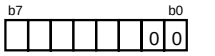
Process 1: Stop and initialize serial I/O.



Serial I/O1 control register (SIO1CON) [Address $1A_{16}$]

Transmit operation stop and initialized
Receive operation stop and initialized

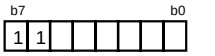
Process 2: Disable serial I/O1 transmit/receive interrupt.



Interrupt control register 1 (ICON1) [Address $3E_{16}$]

Serial I/O1 receive interrupt disabled
Serial I/O1 transmit interrupt disabled

Process 3: Set serial I/O1 control register.



Serial I/O1 control register (SIO1CON) [Address $1A_{16}$]

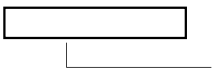
BRG count source selected (set in internal clock selected)
0: f(X_{IN})
1: f(X_{IN})/4
Serial I/O1 synchronous clock selected (**Note 1**)
0: BRG output/4
1: External clock input
$\overline{S_{RDY1}}$ output enable selected
0: $P1_3$ pin operates as normal I/O pin
1: $P1_3$ pin operates as $\overline{S_{RDY1}}$ output pin (**Note 2**)
Transmit interrupt source selected
0: When transmit buffer has emptied
1: When transmit shift operation is completed
Transmit enable selected
0: Transmit disabled (at half-duplex communication receive)
1: Transmit enabled (at full-duplex communication) (**Note 3**)
Receive enable selected
0: Receive disabled (at half-duplex communication transmit)
1: Receive enabled (at full-duplex communication) (**Note 3**)
Clock synchronous serial I/O
Serial I/O1 enabled
($P1_0$–$P1_3$ pins operate as serial I/O1 pins)

Note 1: Setting of serial I/O1 synchronous selection bit is as follows:
"0": $P1_2$ pin is set to be an output pin of the synchronous clock.
"1": $P1_2$ pin is set to be an input pin of the synchronous clock.

2: When an external clock input is selected as the synchronous clock, and the receiver performs the $\overline{S_{RDY1}}$ output, set "1" to the transmit enable bit in addition to the receive enable bit and $\overline{S_{RDY1}}$ output enable bit.

3: When data transmission is executed at the state that an external clock input is selected as the synchronous clock, set "1" to the transmit enable bit while the S_{CLK1} is "H" state.

Process 4: When BRG output/4 is selected as synchronous clock, set value to baud rate generator.

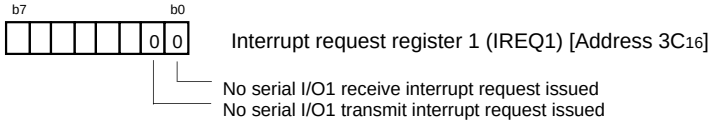


Baud rate generator1 (BRG1) [Address $1C_{16}$]

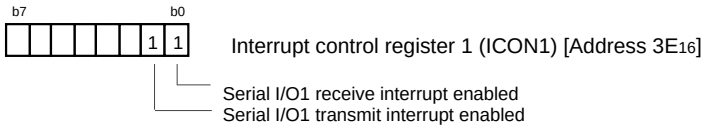
Set baud rate value

Figure 1 Setting method for clock synchronous serial I/O1 (1)

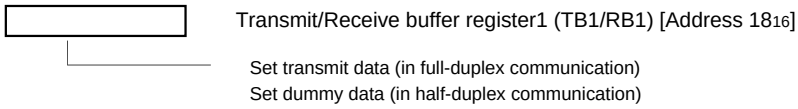
Process 5: In order not to execute the no requested interrupt processing, set “0” (no requested) to the serial I/O1 transmit/receive interrupt request bit.



Process 6: When the interrupt is used, set “1” (interrupt enabled) to the serial I/O transmit/receive interrupt enable bit.



Process 7: Transmit/Receive of serial data (**Notes 1, 2**).



Notes 1: When data transmission is executed at the state that an external clock input is selected as the synchronous clock, set the transmit data while the S_{CLK1} is “H” state.
2: When inputting the S_{RDY1} signal, set used pins to to the input mode before transmitting data.

Figure 2 Setting method for clock synchronous serial I/O1 (2)

3.3 Communication Using Clock Synchronous Serial I/O1 (Transmit/Receive)

Outline : 2-byte data is transmitted and received, using the clock synchronous serial I/O1. $\overline{S_{RDY1}}$ signal is used for communication control.

Specifications : •The serial I/O1 (clock synchronous serial I/O selected) is used.
•Synchronous clock frequency : 125 kHz; f(X_{IN}) = 4 MHz divided by 32
•The receiver outputs the $\overline{S_{RDY1}}$ signal at 2 ms intervals which the timer generates, and 2-byte data is transferred from the transmitter to the receiver.

Figure 3 shows a connection diagram, Figure 4 shows a timing chart, Figure 5 shows the control procedure of transmitter, and Figure 6 shows an example of control procedure of receiver.

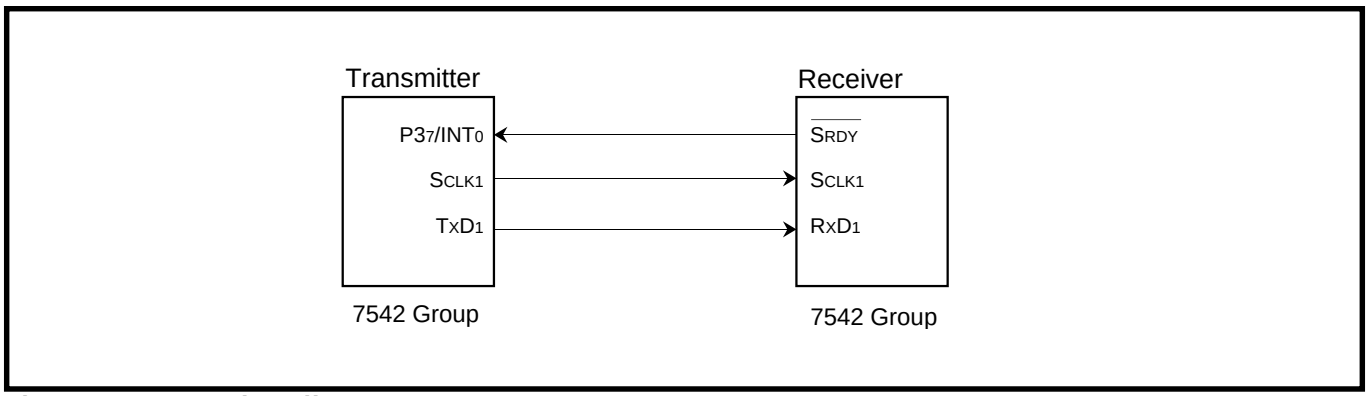


Figure 3 Connection diagram

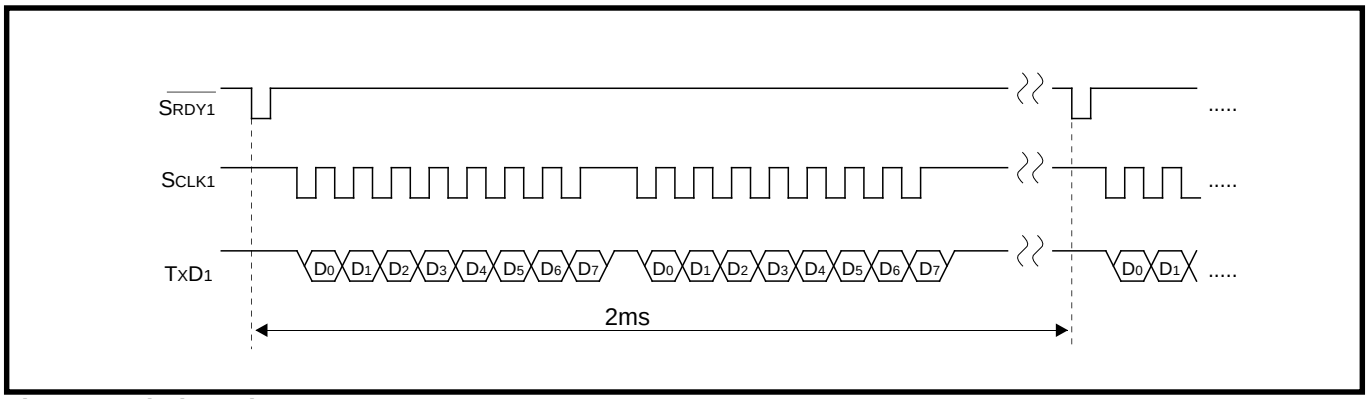


Figure 4 Timing chart

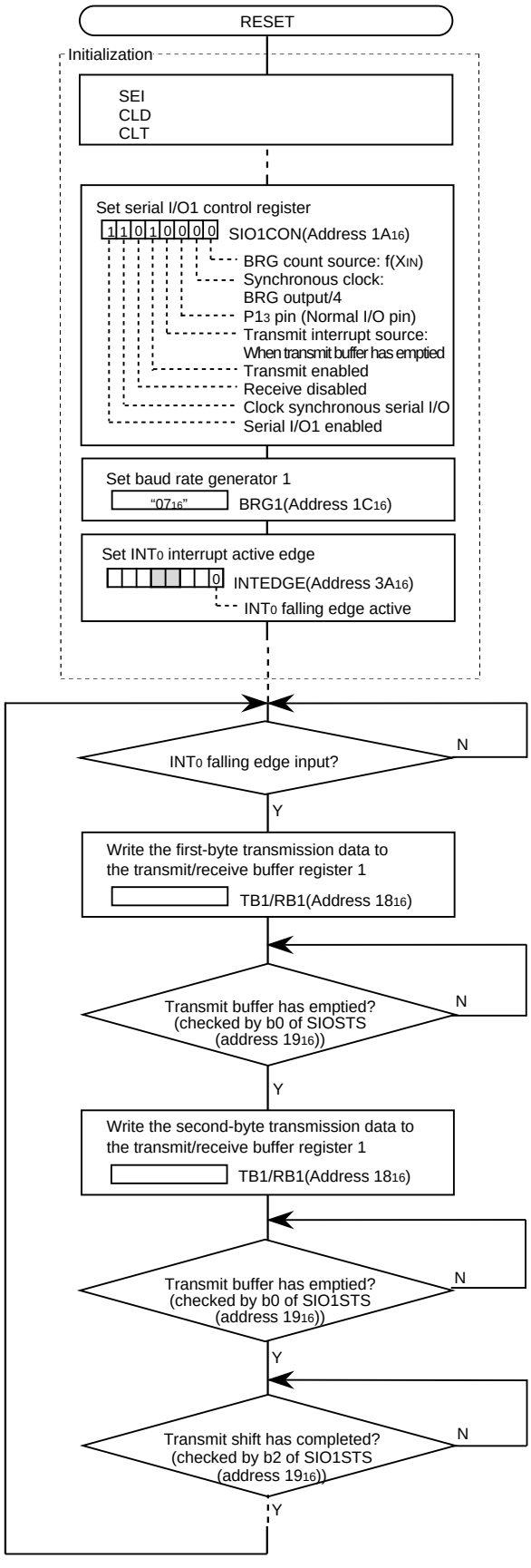


Figure 5 Control procedure of transmitter

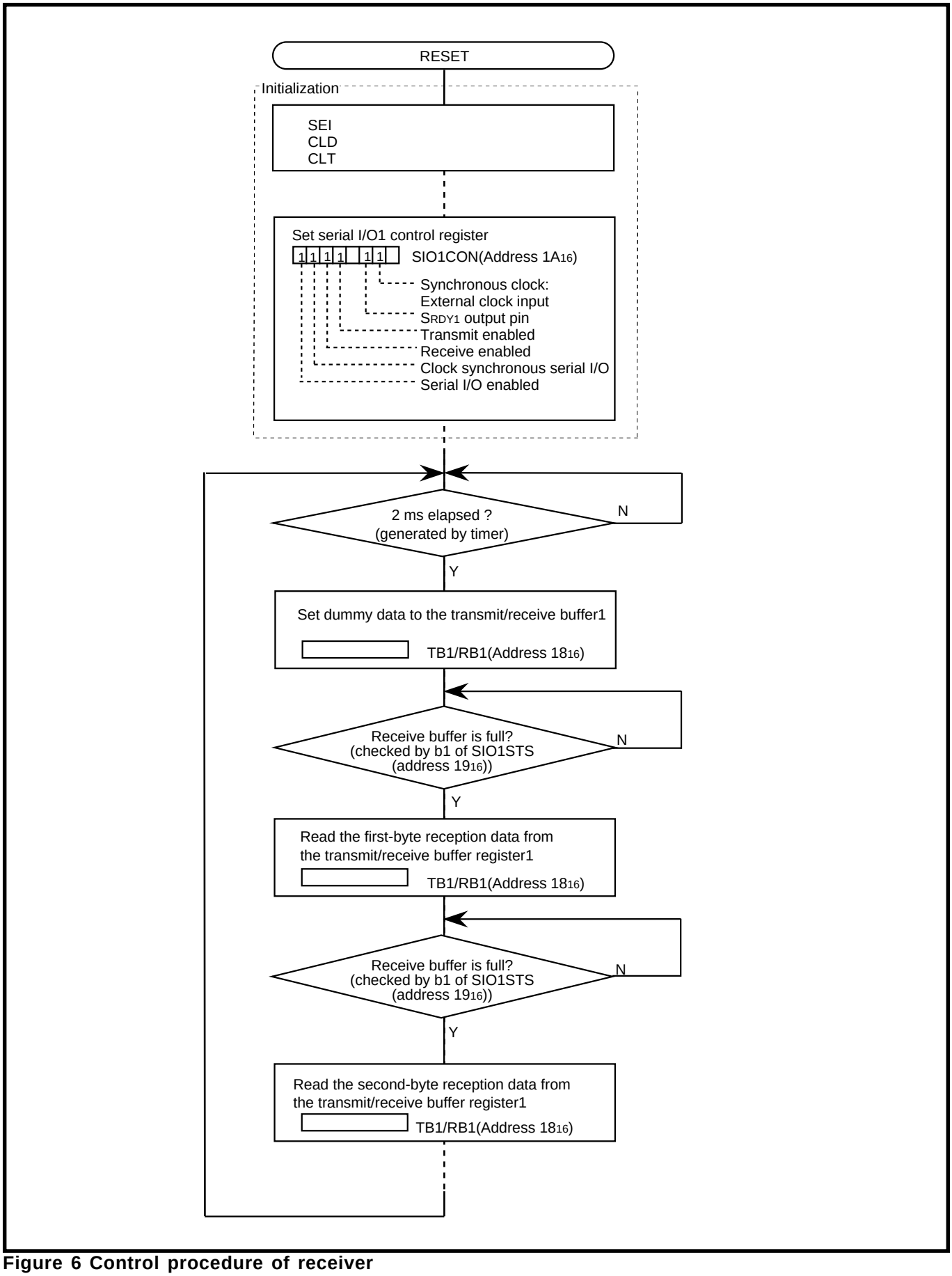


Figure 6 Control procedure of receiver

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