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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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7542 Group

Clock Generation Circuit (Processing During a Power Failure)

1. Abstract

The following article introduces and shows an example of how to use the Clock Generation Circuit (Processing During a Power Failure) in the 7542 Group.

2. Introduction

The application explained in this document applies to the following MCU and parameters:

- Applicable MCU: 7542 Group
- Main clock oscillation frequency (f(XIN)): 8 MHz
- On-chip oscillator frequency (ROSC): 2 MHz (typ)

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the user system operating parameters.

3. Contents

3.1 Clock Generation Circuit (Processing During a Power Failure)

Outline: During a power failure, the backup power supply enables low power consumption operation in on-chip oscillator and wait modes.

Specifications:

- High-speed mode operation is selected under normal conditions.
- The system clock is divide by 128 of the on-chip oscillator when the on-chip oscillator operates.
- When a power failure is detected, operation is switched to on-chip oscillator mode and the main clock oscillation stops.
- Using wait mode, the timer interrupt routine that occurs every 30 ms confirms the conditions for exit from a power failure.
- When an exit from power failure is detected, the main clock oscillation starts. After oscillation is stabilized, the system clock is switched to high-speed mode.

Figure 3.1 shows a Mode Transition Example of System Clock ϕ During a Power Failure, Figure 3.2 shows the Relevant Register Settings, and Figure 3.3 shows the Control Procedure.

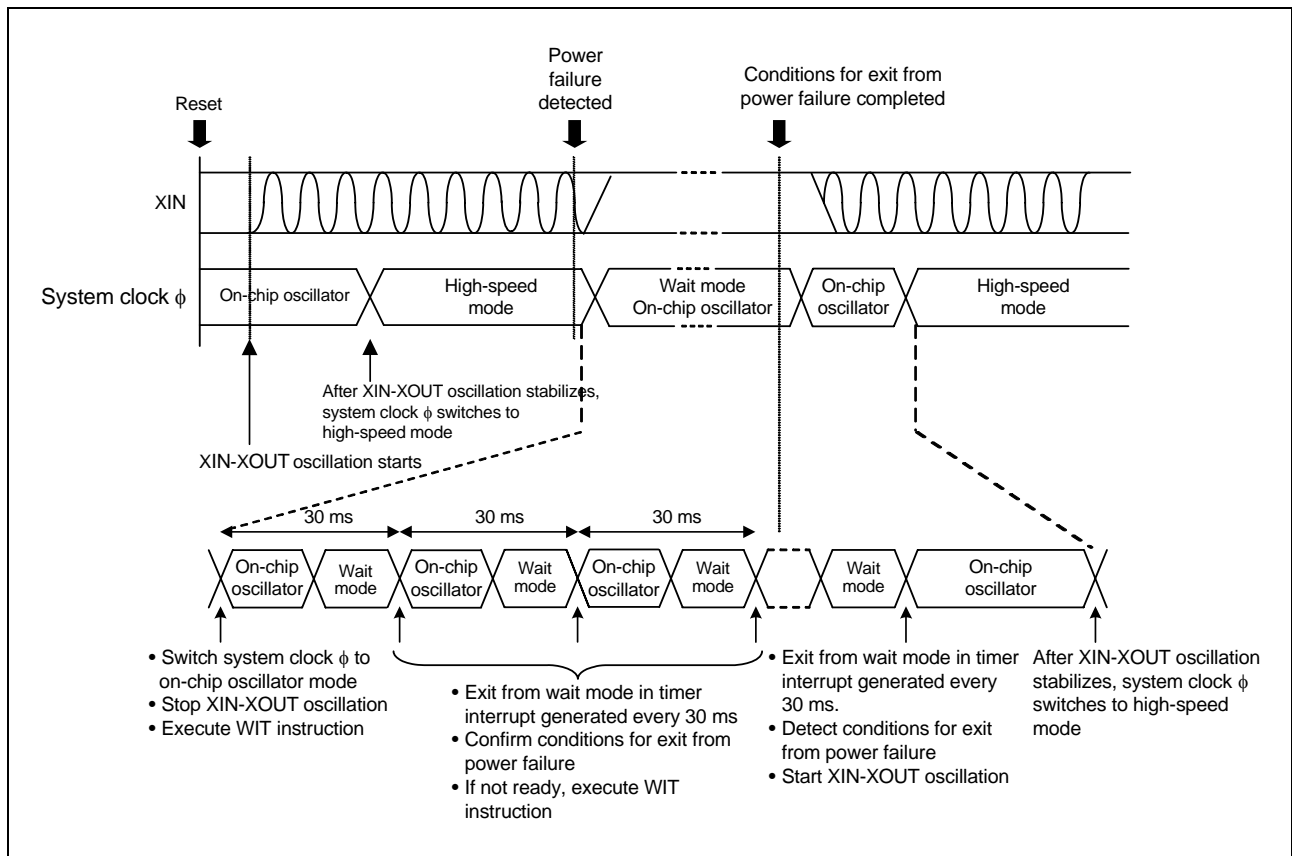


Figure 3.1 Mode Transition Example of System Clock ϕ During a Power Failure

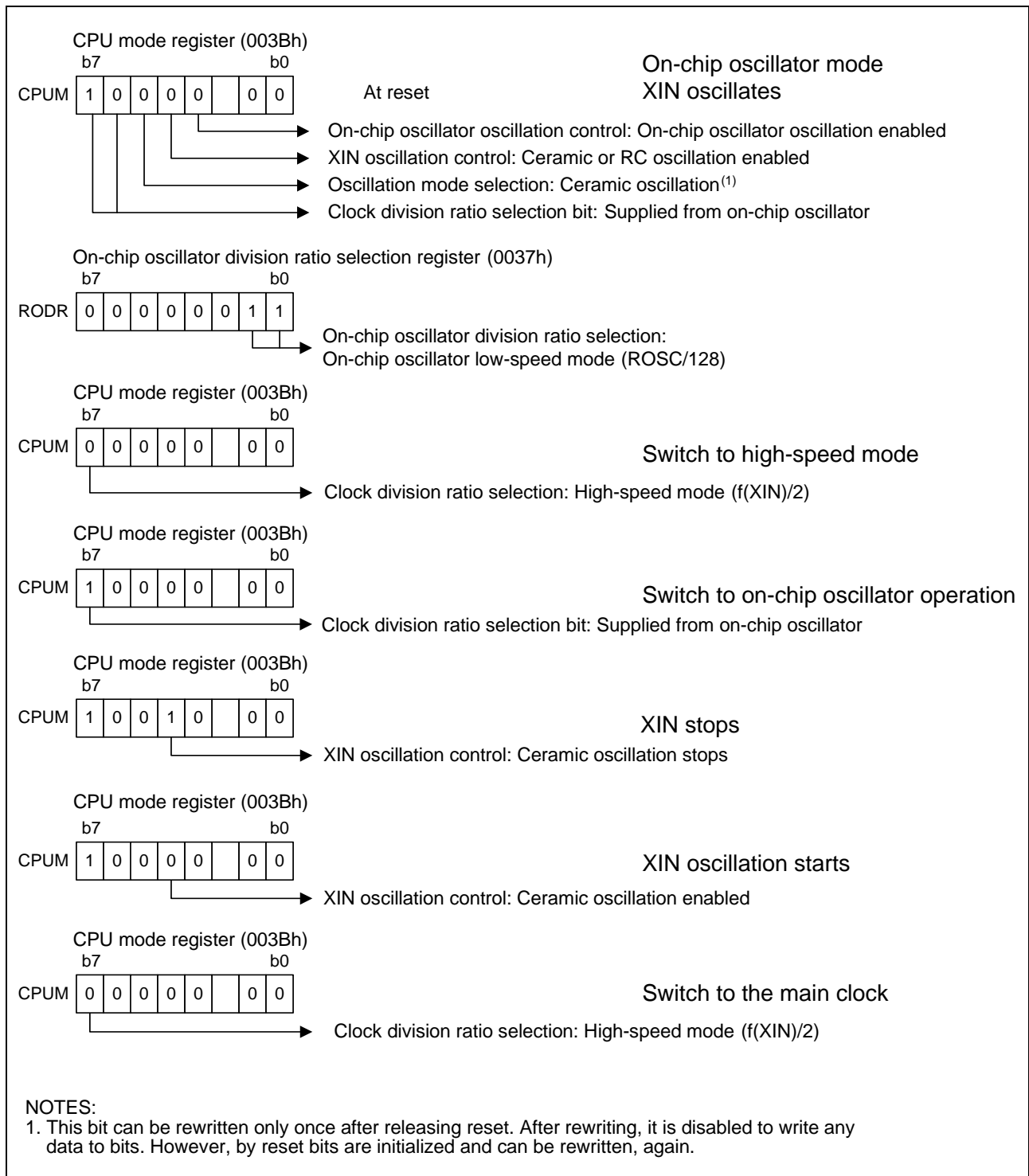


Figure 3.2 Relevant Register Settings

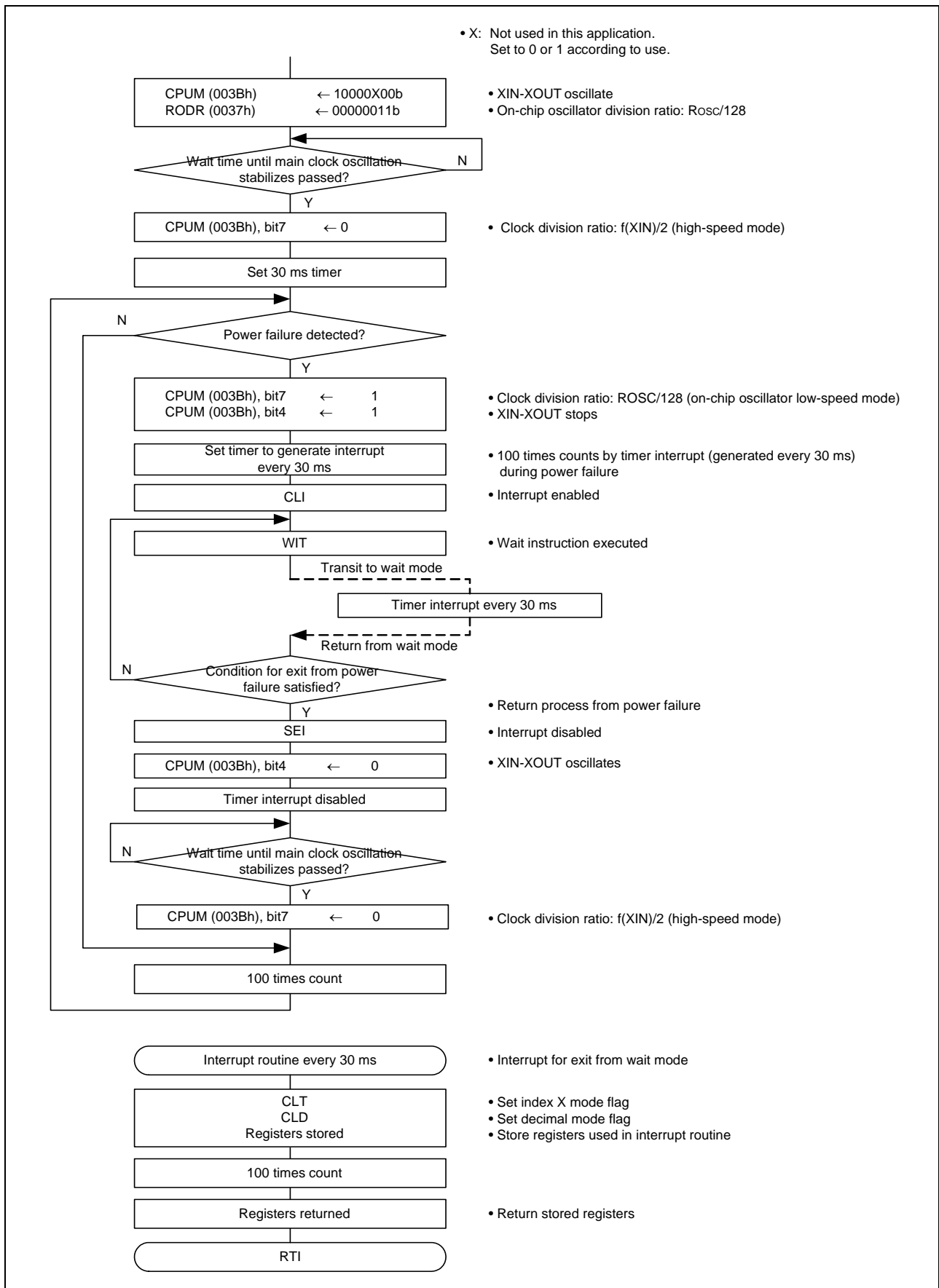


Figure 3.3 Control Procedure

4. Reference Document

Datasheet

7542 Group Datasheet

(Use the most recent version of the document on the Renesas Technology Web site.)

Technical News/Technical Update

(Use the most recent version of the document on the Renesas Technology Web site.)

5. Sample Programming Code

Please visit the Renesas Technology Web site for a reference program.

Click Application Note in the left menu of the 7542 Group.

Web site and Support

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<http://www.renesas.com/>

Inquiries
<http://www.renesas.com/inquiry>
csc@renesas.com

REVISION HISTORY	7542 Group Clock Generation Circuit (Processing During a Power Failure)
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Rev.	Date	Description	
		Page	Summary
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