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4571 Group

Interrupts

1. Abstract

This document shows an example of how to set interrupts in the 4571 group of Renesas microcomputers and an application example for using those interrupts.

2. Introduction

The application example explained in this document is applied for use with the microcomputers and under the conditions described below.

- Microcomputer : 4571 group
- Oscillation frequency : 4 MHz (external 0, external 1 and timer 1), 2 MHz (timer 2), 6 MHz (timer 3), 1 MHz (voltage down detection circuit)
- System clock : Through mode (not frequency divided)

Please note that some sample programs available from Renesas involve manipulating the bits of unused functions for reasons of bit arrangement in the control registers. The values of these bits in a user system should be set to suit the usage condition of the system.

In this application note, explanation is made of an example of interrupt setting method and an application example with respect to the following:

- External 0 interrupt
- External 1 interrupt
- Timer 1 interrupt
- Timer 2 interrupt
- Timer 3 interrupt
- Voltage down detection circuit interrupt

3. Related Registers

3.1 Interrupt Control Register V1

Table 3.1 shows the Bit Configuration of Interrupt Control Register V1.
For write to the register V1, first set a value in the register A and then use the TV1A instruction.
Furthermore, the TAV1 instruction may be used to transfer the content of the register V1 to the register A.

Table 3.1 Bit Configuration of Interrupt Control Register V1

Interrupt Control Register V1		When reset: 0000_2	When RAM backed-up: 0000_2	R/W TAV1/TV1A
$V1_3$	Timer 2 interrupt enable bit	0	Disables interrupt generation (SNZT2 instruction is valid)	
		1	Enables interrupt generation (SNZT2 instruction is invalid)	
$V1_2$	Timer 1 interrupt enable bit	0	Disables interrupt generation (SNZT1 instruction is valid)	
		1	Enables interrupt generation (SNZT1 instruction is invalid)	
$V1_1$	External 1 interrupt enable bit	0	Disables interrupt generation (SNZ1 instruction is valid)	
		1	Enables interrupt generation (SNZ1 instruction is invalid)	
$V1_0$	External 0 interrupt enable bit	0	Disables interrupt generation (SNZ0 instruction is valid)	
		1	Enables interrupt generation (SNZ0 instruction is invalid)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

3.2 Interrupt Control Register V2

Table 3.2 shows the Bit Configuration of Interrupt Control Register V2.
For write to the register V2, first set a value in the register A and then use the TV2A instruction.
Furthermore, the TAV2 instruction may be used to transfer the content of the register V2 to the register A.

Table 3.2 Bit Configuration of Interrupt Control Register V2

Interrupt Control Register V2		When reset: 0000_2	When RAM backed-up: 0000_2	R/W TAV2/TV2A
$V2_3$	Voltage down detection circuit interrupt enable bit	0	Disables interrupt generation (SNZVD instruction is valid)	
		1	Enables interrupt generation (SNZVD instruction is invalid)	
$V2_2$	Unused	0	This bit has no functions, but can be accessed for read/write.	
		1		
$V2_1$	Unused	0	This bit has no functions, but can be accessed for read/write.	
		1		
$V2_0$	Timer 3 interrupt enable bit	0	Disables interrupt generation (SNZT3 instruction is valid)	
		1	Enables interrupt generation (SNZT3 instruction is invalid)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: : Unused bits during interrupt setting

3.3 Interrupt Control Register I1

Table 3.3 shows the Bit Configuration of Interrupt Control Register I1.

For write to the register I1, first set a value in the register A and then use the TI1A instruction.

Furthermore, the TAI1 instruction may be used to transfer the content of the register I1 to the register A.

Table 3.3 Bit Configuration of Interrupt Control Register I1

Interrupt Control Register I1		When reset: 0000_2	When RAM backed-up: State retained	R/W TAI1/TI1A
$I1_3$	INT0 pin input control bit Note 2	0	Disables input	
		1	Enables input	
$I1_2$	INT0 pin interrupt active waveform/ return level select bit Note 2	0	Falling waveform/low level (SNZI0 instruction recognizes low level on INT0 pin)	
		1	Rising waveform/high level (SNZI0 instruction recognizes high level on INT0 pin)	
$I1_1$	INT0 pin edge detection circuit control bit	0	Detects one edge	
		1	Detects both edges	
$I1_0$	INT0 pin timer 1 control enable bit	0	Disables timer 1 control	
		1	Enables timer 1 control	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: When the contents of these bits ($I1_2$ or $I1_3$) are changed, the external interrupt request flag (EXF0) may be set.

3.4 Interrupt Control Register I2

Table 3.4 shows the Bit Configuration of Interrupt Control Register I2.

For write to the register I2, first set a value in the register A and then use the TI2A instruction.

Furthermore, the TAI2 instruction may be used to transfer the content of the register I2 to the register A.

Table 3.4 Bit Configuration of Interrupt Control Register I2

Interrupt Control Register I2		When reset: 0000_2	When RAM backed-up: State retained	R/W TAI2/TI2A
$I2_3$	INT1 pin input control bit Note 2	0	Disables input	
		1	Enables input	
$I2_2$	INT1 pin interrupt active waveform/ return level select bit Note 2	0	Falling waveform/low level (SNZI1 instruction recognizes low level on INT1 pin)	
		1	Rising waveform/high level (SNZI1 instruction recognizes high level on INT1 pin)	
$I2_1$	INT1 pin edge detection circuit control bit	0	Detects one edge	
		1	Detects both edges	
$I2_0$	Unused	0	This bit has no functions, but can be accessed for read/write.	
		1		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: When the contents of these bits ($I2_2$ or $I2_3$) are changed, the external interrupt request flag (EXF1) may be set.

Note 3: : Unused bits during interrupt setting

3.5 Timer Control Register PA

Table 3.5 shows the Bit Configuration of Timer Control Register PA.

For write to the register PA, first set a value in the register A and then use the TPAA instruction.

Table 3.5 Bit Configuration of Timer Control Register PA

Timer Control Register PA		When reset: 00_2	When RAM backed-up: 00_2	W TPAA
PA_1	Prescaler count source select bit	0	Instruction clock (INSTCK)	
		1	Divide-by-4 signal of instruction clock (INSTCK)	
PA_0	Prescaler control bit	0	Stop (state retained)	
		1	Operating	

Note 1: The letter W denotes “writable.”

3.6 Timer Control Register W1

Table 3.6 shows the Bit Configuration of Timer Control Register W1.

For write to the register W1, first set a value in the register A and then use the TW1A instruction.

Furthermore, the TAW1 instruction may be used to transfer the content of the register W1 to the register A.

Table 3.6 Bit Configuration of Timer Control Register W1

Timer Control Register W1		When reset: 0000_2	When RAM backed-up: State retained	R/W TAW1/TW1A
$W1_3$	Timer 1 count auto stop circuit select bit Note 2	0	Does not select timer 1 count auto stop circuit	
		1	Selects timer 1 count auto stop circuit	
$W1_2$	Timer 1 control bit	0	Stop (state retained)	
		1	Operating	
$W1_1$	Timer 1 count source select bit	$W1_1$	$W1_0$	Count source
		0	0	PWM signal (PWMOUT)
		0	1	Prescaler output (ORCLK)
$W1_0$		1	0	System clock (STCK)
		1	1	CNTR0 input

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: This function is usable only when INT0 pin timer 1 control is enabled ($I1_0$ = 1) and the timer 1 count start sync circuit is selected ($W5_3$ = 1).

3.7 Timer Control Register W2

Table 3.7 shows the Bit Configuration of Timer Control Register W2.

For write to the register W2, first set a value in the register A and then use the TW2A instruction.

Furthermore, the TAW2 instruction may be used to transfer the content of the register W2 to the register A.

Table 3.7 Bit Configuration of Timer Control Register W2

Timer Control Register W2		When reset: 0000_2			When RAM backed-up: State retained	R/W TAW2/TW2A
$W2_3$	CNTR0 pin function select bit	0	Divide-by-2 output of time 1 underflow signal			
		1	Divide-by-2 output of time 2 underflow signal			
$W2_2$	Timer 2 control bit	0	Stop (state retained)			
		1	Operating			
$W2_1$	Timer 2 count source select bit	$W2_1$	$W2_0$	Count source		
		0	0	PWM signal (PWMOUT)		
		0	1	Prescaler output (ORCLK)		
$W2_0$		1	0	System clock (STCK)		
		1	1	Time 1 underflow signal (T1UDF)		

Note 1: The letter R denotes "readable," and the letter W denotes "writable."

3.8 Timer Control Register W3

Table 3.8 shows the Bit Configuration of Timer Control Register W3.

For write to the register W3, first set a value in the register A and then use the TW3A instruction.

Furthermore, the TAW3 instruction may be used to transfer the content of the register W3 to the register A.

Table 3.8 Bit Configuration of Timer Control Register W3

Timer Control Register W3		When reset: 0000_2		When RAM backed-up: 0000_2	R/W TAW3/TW3A
$W3_3$	CNTR1 pin output control bit	0	Disables CNTR1 pin output		
		1	Enables CNTR1 pin output		
$W3_2$	PWM signal high period extension function control bit	0	Disables PWM signal high period extension function		
		1	Enables PWM signal high period extension function		
$W3_1$	Timer 3 control bit	0	Stop (state retained)		
		1	Operating		
$W3_0$	Timer 3 count source select bit	0	X_{IN} input		
		1	Divide-by-2 signal of prescaler output (ORCLK)		

Note 1: The letter R denotes "readable," and the letter W denotes "writable."

3.9 Timer Control Register W5

Table 3.9 shows the Bit Configuration of Timer Control Register W5.

For write to the register W5, first set a value in the register A and then use the TW5A instruction.

Furthermore, the TAW5 instruction may be used to transfer the content of the register W5 to the register A.

Table 3.9 Bit Configuration of Timer Control Register W5

Timer Control Register W5		When reset: 0000_2		When RAM backed-up: State retained	R/W TAW5/TW5A
$W5_3$	Timer 1 count start sync circuit select bit Note 2	0	Does not select timer 1 count start sync circuit		
		1	Selects timer 1 count start sync circuit		
$W5_2$	CNTR0 pin input count edge select bit	0	Falling edge		
		1	Rising edge		
$W5_1$	CNTR1 pin output auto control circuit select bit	0	Does not select CNTR1 pin output auto control circuit		
		1	Selects CNTR1 pin output auto control circuit		
$W5_0$	D_4/CNTR0 pin function select bit	0	D_4 input-output/CNTR0 input		
		1	D_4 input/CNTR0 output		

Note 1: The letter R denotes "readable," and the letter W denotes "writable."

Note 2: This function is usable only when INT0 pin timer 1 control is enabled ($I1_0$ = 1).

4. Application Example of Using the Interrupts

4.1 External 0 Interrupt

The INT0 pin is an external interrupt pin whose active waveform is selectable. A falling edge (H → L), rising edge (L → H) and both edges (H → L and L → H) on this pin can be recognized.

Point: A falling edge (H → L), rising edge (L → H) or both edges (H → L and L → H) can be used as a trigger for external 0 interrupt.

Specification: External 0 interrupt is generated by both edges (H → L and L → H) of an external signal.

Figure 4.1 shows an Example of External 0 Interrupt Operation, and Figure 4.3 shows an Example of External 0 Interrupt Setting.

4.2 External 1 Interrupt

The INT1 pin is an external interrupt pin whose active waveform is selectable. A falling edge (H → L), rising edge (L → H) and both edges (H → L and L → H) on this pin can be recognized.

Point: A falling edge (H → L), rising edge (L → H) or both edges (H → L and L → H) can be used as a trigger for external 1 interrupt.

Specification: External 1 interrupt is generated by one edge (L → H) of an external signal.

Figure 4.2 shows an Example of External 1 Interrupt Operation, and Figure 4.4 shows an Example of External 1 Interrupt Setting.

4.3 Timer 1 Interrupt

Timer 1 permits a fixed-cycle interrupt to be used based on a set timer value.

Point: A fixed-cycle interrupt based on an underflow signal of timer 1 can be used.

Specification: A timer 1 interrupt is generated every 1 ms synchronously with the timing derived from the system clock frequency (= 4.0 MHz) by dividing it with the prescaler and timer 1.

Figure 4.5 shows an Example of Timer 1 Fixed-cycle Interrupt Setting.

4.4 Timer 2 Interrupt

Timer 2 permits a fixed-cycle interrupt to be used based on a set timer value.

Point: A fixed-cycle interrupt based on an underflow signal of timer 2 can be used.

Specification: A timer 2 interrupt is generated every 0.125 ms synchronously with the timing derived from the system clock frequency (= 2.0 MHz) by dividing it with timer 2.

Figure 4.6 shows an Example of Timer 2 Fixed-cycle Interrupt Setting.

4.5 Timer 3 Interrupt

Timer 3 permits a fixed-cycle interrupt to be used based on a set timer value.

Point: A fixed-cycle interrupt based on an underflow signal of timer 3 can be used.

Specification: A timer 3 interrupt is generated every 10 ms synchronously with the timing derived from the system clock frequency (= 6.0 MHz) by dividing it with the prescaler and timer 3.

Figure 4.7 shows an Example of Timer 3 Fixed-cycle Interrupt Setting.

4.6 Voltage Down Detection Circuit Interrupt

The voltage down detection circuit permits the use of an interrupt based on a drop of the power supply voltage below a predetermined value (V_{INT}).

Point: An interrupt based on a drop of the power supply voltage below a predetermined value (V_{INT}) can be used.

Specification: An interrupt is generated when the power supply voltage drops below a predetermined value (V_{INT}), and output of D0 port is inverted.

Figure 4.7 shows an Example of Timer 3 Fixed-cycle Interrupt Setting.

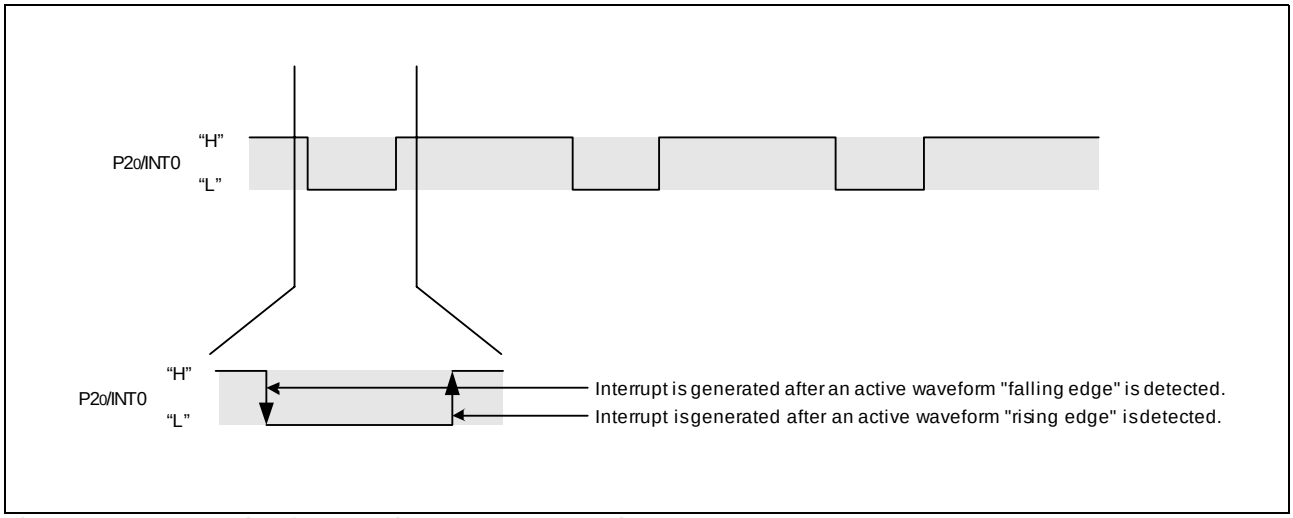


Figure 4.1 Example of External 0 Interrupt Operation

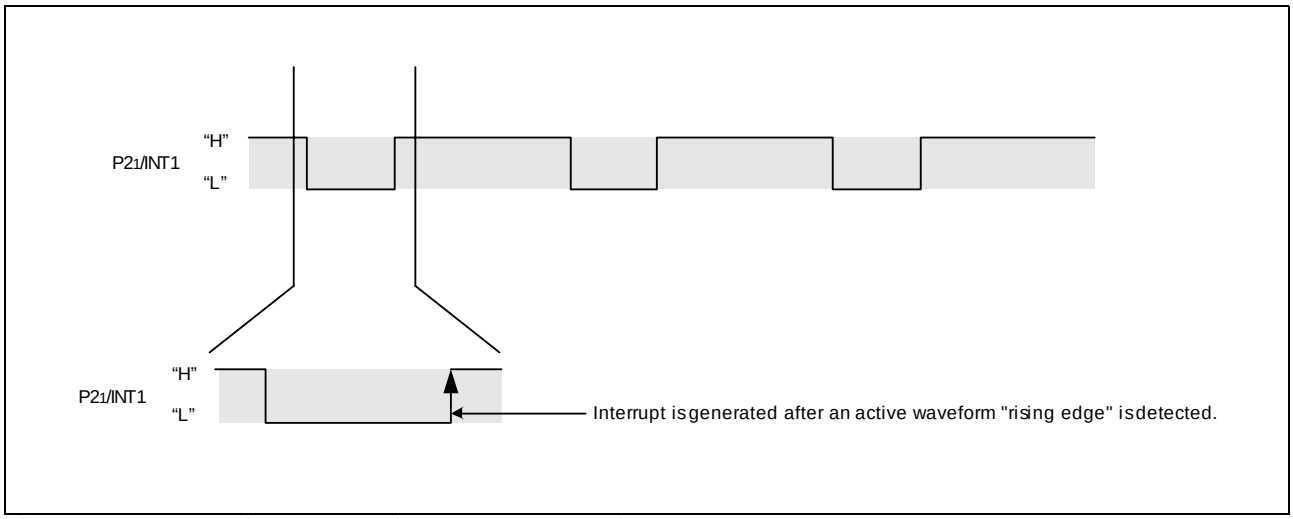
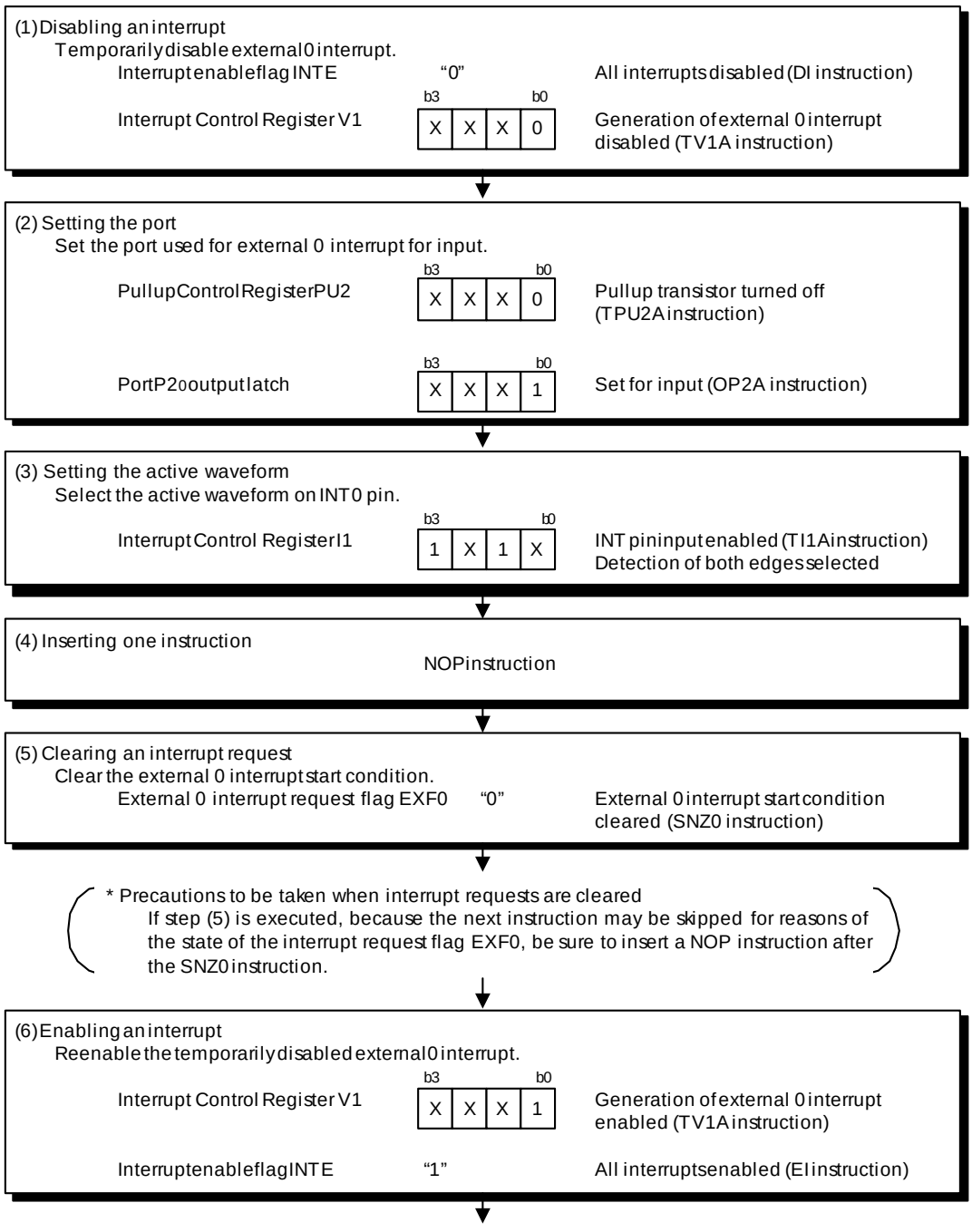


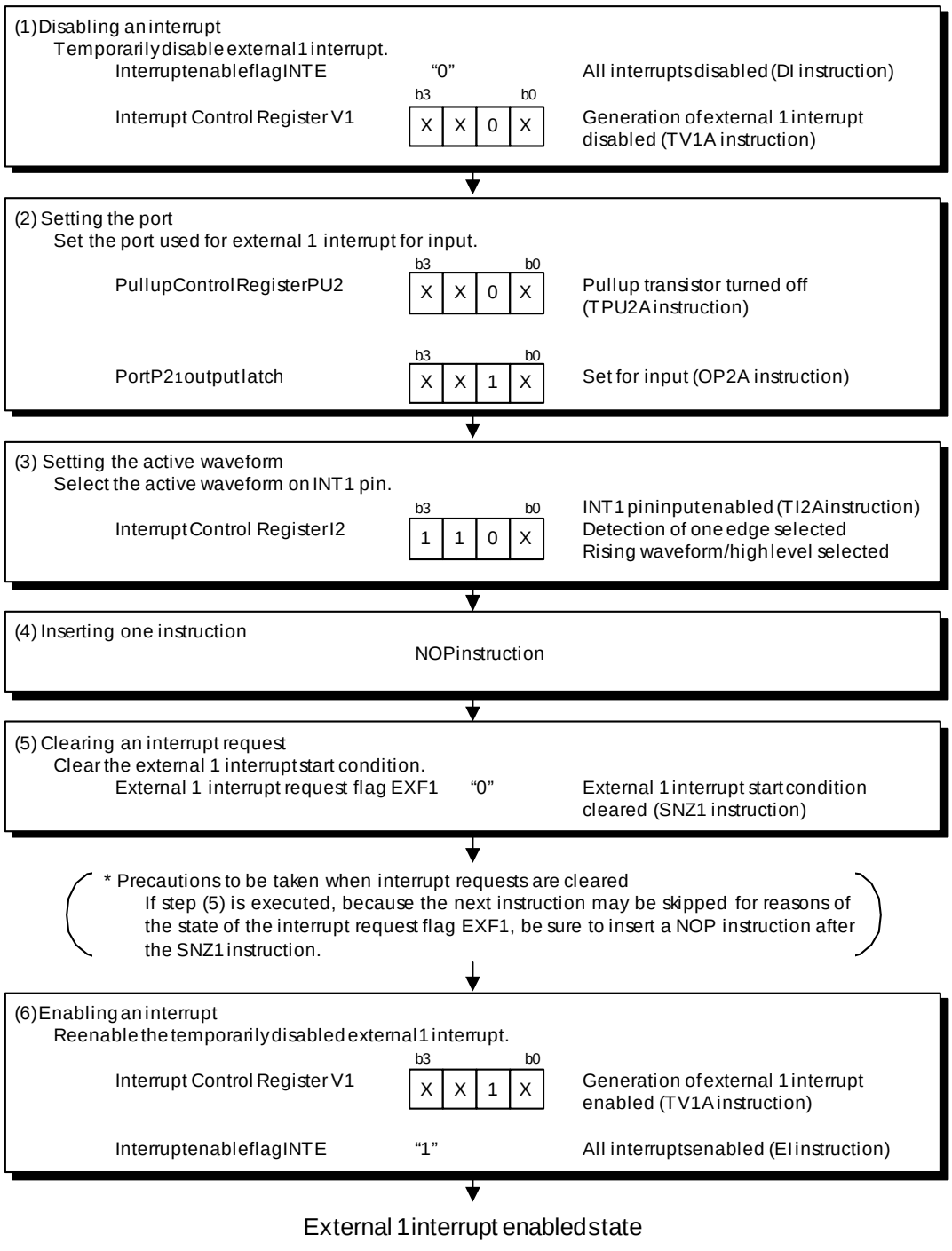
Figure 4.2 Example of External 1 Interrupt Operation



Note: The active waveform that constitutes the external 0 interrupt start condition requires that the signal levels before and after the change of state be retained for at least 4 system clock cycles each.

X: Don't care.

Figure 4.3 Example of External 0 Interrupt Setting



Note: The active waveform that constitutes the external 1 interrupt start condition requires that the signal levels before and after the change of state be retained for at least 4 system clock cycles each.

X: Don't care.

Figure 4.4 Example of External 1 Interrupt Setting

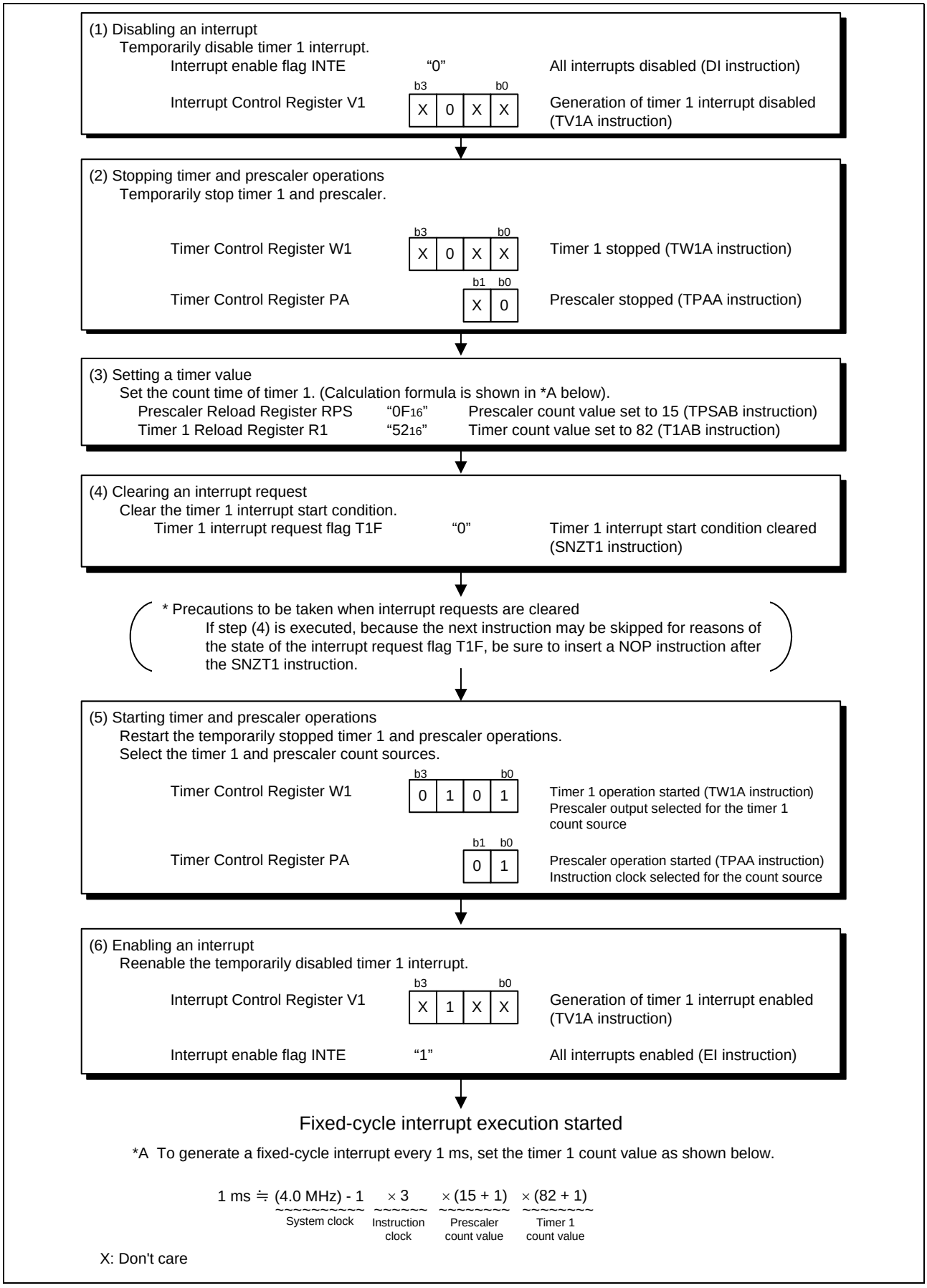


Figure 4.5 Example of Timer 1 Fixed-cycle Interrupt Setting

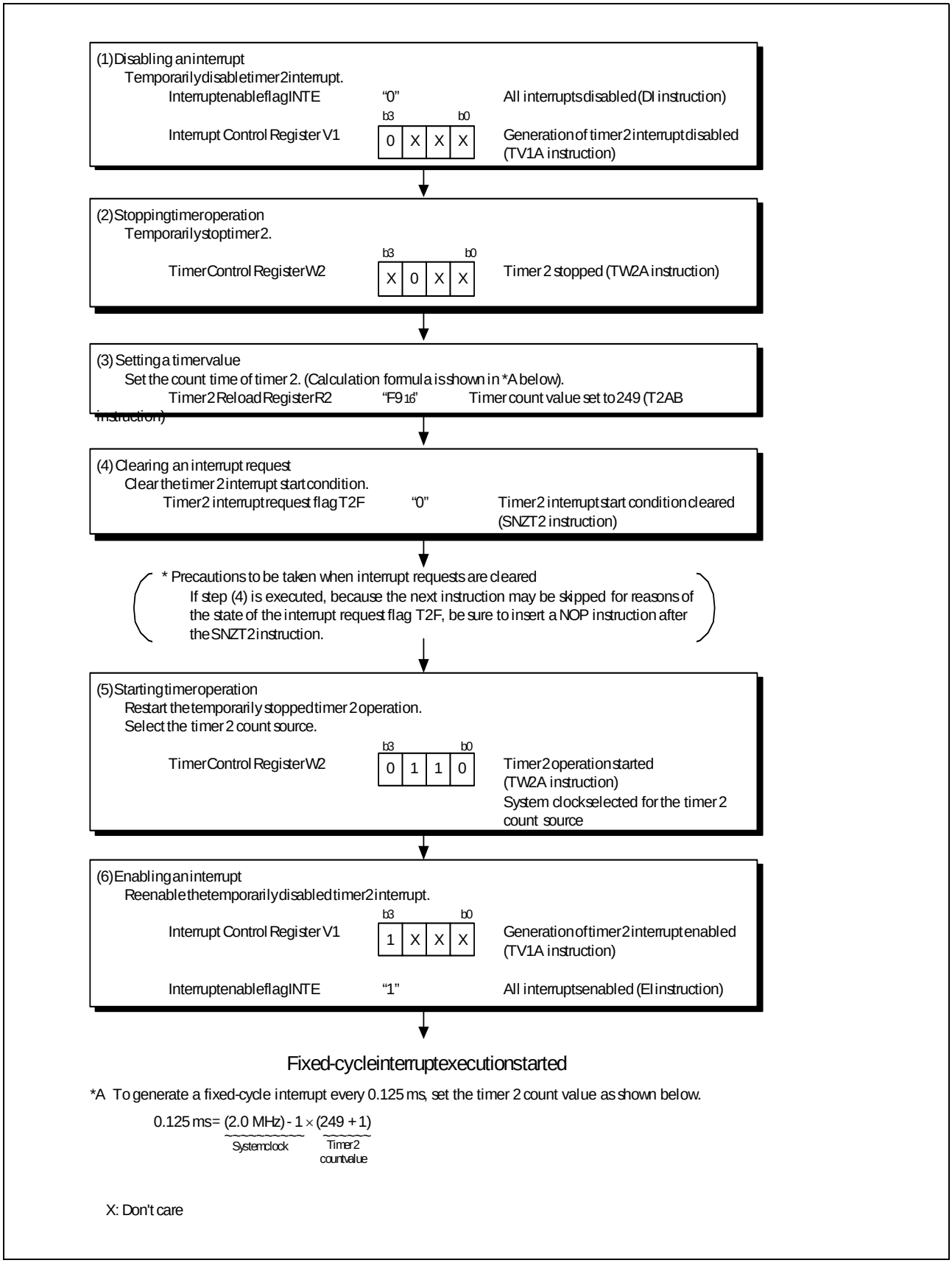


Figure 4.6 Example of Timer 2 Fixed-cycle Interrupt Setting

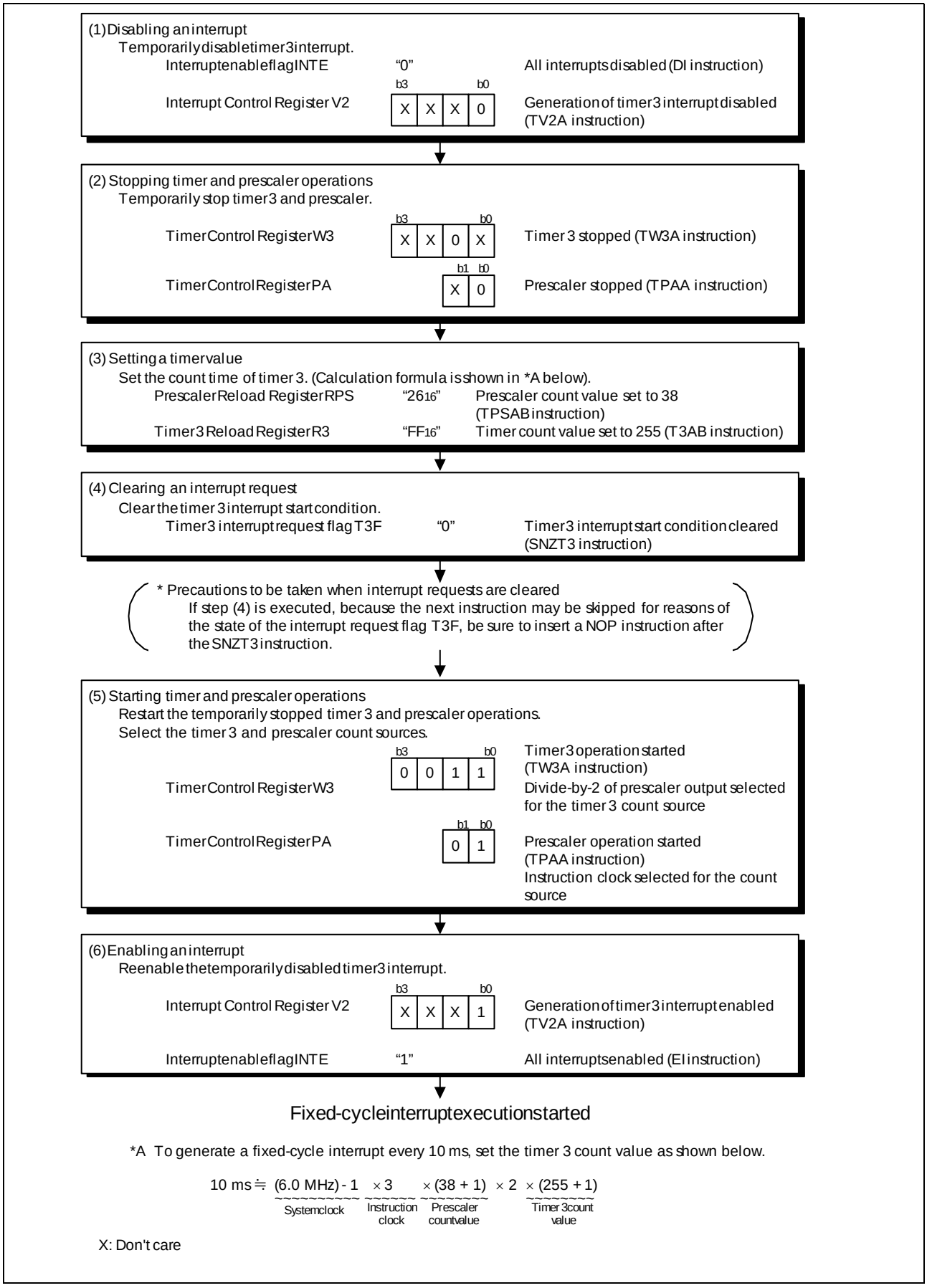


Figure 4.7 Example of Timer 3 Fixed-cycle Interrupt Setting

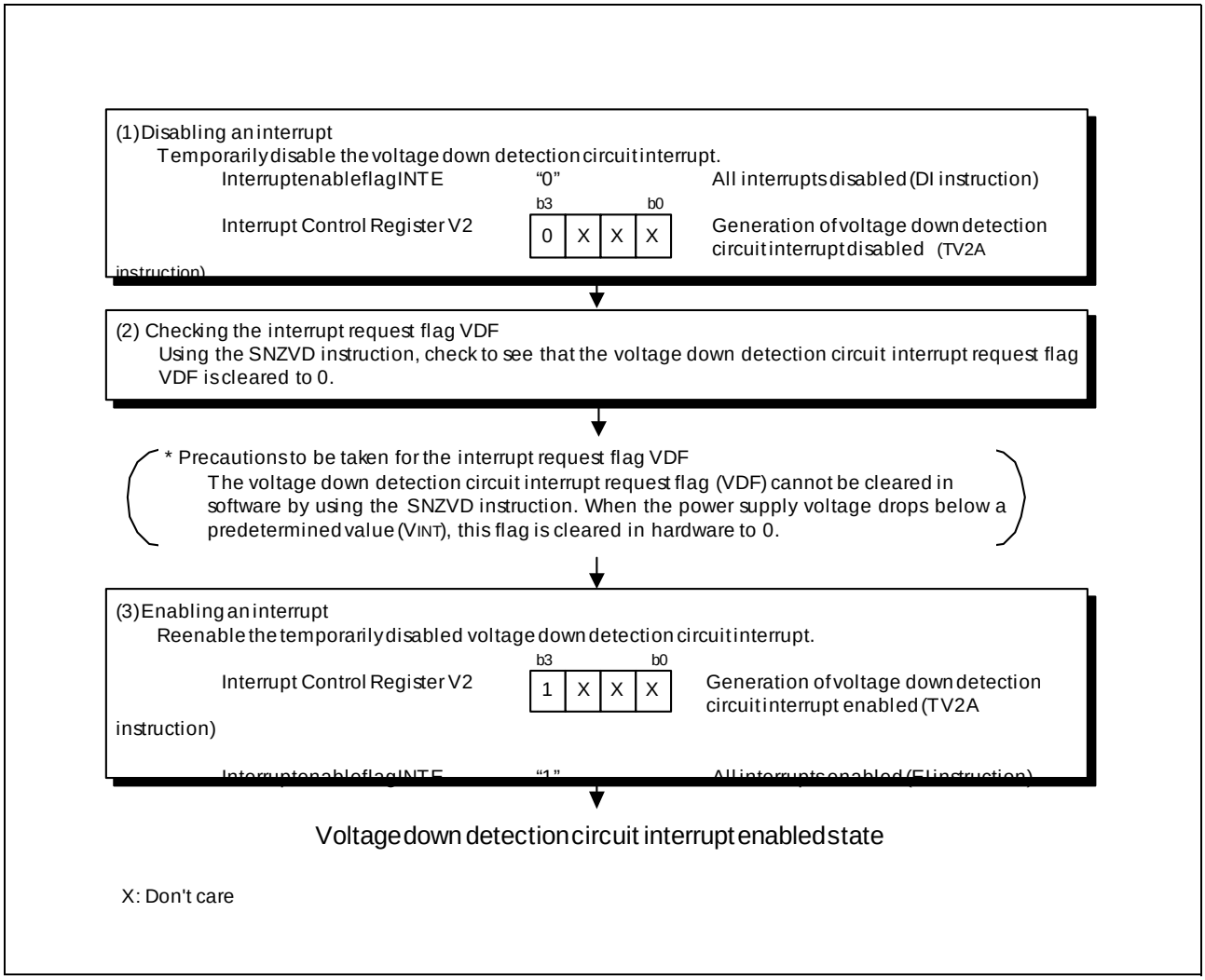


Figure 4.8 Example of Voltage Down Detection Circuit Interrupt Setting

5. Sample Programs

Sample programs are available from the Renesas Technology Web site. To download one, click the screen menu "Application Note" on the left side of 4571 group Web page.

6. Reference Documents

Data sheet
4571 Group Data Sheet

The latest version is available from the Renesas Technology Web site.

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Rev.	Date	Description	
		Page	Points
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