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4571 Group

Input/Output Ports

1. Abstract

This document shows an example of how to set the input/output ports of the 4571 group of Renesas microcomputers and an application example of using those pins.

2. Introduction

The application example explained in this document is applied for use with the microcomputers and under the conditions described below.

• Microcomputer: 4571 group

Please note that some sample programs available from Renesas involve manipulating the bits of unused functions for reasons of bit arrangement in the control registers. The values of these bits in a user system should be set to suit the usage condition of the system.

3. Input/Output Ports

3.1 Port P0

Port P0 permits 4 bits of data to be input or output to and from the port.

The key-on wakeup function and the pullup transistor function of this port can be turned on or off by setting up the register K0 and register PU0, respectively.

3.1.1 Port P0 Input/Output Method

- Input method

  For port P0i (i = 0-3) to be used, set the corresponding output latch to 1 using the OP0A instruction. If the output latch is set to 0, a low-level signal will be input.

  When the IAP0 instruction is executed, the pin state of port P0 is transferred to the register A.
- Output method

  The content of register A is output to port P0 by the OP0A instruction.

3.2 Port P1

Port P1 permits 4 bits of data to be input or output to and from the port.

The key-on wakeup function and the pullup transistor function of this port can be turned on or off by setting up the register K1 and register PU1, respectively.

3.2.1 Port P1 Input/Output Method

- Input method

  For port P1i (i = 0-3) to be used, set the corresponding output latch to 1 using the OP1A instruction. If the output latch is set to 0, a low-level signal will be input.

  When the IAP1 instruction is executed, the pin state of port P1 is transferred to the register A.
- Output method

  The content of register A is output to port P1 by the OP1A instruction.

3.3 Port P2

Port P2 permits 2 bits of data to be input or output to and from the port. Port $P2_0$ and $P2_1$ are shared with the interrupt input pins INT0 and INT1, respectively.

The key-on wakeup function and the pullup transistor function of this port can be turned on or off by setting up the registers $K2_1$ and $K2_0$ and registers $PU2_1$ and $PU2_0$, respectively.

Furthermore, the return condition or the active waveform level of the INT input pin-based key-on wakeup function can be selected by setting up the register L.

3.3.1 Port P2 Input/Output Method

- Input method

  For port P2i (i = 0, 1) to be used, set the corresponding output latch to 1 using the OP2A instruction. If the output latch is set to 0, a low-level signal will be input.

  When the IAP2 instruction is executed, the pin state of port P2 is transferred to the register A.
- Output method

  The content of register A is output to port P2 by the OP2A instruction.

3.4 Port P3

Port P3 permits 2 bits of data to be input or output to and from the port.

Furthermore, the port output mode can be selected between N-channel open-drain output and CMOS output by setting up the registers $FR0_0$ and $FR0_1$.

3.4.1 Port P3 Input/Output Method

- Input method

  For port P3i (i = 0-3) to be used, first set the corresponding registers $FR0_0$-$FR0_1$ to 0 and then set the corresponding output latch to 1 using the OP3A instruction. If the output latch is set to 0, a low-level signal will be input.

  When the IAP3 instruction is executed, the pin state of port P3 is transferred to the register A.

- Output method

  The content of register A is output to port P3 by the OP3A instruction.

  The output mode of this port can be selected between N-channel open-drain output and CMOS output bitwise by setting up the registers $FR0_0$-$FR0_1$.

3.5 Port D

Port D permits 5 bits of data to be input or output bitwise to and from the port. Port D_4 is shared with the CNTR0 pin.

Furthermore, the output mode of port D_0-D_3 can be selected between N-channel open-drain output and CMOS output by setting up the register FR1.

3.5.1 Port D Input/Output Method

Port D controls input/output of data bitwise, or one bit at a time. Therefore, if data is to be input/output on port D_0-D_4, one line of port D must first be selected with the data pointer register Y.

- Input method

  For port D_0-D_3 to be used, first set the corresponding register FR1i (i = 0-3) to 0 and then set the output latch of port Di (i = 0-3) to 1 using the SD instruction. If the output latch is set to 0, a low-level signal will be input.

  For port D_4, set its output latch to 1 using the SD instruction. If the output latch is set to 0, a low-level signal will be input.

  When the SZD instruction is executed, if the content of the port specified by the register Y is 0, the next instruction is skipped; if 1, the next instruction is executed.

- Output method

  Set the output level in the output latch using the SD and RD instructions.

  The output mode of port D_0-D_3 can be selected between N-channel open-drain output and CMOS output bitwise by setting up the register FR1.

  When the SD instruction is executed, the port pin goes to a high-impedance or a high-level state.

  When the CLD instruction is executed, all pins of port D go to a high-impedance or a high-level state.

  When the RD instruction is executed, the port pin goes to a low-level state.

Note 1: When using the SD and RD instructions, do not set any value equal to or greater than "01012" in the register Y.

Note 2: Port D_4 is shared with CNTR0. Therefore, if this port pin needs to be used as port D_4, set register W50 to 0.

3.6 Port C

Port C permits 1 bit of data to be output from the port. Port C is shared with the CNTR1 pin.

3.6.1 Port C Output Method

- Output method

  The output mode of this port is CMOS. When the SCP instruction is executed, the port pin goes to a high-level state.

  When the RCP instruction is executed, the port pin goes to a low-level state.

3.7 Port K

Port K permits 1 bit of data to be input through the port.

The key-on wakeup function of this port can be turned on or off by setting up the register $K2_2$.

3.7.1 Port K Input Method

- Input method

  When the IAK instruction is executed, the pin state of port K is transferred to the least significant bit (A_0) of the register A.

  The content of 3 high-order bits (A_3-A_1) of the register A is 0.

4. Related Registers

4.1 Timer Control Register W5

Table 4.1 shows the Bit Configuration of Timer Control Register W5.

For write to the register W5, first set a value in the register A and then use the TW5A instruction.

Furthermore, the TAW5 instruction may be used to transfer the content of the register W5 to the register A.

Table 4.1 Bit Configuration of Timer Control Register W5

Timer Control Register W5		When reset: 0000_2	When RAM backed-up: State retained	R/W TAW5/TW5A
$W5_3$	Timer 1 count start sync circuit select bit Note 2	0	Does not select timer 1 count start sync circuit	
		1	Selects timer 1 count start sync circuit	
$W5_2$	CNTR0 pin input count edge select bit	0	Falling edge	
		1	Rising edge	
$W5_1$	CNTR1 pin output auto control circuit select bit	0	Does not select CNTR1 pin output auto control circuit	
		1	Selects CNTR1 pin output auto control circuit	
$W5_0$	D_4/CNTR0 pin function select bit	0	D_4 output/CNTR0 input	
		1	D_4 input/CNTR0 output	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: This function is usable only when $I1_0 = 1$).
Note 3: : Unused bits during port setting

4.2 Pullup Control Register PU0

Table 4.2 shows the Bit Configuration of Pullup Control Register PU0.

For write to the register PU0, first set a value in the register A and then use the TPU0 instruction.

Furthermore, the TAPU0 instruction may be used to transfer the content of the register PU0 to the register A.

Table 4.2 Bit Configuration of Pullup Control Register PU0

Pullup Control Register PU0		When reset: 0000_2	When RAM backed-up: State retained	R/W TAPU0/TPU0A
$PU0_3$	Port $P0_3$ pullup transistor control bit	0	Turns pullup transistor off	
		1	Turns pullup transistor on	
$PU0_2$	Port $P0_2$ pullup transistor control bit	0	Turns pullup transistor off	
		1	Turns pullup transistor on	
$PU0_1$	Port $P0_1$ pullup transistor control bit	0	Turns pullup transistor off	
		1	Turns pullup transistor on	
$PU0_0$	Port $P0_0$ pullup transistor control bit	0	Turns pullup transistor off	
		1	Turns pullup transistor on	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

4.3 Pullup Control Register PU1

Table 4.3 shows the Bit Configuration of Pullup Control Register PU1.

For write to the register PU1, first set a value in the register A and then use the TPU1 instruction.

Furthermore, the TAPU1 instruction may be used to transfer the content of the register PU1 to the register A.

Table 4.3 Bit Configuration of Pullup Control Register PU1

Pullup Control Register PU1		When reset: 0000_2		When RAM backed-up: State retained	R/W TAPU1/TPU1A
$PU1_3$	Port $P1_3$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU1_2$	Port $P1_2$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU1_1$	Port $P1_1$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU1_0$	Port $P1_0$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

4.4 Pullup Control Register PU2

Table 4.4 shows the Bit Configuration of Pullup Control Register PU2.

For write to the register PU2, first set a value in the register A and then use the TPU2 instruction.

Furthermore, the TAPU2 instruction may be used to transfer the content of the register PU2 to the register A.

Table 4.4 Bit Configuration of Pullup Control Register PU2

Pullup Control Register PU2		When reset: 0000_2		When RAM backed-up: State retained	R/W TAPU2/TPU2A
$PU2_3$	Unused	0	This bit has no functions, but can be accessed for read/write.		
		1			
$PU2_2$	Unused	0	This bit has no functions, but can be accessed for read/write.		
		1			
$PU2_1$	Port $P2_1$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU2_0$	Port $P2_0$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during port setting

4.5 Port Output Mode Control Register FR0

Table 4.5 shows the Bit Configuration of Port Output Mode Control Register FR0.

For write to the register FR0, first set a value in the register A and then use the TFR0A instruction.

Table 4.5 Bit Configuration of Port Output Mode Control Register FR0

Port Output Mode Control Register FR0		When reset: 0000_2		When RAM backed-up: State retained	W TFR0A
$FR0_3$	Unused	0	This bit has no functions, but can be accessed for read/write.		
		1			
$FR0_2$	Unused	0	This bit has no functions, but can be accessed for read/write.		
		1			
$FR0_1$	Port $P3_1$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR0_0$	Port $P3_0$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		

Note 1: The letter W denotes “writable.”

Note 2: : Unused bits during port setting

4.6 Port Output Mode Control Register FR1

Table 4.6 shows the Bit Configuration of Port Output Mode Control Register FR1.

For write to the register FR1, first set a value in the register A and then use the TFR1A instruction.

Table 4.6 Bit Configuration of Port Output Mode Control Register FR1

Port Output Mode Control Register FR1		When reset: 0000_2		When RAM backed-up: State retained	W TFR1A
$FR1_3$	Port D_3 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_2$	Port D_2 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_1$	Port D_1 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_0$	Port D_0 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		

Note 1: The letter W denotes “writable.”

4.7 Key-on Wakeup Control Register K0

Table 4.7 shows the Bit Configuration of Key-on Wakeup Control Register K0.

For write to the register K0, first set a value in the register A and then use the TK0A instruction.

Furthermore, the TAK0 instruction may be used to transfer the content of the register K0 to the register A.

Table 4.7 Bit Configuration of Key-on Wakeup Control Register K0

Key-on Wakeup Control Register K0		When reset: 0000_2		When RAM backed-up: State retained	R/W TAK0/TK0A
$K0_3$	Port $P0_3$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K0_2$	Port $P0_2$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K0_1$	Port $P0_1$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K0_0$	Port $P0_0$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

4.8 Key-on Wakeup Control Register K1

Table 4.8 shows the Bit Configuration of Key-on Wakeup Control Register K1.

For write to the register K1, first set a value in the register A and then use the TK1A instruction.

Furthermore, the TAK1 instruction may be used to transfer the content of the register K1 to the register A.

Table 4.8 Bit Configuration of Key-on Wakeup Control Register K1

Key-on Wakeup Control Register K1		When reset: 0000_2		When RAM backed-up: State retained	R/W TAK1/TK1A
$K1_3$	Port $P1_3$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K1_2$	Port $P1_2$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K1_1$	Port $P1_1$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K1_0$	Port $P1_0$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

4.9 Key-on Wakeup Control Register K2

Table 4.9 shows the Bit Configuration of Key-on Wakeup Control Register K2.

For write to the register K2, first set a value in the register A and then use the TK2A instruction.

Furthermore, the TAK2 instruction may be used to transfer the content of the register K2 to the register A.

Table 4.9 Bit Configuration of Key-on Wakeup Control Register K2

Key-on Wakeup Control Register K2		When reset: 0000_2	When RAM backed-up: State retained	R/W TAK2/TK2A
$K2_3$	Unused	0	This bit has no functions, but can be accessed for read/write.	
		1		
$K2_2$	Port K key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
$K2_1$	Port $P2_1$ key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
$K2_0$	Port $P2_0$ key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: : Unused bits during port setting

4.10 Key-on Wakeup Control Register L1

Table 4.10 shows the Bit Configuration of Key-on Wakeup Control Register L1.

For write to the register L1, first set a value in the register A and then use the TL1A instruction.

Furthermore, the TAL1 instruction may be used to transfer the content of the register L1 to the register A.

Table 4.10 Bit Configuration of Key-on Wakeup Control Register L1

Key-on Wakeup Control Register L1		When reset: 0000_2	When RAM backed-up: State retained	R/W TAL1/TL1A
$L1_3$	INT1 pin return condition select bit	0	Level retured	
		1	Edge returned	
$L1_2$	INT1 pin active waveform level select bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
$L1_1$	INT0 pin return condition select bit	0	Level retured	
		1	Edge returned	
$L1_0$	INT0 pin key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

5. Port Application Example

5.1 Key Input by Key Scan

When N-channel open-drain output is selected for the output mode of port D and the internal pullup transistor of port P0 is used, a key matrix can be configured by connecting an external circuit comprised of only keys to the chip.

Point: The external component needed for this application consists of only keys.
Specification: Port D outputs a low-level signal, and port P0 accepts 16 keys as its input.

Figure 5.1 shows an Example of a Key Matrix Circuit. Figue 5.2 shows Key Scan Input Timing.

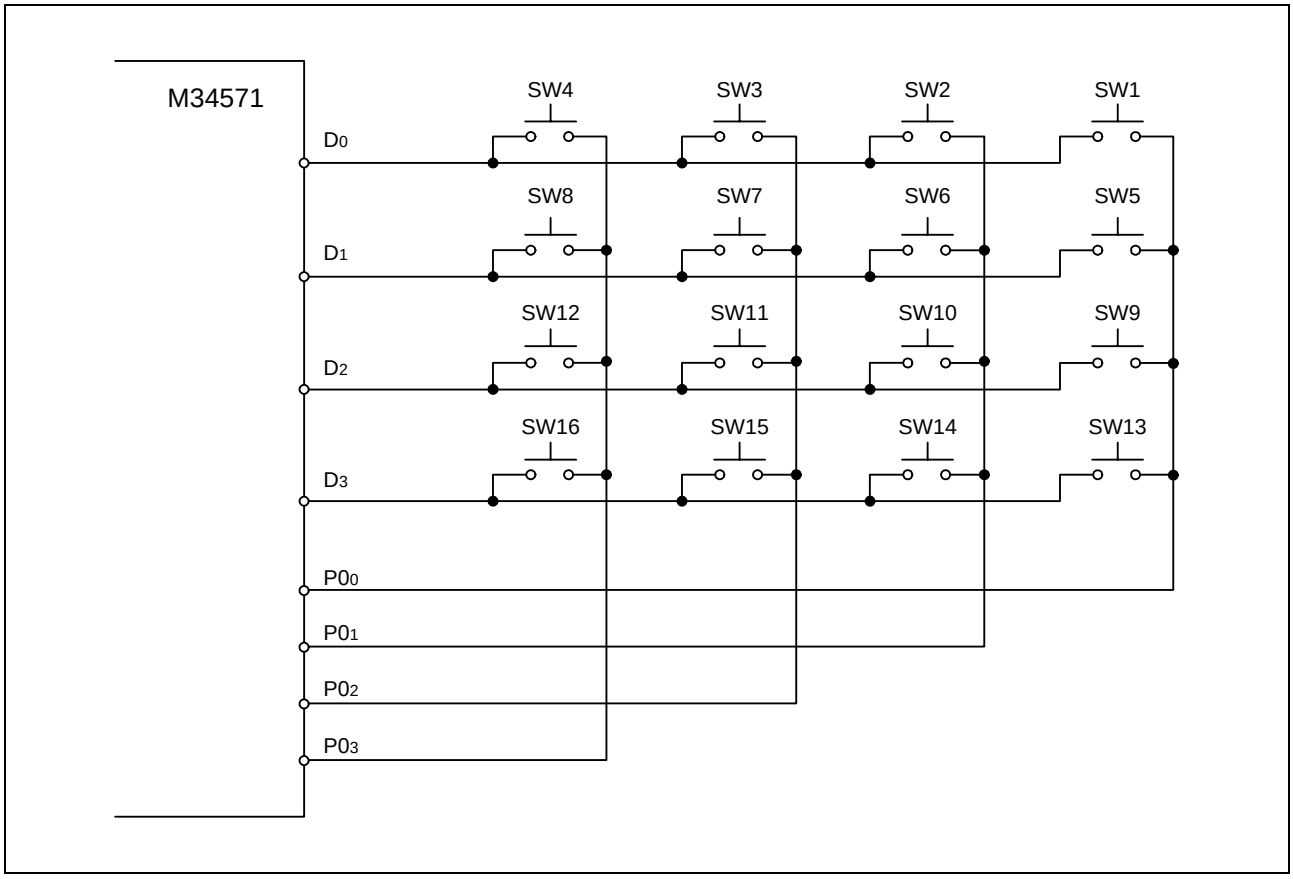
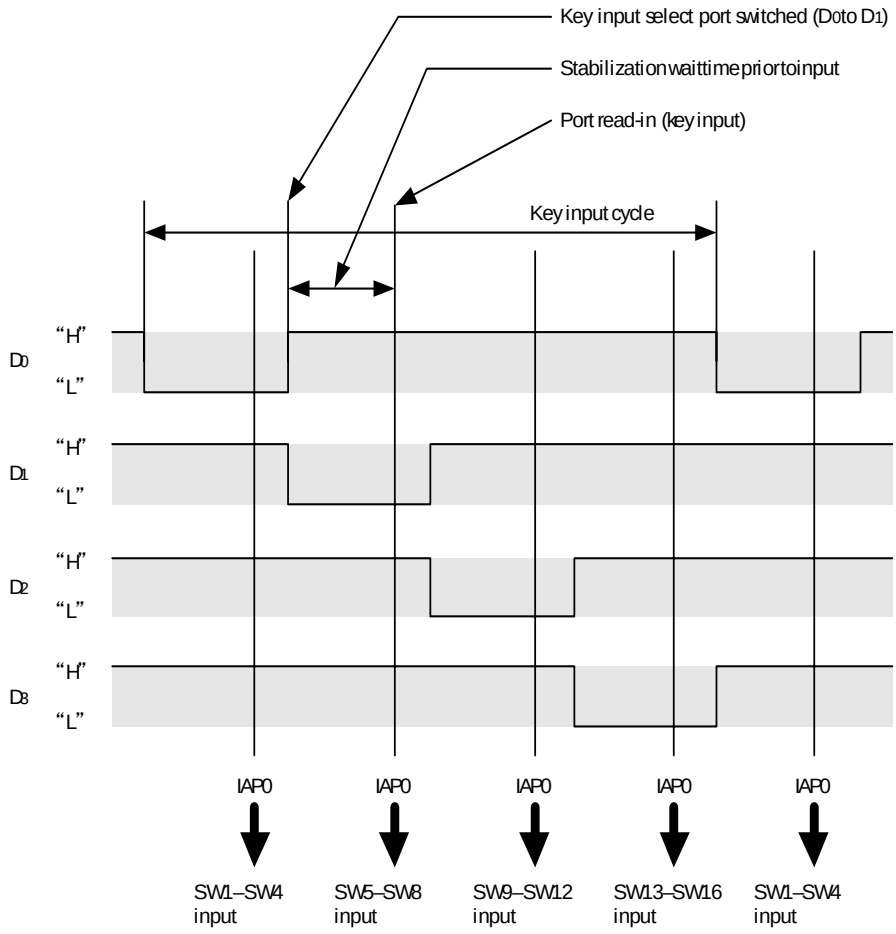


Figure 5.1 Example of a Key Matrix Circuit



Note: High-level output on port D goes to a high-impedance state.

Figue 5.2 Key Scan Input Timing

6. Reference Documents

Data sheet
4571 Group Data Sheet

The latest version is available from the Renesas Technology Web site.

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Rev.	Date	Description	
		Page	Points
1.00	2006.08.01	-	First edition issued

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