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## 455A Group

### LCD Display Function

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#### 1. Abstract

This document presents the method for using the LCD display function of the 455A-group microcomputers and shows an application example.

#### 2. Introduction

The application example explained in this document applies for use with the microcomputers and under the conditions described below.

- Microcomputer : 455A group
- Oscillator frequency : 32.768 kHz as sub-clock f(XCIN), however
- System clock : Used in through mode (not frequency divided)

### 3. Related Registers

#### 3.1 LCD Control Register L1

Table 3.1 shows the bit configuration of LCD Control Register L1.

For write to the register L1, first set a value in the register A and then use the TL1A instruction.

Furthermore, the TAL1 instruction may be used to transfer the content of register L1 to the register A.

Table 3.1 Bit Configuration of LCD Control Register L1

LCD Control Register L1		When reset: 0000 <sub>2</sub>		When powered down: State retained		R/W TAL1/TL1A	
L13	LCD power supply internal dividing resistor select bit <sup>Note 2</sup>	0	2r × 3, 2r × 2				
		1	r × 3, r × 2				
L12	LCD control bit	0	Stop (turned off)				
		1	Start				
L11	LCD duty cycle/bias select bit	L11	L10	Duty cycle		Bias	
		0	0	Use prohibited		Use prohibited	
		0	1	1/2		1/2	
		1	0	1/3		1/3	
L10		1	1	1/4		1/3	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: When 1/3 bias is selected, a “x3” resistor is used; when 1/2 bias is selected, a “x2” resistor is used.

#### 3.2 LCD Control Register L2

Table 3.2 shows the bit configuration of LCD Control Register L2.

For write to the register L2, first set a value in the register A and then use the TL2A instruction.

Table 3.2 Bit Configuration of LCD Control Register L2

LCD Control Register L2		When reset: 0000 <sub>2</sub>		When powered down: State retained		W TL2A	
L23	SEG0/VLC3 pin function select bit <sup>Note 2</sup>	0	SEG0				
		1	VLC3				
L22	SEG1/VLC2 pin function select bit <sup>Note 3</sup>	0	SEG1				
		1	VLC2				
L21	SEG2/VLC1 pin function select bit <sup>Note 3</sup>	0	SEG2				
		1	VLC1				
L20	LCD power supply internal dividing resistor control bit	0	Enables internal dividing resistor				
		1	Disables internal dividing resistor				

Note 1: The letter W denotes “writable.”

Note 2: When SEG0 pin is selected, VLC3 is connected to VDD internally in the chip.

Note 3: When SEG1 and SEG2 pins are selected, always be sure to use the internal dividing resistor.

### 3.3 LCD Control Register L3

Table 3.3 shows the bit configuration of LCD Control Register L3.

For write to the register L3, first set a value in the register A and then use the TL3A instruction.

Table 3.3 Bit Configuration of LCD Control Register L3

LCD Control Register L3		When reset: 11112	When powered down: State retained	W TL3A
L33	P23/SEG27 pin function select bit	0	SEG27	
		1	P23	
L32	P22/SEG26 pin function select bit	0	SEG26	
		1	P22	
L31	P21/SEG25 pin function select bit	0	SEG25	
		1	P21	
L30	P20/SEG24 pin function select bit	0	SEG24	
		1	P20	

Note 1: The letter W denotes “writable.”

### 3.4 LCD Control Register C1

Table 3.4 shows the bit configuration of LCD Control Register C1.

For write to the register C1, first set a value in the register A and then use the TC1A instruction.

Table 3.4 Bit Configuration of LCD Control Register C1

LCD Control Register C1		When reset: 11112	When powered down: State retained	W TC1A
C13	P03/SEG19 pin function select bit	0	SEG19	
		1	P03	
C12	P02/SEG18 pin function select bit	0	SEG18	
		1	P02	
C11	P01/SEG17 pin function select bit	0	SEG17	
		1	P01	
C10	P00/SEG16 pin function select bit	0	SEG16	
		1	P00	

Note 1: The letter W denotes “writable.”

### 3.5 LCD Control Register C2

Table 3.5 shows the bit configuration of LCD Control Register C2.

For write to the register C2, first set a value in the register A and then use the TC2A instruction.

Table 3.5 Bit Configuration of LCD Control Register C2

LCD Control Register C2		When reset: 11112	When powered down: State retained	W TC2A
C23	P13/SEG23 pin function select bit	0	SEG23	
		1	P13	
C22	P12/SEG22 pin function select bit	0	SEG22	
		1	P12	
C21	P11/SEG21 pin function select bit	0	SEG21	
		1	P11	
C20	P10/SEG20 pin function select bit	0	SEG20	
		1	P10	

Note 1: The letter W denotes “writable.”

### 3.6 LCD Control Register C3

Table 3.6 shows the bit configuration of LCD Control Register C3.

For write to the register C3, first set a value in the register A and then use the TC3A instruction.

Table 3.6 Bit Configuration of LCD Control Register C3

LCD Control Register C3		When reset: 11112	When powered down: State retained	W TC3A
C33	P33/SEG31 pin function select bit	0	SEG31	
		1	P33	
C32	P32/SEG30 pin function select bit	0	SEG30	
		1	P32	
C31	P31/SEG29 pin function select bit	0	SEG29	
		1	P31	
C30	P30/SEG28 pin function select bit	0	SEG28	
		1	P30	

Note 1: The letter W denotes “writable.”

### 3.7 Timer Control Register W3

Table 3.7 shows the bit configuration of Timer Control Register W3.

For write to the register W3, first set a value in the register A and then use the TW3A instruction.

Furthermore, the TAW3 instruction may be used to transfer the content of register W3 to the register A.

Table 3.7 Bit Configuration of Timer Control Register W3

Timer Control Register W3		When reset: 0000 <sub>2</sub>		When powered down: State retained		R/W TAW3/TW3A	
W3 <sub>3</sub>	Timer 3 control bit	0	Stop (initial state)				
		1	Start				
W3 <sub>2</sub>	Timer 3 count value select bit	W3 <sub>2</sub>	W3 <sub>1</sub>	W3 <sub>0</sub>	Count value		
		0	0	0	Generates underflow every 512 counts		
0		0	1	Generates underflow every 1,024 counts			
0		1	0	Generates underflow every 2,048 counts			
0		1	1	Generates underflow every 4,096 counts			
1		0	0	Generates underflow every 8,192 counts			
1		0	1	Generates underflow every 16,384 counts			
1		1	0	Generates underflow every 32,768 counts			
W3 <sub>0</sub>		1	1	1	Generates underflow every 65,536 counts		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

### 3.8 Timer Control Register W4

Table 3.8 shows the bit configuration of Timer Control Register W4.

For write to the register W4, first set a value in the register A and then use the TW4A instruction.

Furthermore, the TAW4 instruction may be used to transfer the content of register W4 to the register A.

Table 3.8 Bit Configuration of Timer Control Register W4

Timer Control Register W4		When reset: 0000 <sub>2</sub>		When powered down: State retained		R/W TAW4/TW4A	
W4 <sub>3</sub>	Timer LC control bit	0	Stop (state retained)				
		1	Start				
W4 <sub>2</sub>	Timer LC count source select bit	0	Bit 4 of timer 3 (T3 <sub>4</sub> )				
		1	System clock (STCK)				
W4 <sub>1</sub>	CNTR pin output auto control circuit select bit	0	Deselects CNTR pin output auto control circuit				
		1	Selects CNTR pin output auto control circuit				
W4 <sub>0</sub>	CNTR pin input count edge select bit	0	Falling edge				
		1	Rising edge				

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during LCD display function setting.

### 3.9 Timer Control Register W5

Table 3.9 shows the bit configuration of the Timer Control Register W5.

For write to the register W5, first set a value in the register A and then use the TW5A instruction.

Furthermore, the TAW5 instruction may be used to transfer the content of register W5 to the register A.

Table 3.9 Bit Configuration of Timer Control Register W5

Timer Control Register W5		When reset: 0000 <sub>2</sub>		When powered down: State retained	R/W TAW5/TW5A
W53	Unused	0	This bit has no functions, but can be accessed for read/write.		
		1	This bit has no functions, but can be accessed for read/write.		
W52	Unused	0	This bit has no functions, but can be accessed for read/write.		
		1	This bit has no functions, but can be accessed for read/write.		
W51	Timer 3 count source select bit	W51	W50	Count source	
		0	0	XcIN input	
0		1	ORCLK input		
1		0	Low-speed on-chip oscillator input (LSOCO)		
W50		1	1	High-speed on-chip oscillator input (HSOCO)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during LCD display function setting.



## 4. Application Example for the LCD Display Function

### 4.1 LCD Display

The LCD display function permits display of up to 4 common × 32 segment = 128 pixels to be controlled.

**Point** : Data can easily be displayed on LCD using the LCD display function.

**Specification** : Data is displayed on LCD at a 1/4 duty cycle and 1/3 bias using the LCD display panel that is shown as an example below. The frame frequency is set to 85.3 Hz using timer LC for the LCD clock source, bit 4 of timer 3 for the timer LC clock source and the sub-clock  $f(XCIN) = 32.768$  kHz for the timer 3 clock source, respectively. In the sample program, a string “M3455A” is displayed on the LCD panel shown below.

Figure 4.1 shows an example of an LCD display panel. Figure 4.2 shows an example of RAM arrangement for LCD display. Figure 4.3 shows an example of a segment arrangement for an LCD display panel. Figure 4.4 shows an example of how to set the registers for LCD display.

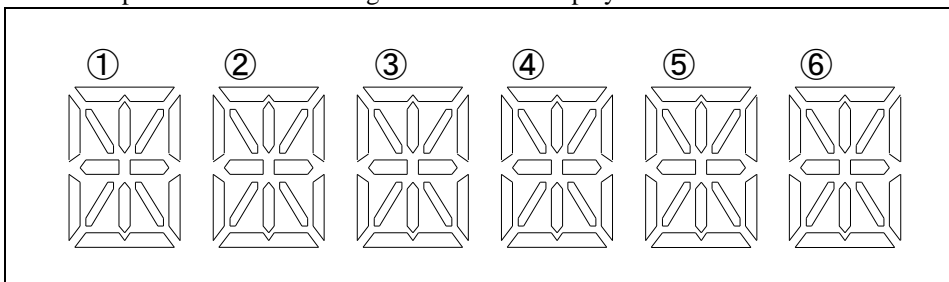


Figure 4.1 Example of an LCD Display Panel

Register Z	1																
Register X	12				13				14				15				
Register Y	bit	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8		SEG0	SEG0	SEG0	SEG0	SEG8	SEG8	SEG8	SEG8	SEG16	SEG16	SEG16	SEG16	SEG24	SEG24	SEG24	SEG24
9		SEG1	SEG1	SEG1	SEG1	SEG9	SEG9	SEG9	SEG9	SEG17	SEG17	SEG17	SEG17	SEG25	SEG25	SEG25	SEG25
10		SEG2	SEG2	SEG2	SEG2	SEG10	SEG10	SEG10	SEG10	SEG18	SEG18	SEG18	SEG18	SEG26	SEG26	SEG26	SEG26
11		SEG3	SEG3	SEG3	SEG3	SEG11	SEG11	SEG11	SEG11	SEG19	SEG19	SEG19	SEG19	SEG27	SEG27	SEG27	SEG27
12		SEG4	SEG4	SEG4	SEG4	SEG12	SEG12	SEG12	SEG12	SEG20	SEG20	SEG20	SEG20	SEG28	SEG28	SEG28	SEG28
13		SEG5	SEG5	SEG5	SEG5	SEG13	SEG13	SEG13	SEG13	SEG21	SEG21	SEG21	SEG21	SEG29	SEG29	SEG29	SEG29
14		SEG6	SEG6	SEG6	SEG6	SEG14	SEG14	SEG14	SEG14	SEG22	SEG22	SEG22	SEG22	SEG30	SEG30	SEG30	SEG30
15		SEG7	SEG7	SEG7	SEG7	SEG15	SEG15	SEG15	SEG15	SEG23	SEG23	SEG23	SEG23	SEG31	SEG31	SEG31	SEG31
COM		COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0

Figure 4.2 Example of RAM Arrangement for LCD Display

Register Z	1												
Register X	12				13				14				
Register Y	bit	3	2	1	0	3	2	1	0	3	2	1	0
8		①-d	①-c	①-b	①-a	③-d	③-c	③-b	③-a	⑤-d	⑤-c	⑤-b	⑤-a
9		①-h	①-g	①-f	①-e	③-h	③-g	③-f	③-e	⑤-h	⑤-g	⑤-f	⑤-e
10		①-k	①-j		①-i	③-k	③-j		③-i	⑤-k	⑤-j		⑤-i
11		①-n	①-l		①-m	③-n	③-l		③-m	⑤-n	⑤-l		⑤-m
12		②-d	②-c	②-b	②-a	④-d	④-c	④-b	④-a	⑥-d	⑥-c	⑥-b	⑥-a
13		②-h	②-g	②-f	②-e	④-h	④-g	④-f	④-e	⑥-h	⑥-g	⑥-f	⑥-e
14		②-k	②-j		②-i	④-k	④-j		④-i	⑥-k	⑥-j		⑥-i
15		②-n	②-l		②-m	④-n	④-l		④-m	⑥-n	⑥-l		⑥-m
COM		COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0

Figure 4.3 Example of a Segment Arrangement for an LCD Display Panel

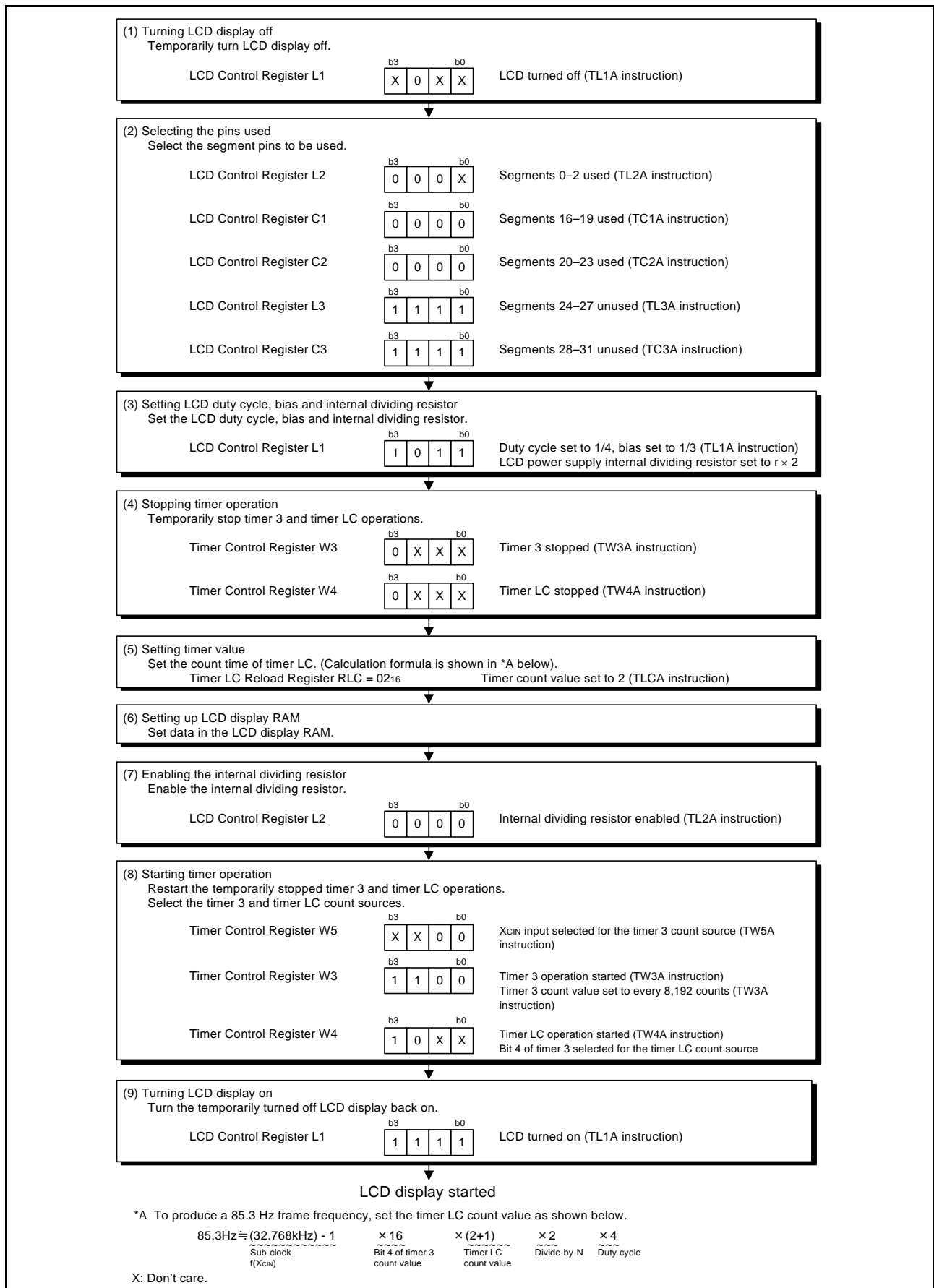


Figure 4.4 Example of LCD Display Setting

## 5. Reference Documents

Data sheet

455A Group Data Sheet

(The latest version is available from the Renesas Technology Web site.)

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(The latest information is available from the Renesas Technology Web site.)

## 6. Sample Programs

Sample programs are available from the Renesas Technology Web site.

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