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## 455A Group

### Input/Output Ports

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#### 1. Abstract

This document presents the method for using the input/output pins of the 455A-group microcomputers and shows an application example.

#### 2. Introduction

The application example explained in this document applies for use with the microcomputers and under the conditions described below.

- Microcomputer : 455A group

### 3. Input/Output Ports

#### 3.1 Port P0

Port P0 permits 4 bits of data to be input or output to and from the port. Ports P00–P03 are shared with LCD segment output pins SEG16–SEG19. The pin function of these ports can be chosen to be input/output ports or LCD segment output pins by setting up the register C1.

The key-on wakeup function and the pullup transistor function of port P0 can be turned on or off by setting up the registers K00–K01 and register PU00–PU01, respectively.

Furthermore, the output mode of this port can be chosen to be N-channel open-drain output or CMOS output by setting up the registers FR00–FR01.

##### 3.1.1 Port P0 Input/Output Method

- Input method  
 For the ports P00–P03 used, set the corresponding register FR0i (i = 0–1) to 0 and then set the output latch of port P0i (i = 0–3) to 1 using the OP0A instruction. If the output latch is set to 0, a low-level signal will be input.  
 When the IAP0 instruction is executed, the pin state of port P0 is transferred to the register A.
- Output method  
 The content of register A is output to port P0 by the OP0A instruction.  
 The output type of this port can be chosen to be N-channel open-drain output or CMOS output in 2-bit units by setting up the registers FR00–FR01.

#### 3.2 Port P1

Port P1 permits 4 bits of data to be input or output to and from the port. Ports P100–P13 are shared with LCD segment output pins SEG20–SEG23. The pin function of these ports can be chosen to be input/output ports or LCD segment output pins by setting up the register C2.

The key-on wakeup function and the pullup transistor function of port P1 can be turned on or off by setting up the registers K02–K03 and register PU02–PU03, respectively.

Furthermore, the output mode of this port can be chosen to be N-channel open-drain output or CMOS output by setting up the registers FR02–FR03.

##### 3.2.1 Port P1 Input/Output Method

- Input method  
 For the ports P10–P13 used, set the corresponding register FR0i (i = 2–3) to 0 and then set the output latch of port P1i (i = 0–3) to 1 using the OP1A instruction. If the output latch is set to 0, a low-level signal will be input.  
 When the IAP1 instruction is executed, the pin state of port P1 is transferred to the register A.
- Output method  
 The content of register A is output to port P1 by the OP1A instruction.  
 The output type of this port can be chosen to be N-channel open-drain output or CMOS output in 2-bit units by setting up the registers FR02–FR03.

### 3.3 Port P2

Port P2 permits 4 bits of data to be input or output to and from the port. Ports P20–P23 are shared with LCD segment output pins SEG24–SEG27. The pin function of these ports can be chosen to be input/output ports or LCD segment output pins by setting up the register L3.

The key-on wakeup function and the pullup transistor function of port P2 can be turned on or off by setting up the register K1 and register PU1, respectively.

Furthermore, the output mode of this port can be chosen to be N-channel open-drain output or CMOS output by setting up the register FR3.

#### 3.3.1 Port P2 Input/Output Method

- Input method

For the ports P20–P23 used, set the corresponding register FR3i (i = 0–3) to 0 and then set the output latch of port P2i (i = 0–3) to 1 using the OP2A instruction. If the output latch is set to 0, a low-level signal will be input.

When the IAP2 instruction is executed, the pin state of port P2 is transferred to the register A.

- Output method

The content of register A is output to port P2 by the OP2A instruction.

The output type of this port can be chosen to be N-channel open-drain output or CMOS output in 1-bit units by setting up the registers FR30–FR33.

### 3.4 Port P3

Port P3 permits 4 bits of data to be input or output to and from the port. Ports P30–P33 are shared with LCD segment output pins SEG28–SEG31. The pin function of these ports can be chosen to be input/output ports or LCD segment output pins by setting up the register C3.

The key-on wakeup function and the pullup transistor function of port P3 can be turned on or off by setting up the register K2i (i = 2–3) and the register PU2, respectively.

Furthermore, the output mode of this port can be chosen to be N-channel open-drain output or CMOS output by setting up the registers FR22–FR23.

#### 3.4.1 Port P3 Input/Output Method

- Input method

For the ports P30–P33 used, set the corresponding register FR2i (i = 2–3) to 0 and then set the output latch of port P3i (i = 0–3) to 1 using the OP3A instruction. If the output latch is set to 0, a low-level signal will be input.

When the IAP3 instruction is executed, the pin state of port P3 is transferred to the register A.

- Output method

The content of register A is output to port P3 by the OP3A instruction.

The output type of this port can be chosen to be N-channel open-drain output or CMOS output in 2-bit units by setting up the registers FR22–FR23.

### 3.5 Port D

Port D consists of eight bitwise input/output ports. Ports D5, D6 and D7 are shared with the INT, XCIN and XCOUT pins, respectively.

Furthermore, the output mode of ports D0–D5 can be chosen to be N-channel open-drain output or CMOS output by setting up the registers FR1 and FR20–FR21.

When the CLD instruction is executed, all pins of port D go to a high-impedance state or a high-level state depending on how the registers FR1i (i=0–3) and FR2i (i=0–1) are set.

#### 3.5.1 Port D0–D5 Input/Output Method

Ports D0–D5 control input/output of data bitwise, or one bit at a time. Therefore, if data is to be input/output on ports D0–D5, one line of port D must first be selected with the data pointer register Y.

- Input method

For the ports D0–D5 used, set the corresponding register FR1i (i = 0–3) and FR2i (i = 0–1) to 0 and then set the output latch of port Di (i = 0–5) to 1 using the SD instruction. If the output latch is set to 0, a low-level signal will be input.

When the SZD instruction is executed, if the content of the port specified by the register Y is 0, the next instruction is skipped; if 1, the next instruction is executed.

- Output method

Set the output level of ports D0–D5 in each corresponding output latch using the SD and RD instructions.

The output modes of ports D0–D3 and ports D4–D5 can be chosen to be N-channel open-drain output or CMOS output in 1-bit units by setting up the register FR1 and registers FR20–FR21, respectively.

When the SD instruction is executed, the port pin goes to a high-impedance or a high-level state depending on how the registers FR1i (i = 0–3) and FR2i (i = 0–1) are set.

When the RD instruction is executed, the port pin goes to a low-level state.

#### 3.5.2 Port D6–D7 Input/Output Method

Ports D6–D7 control input/output of data bitwise, or one bit at a time. Therefore, if data is to be input/output on ports D6–D7, one line of port D must first be selected with the data pointer register Y.

Ports D6–D7 are shared with the XCIN and XCOUT pins, respectively. To use these shared facilities as ports D6–D7, set the register RG2 to 1.

- Input method

Set the output latch corresponding to the port pin to be used D6–D7 to 1 by using the SD instruction. If the output latch for the port is set to 0, a low signal will be input.

If when the SZD instruction is executed the content of the port specified by register Y is 0, the next instruction is skipped; if 1, the next instruction is executed.

- Output method

Set the output level of ports D6–D7 in each corresponding output latch using the SD and RD instructions.

When the SD instruction is executed, the port pin goes to a high-impedance state.

When the RD instruction is executed, the port pin goes to a low-level state.

Note: If the SD and RD instructions are used, do not set any value equal to or greater than “10002” in the register Y.

### 3.6 Port C

Port C permits 1 bit of data to be output from the port. Port C is shared with the CNTR pin. However, if the CNTR pin is used for input, no data can be output from this port.

#### 3.6.1 Port C Output Method

- Output method

The output mode of this port is CMOS. When the SCP instruction is executed, the port pin goes to a high-level state.

When the RCP instruction is executed, the port pin goes to a low-level state.

Note: Actually output from the pin is a logical OR of CNTR output and port C output.

## 4. Related Registers

### 4.1 Timer Control Register W1

Table 4.1 shows the bit configuration of Timer Control Register W1.

For write to the register W1, first set a value in the register A and then use the TW1A instruction.

Furthermore, the TAW1 instruction may be used to transfer the content of register W1 to the register A.

Table 4.1 Bit Configuration of Timer Control Register W1

Timer Control Register W1		When reset: 0000 <sub>2</sub>	When powered down: State retained	R/W TAW1/TW1A
W13	Timer 1 count auto stop circuit select bit Note 2	0	Deselects timer 1 count auto stop circuit	
		1	Selects timer 1 count auto stop circuit	
W12	Timer 1 control bit	0	Stop (state retained)	
		1	Start	
W11	Timer 1 count source select bit Note 3	W11	W10	Count source
		0	0	PWM signal (PWMOUT)
		0	1	Prescaler output (ORCLK)
		1	0	Timer 3 underflow signal (T3UDF)
W10		1	1	CNTR input

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: This function is usable only when the timer 1 count start synchronizing circuit is selected (I10 = 1).

Note 3: If CNTR input is selected for the timer 1 count source, port C output is disabled.

Note 4: : Unused bits during port setting.

### 4.2 Timer Control Register W2

Table 4.2 shows the bit configuration of Timer Control Register W2.

For write to the register W2, first set a value in the register A and then use the TW2A instruction.

Furthermore, the TAW2 instruction may be used to transfer the content of register W2 to the register A.

Table 4.2 Bit Configuration of Timer Control Register W2

Timer Control Register W2		When reset: 0000 <sub>2</sub>	When powered down: 0000 <sub>2</sub>	R/W TAW2/TW2A
W23	CNTR pin output control bit	0	Disables CNTR pin output	
		1	Enables CNTR pin output	
W22	PWM signal high period extend function control bit	0	Disables PWM signal high period extend function	
		1	Enables PWM signal high period extend function	
W21	Timer 2 control bit	0	Stop (state retained)	
		1	Start	
W20	Timer 2 count source select bit	0	XIN input	
		1	Prescaler output (ORCLK) divided by 2	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during port setting.



### 4.3 Pullup Control Register PU0

Table 4.3 shows the bit configuration of Pullup Control Register PU0.

For write to the register PU0, first set a value in the register A and then use the TPU0A instruction.

Furthermore, the TAPU0 instruction may be used to transfer the content of register PU0 to the register A.

Table 4.3 Bit Configuration of Pullup Control Register PU0

Pull-up control register PU0		When reset: 00002	When powered down: State retained	R/W TAPU0/TPU0A
PU03	Port P12 and P13 pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU02	Port P10 and P11 pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU01	Port P02 and P03 pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU00	Port P00 and P01 pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

### 4.4 Pullup Control Register PU1

Table 4.4 shows the bit configuration of Pullup Control Register PU1.

For write to the register PU1, first set a value in the register A and then use the TPU1A instruction.

Furthermore, the TAPU1 instruction may be used to transfer the content of register PU1 to the register A.

Table 4.4 Bit Configuration of Pullup Control Register PU1

Pull-up control register PU1		When reset: 00002	When powered down: State retained	R/W TAPU1/TPU1A
PU13	Port P23 pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU12	Port P22 pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU11	Port P21 pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU10	Port P20 pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

## 4.5 Pullup Control Register PU2

Table 4.5 shows the bit configuration of Pullup Control Register PU2.

For write to the register PU2, first set a value in the register A and then use the TPU2A instruction.

Furthermore, the TAPU2 instruction may be used to transfer the content of register PU2 to the register A.

Table 4.5 Bit Configuration of Pullup Control Register PU2

Pull-up control register PU2		When reset: 00002	When powered down: State retained	R/W TAPU2/TPU2A
PU2 <sub>3</sub>	Port P3 <sub>3</sub> pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU2 <sub>2</sub>	Port P3 <sub>2</sub> pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU2 <sub>1</sub>	Port P3 <sub>1</sub> pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU2 <sub>0</sub>	Port P3 <sub>0</sub> pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

## 4.6 Pullup Control Register PU3

Table 4.6 shows the bit configuration of Pullup Control Register PU3.

For write to the register PU3, first set a value in the register A and then use the TPU3A instruction.

Furthermore, the TAPU3 instruction may be used to transfer the content of register PU3 to the register A.

Table 4.6 Bit Configuration of Pullup Control Register PU3

Pull-up control register PU3		When reset: 00002	When powered down: State retained	R/W TAPU3/TPU3A
PU3 <sub>3</sub>	Port D <sub>6</sub> and D <sub>7</sub> pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU3 <sub>2</sub>	Port D <sub>4</sub> and D <sub>5</sub> pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU3 <sub>1</sub>	Port D <sub>2</sub> and D <sub>3</sub> pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	
PU3 <sub>0</sub>	Port D <sub>0</sub> and D <sub>1</sub> pull-up transistor control bit	0	Pull-up transistor OFF	
		1	Pull-up transistor ON	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

#### 4.7 Port Output Mode Control Register FR0

Table 4.7 shows the bit configuration of Port Output Mode Control Register FR0.

For write to the register FR0, first set a value in the register A and then use the TFR0A instruction.

Table 4.7 Bit Configuration of Port Output Mode Control Register FR0

Port Output Mode Control Register FR0		When reset: 0000 <sub>2</sub>	When powered down: State retained	W TFR0A
FR0 <sub>3</sub>	Port P1 <sub>2</sub> and P1 <sub>3</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR0 <sub>2</sub>	Port P1 <sub>0</sub> and P1 <sub>1</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR0 <sub>1</sub>	Port P0 <sub>2</sub> and P0 <sub>3</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR0 <sub>0</sub>	Port P0 <sub>0</sub> and P0 <sub>1</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	

Note 1: The letter W denotes “writable.”

#### 4.8 Port Output Mode Control Register FR1

Table 4.8 shows the bit configuration of Port Output Mode Control Register FR1.

For write to the register FR1, first set a value in the register A and then use the TFR1A instruction.

Table 4.8 Bit Configuration of Port Output Mode Control Register FR1

Port Output Mode Control Register FR1		When reset: 0000 <sub>2</sub>	When powered down: State retained	W TFR1A
FR1 <sub>3</sub>	Port D <sub>3</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR1 <sub>2</sub>	Port D <sub>2</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR1 <sub>1</sub>	Port D <sub>1</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR1 <sub>0</sub>	Port D <sub>0</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	

Note 1: The letter W denotes “writable.”

## 4.9 Port Output Mode Control Register FR2

Table 4.9 shows the bit configuration of Port Output Mode Control Register FR2.

For write to the register FR2, first set a value in the register A and then use the TFR2A instruction.

Table 4.9 Bit Configuration of Port Output Mode Control Register FR2

Port Output Mode Control Register FR2		When reset: 0000 <sub>2</sub>	When powered down: State retained	W TFR2A
FR23	Port P3 <sub>2</sub> and P3 <sub>3</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR22	Port P3 <sub>0</sub> and P3 <sub>1</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR21	Port D <sub>5</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR20	Port D <sub>4</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	

Note 1: The letter W denotes “writable.”

## 4.10 Port Output Mode Control Register FR3

Table 4.10 shows the bit configuration of Port Output Mode Control Register FR3.

For write to the register FR3, first set a value in the register A and then use the TFR3A instruction.

Table 4.10 Bit Configuration of Port Output Mode Control Register FR3

Port Output Mode Control Register FR3		When reset: 0000 <sub>2</sub>	When powered down: State retained	W TFR3A
FR33	Port P2 <sub>3</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR32	Port P2 <sub>2</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR31	Port P2 <sub>1</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR30	Port P2 <sub>0</sub> output mode select bit	0	N-channel open-drain output	
		1	CMOS output	

Note 1: The letter W denotes “writable.”

#### 4.11 Key-on Wakeup Control Register K0

Table 4.11 shows the bit configuration of Key-on Wakeup Control Register K0.

For write to the register K0, first set a value in the register A and then use the TK0A instruction.

Furthermore, the TAK0 instruction may be used to transfer the content of register K0 to the register A.

Table 4.11 Bit Configuration of Key-on Wakeup Control Register K0

Key-on Wakeup Control Register K0		When reset: 00002	When powered down: State retained	R/W TAK0/TK0A
K03	Port P12 and P13 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
K02	Port P10 and P11 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
K01	Port P02 and P03 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
K00	Port P00 and P01 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

#### 4.12 Key-on Wakeup Control Register K1

Table 4.12 shows the bit configuration of Key-on Wakeup Control Register K1.

For write to the register K1, first set a value in the register A and then use the TK1A instruction.

Furthermore, the TAK1 instruction may be used to transfer the content of register K1 to the register A.

Table 4.12 Bit Configuration of Key-on Wakeup Control Register K1

Key-on Wakeup Control Register K1		When reset: 00002	When powered down: State retained	R/W TAK1/TK1A
K13	Port P23 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
K12	Port P22 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
K11	Port P21 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
K10	Port P20 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

### 4.13 Key-on Wakeup Control Register K2

Table 4.13 shows the bit configuration of Key-on Wakeup Control Register K2.

For write to the register K2, first set a value in the register A and then use the TK2A instruction.

Furthermore, the TAK2 instruction may be used to transfer the content of register K2 to the register A.

Table 4.13 Bit Configuration of Key-on Wakeup Control Register K2

Key-on Wakeup Control Register K2		When reset: 0000 <sub>2</sub>	When powered down: State retained	R/W TAK2/TK2A
K2 <sub>3</sub>	Port P3 <sub>2</sub> and P3 <sub>3</sub> <sup>Note 3</sup> key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
K2 <sub>2</sub>	Port P3 <sub>0</sub> and P3 <sub>1</sub> <sup>Note 2</sup> key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
K2 <sub>1</sub>	INT pin return condition select bit	0	Level returned	
		1	Edge returned	
K2 <sub>0</sub>	INT pin key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: To disable the key-on wakeup function of ports P3<sub>0</sub> and P3<sub>1</sub> (K2<sub>2</sub> = 0), set the values of registers K3<sub>0</sub> and K3<sub>1</sub> to 0.

Note 3: To disable the key-on wakeup function of ports P3<sub>2</sub> and P3<sub>3</sub> (K2<sub>3</sub> = 0), set the values of registers K3<sub>2</sub> and K3<sub>3</sub> to 0.

Note 4: : Unused bits during port setting.

### 4.14 Key-on Wakeup Control Register K3

Table 4.14 shows the bit configuration of Key-on Wakeup Control Register K3.

For write to the register K3, first set a value in the register A and then use the TK3A instruction.

Furthermore, the TAK3 instruction may be used to transfer the content of register K3 to the register A.

Table 4.14 Bit Configuration of Key-on Wakeup Control Register K3

Key-on Wakeup Control Register K3		When reset: 0000 <sub>2</sub>	When powered down: State retained	R/W TAK3/TK3A
K3 <sub>3</sub>	Ports D <sub>6</sub> and D <sub>7</sub> key-on wakeup control bit	0	Key-on wakeup not used	
		1	Key-on wakeup used	
K3 <sub>2</sub>	Ports D <sub>4</sub> and D <sub>5</sub> key-on wakeup control bit	0	Key-on wakeup not used	
		1	Key-on wakeup used	
K3 <sub>1</sub>	Ports D <sub>2</sub> and D <sub>3</sub> key-on wakeup control bit	0	Key-on wakeup not used	
		1	Key-on wakeup used	
K3 <sub>0</sub>	Ports D <sub>0</sub> and D <sub>1</sub> key-on wakeup control bit	0	Key-on wakeup not used	
		1	Key-on wakeup used	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

## 4.15 Clock Control Register RG

Table 4.15 shows the bit configuration of the Clock Control Register RG.

For write to the register RG, first set a value in the register A and then use the TRGA instruction.

Table 4.15 Bit Configuration of Clock Control Register RG

Clock Control Register RG		When reset: 1000 <sub>2</sub>	When powered down: State retained	W TRGA
RG <sub>3</sub>	Low-speed on-chip oscillator (f(LSOCO)) control bit <sup>Note 3</sup>	0	Low-speed on-chip oscillator (f(LSOCO)) oscillation available	
		1	Low-speed on-chip oscillator (f(LSOCO)) oscillation stop	
RG <sub>2</sub>	Sub-clock (f(XCIN)) control bit <sup>Note 3</sup>	0	Sub-clock (f(XCIN)) oscillation available, ports D6 and D7 not selected	
		1	Sub-clock (f(XCIN)) oscillation stop, ports D6 and D7 selected	
RG <sub>1</sub>	Main-clock (f(XIN)) control bit <sup>Note 3</sup>	0	Main clock (f(XIN)) oscillation available	
		1	Main clock (f(XIN)) oscillation stop	
RG <sub>0</sub>	High-speed on-chip oscillator (f(HSOCO)) control bit <sup>Note 3</sup>	0	High-speed on-chip oscillator (f(HSOCO)) oscillation available	
		1	High-speed on-chip oscillator (f(HSOCO)) oscillation stop	

Note 1: The letter W denotes “writable.”

Note 2: : Unused bits during port setting.

Note 3: Any oscillator circuit that is selected for the system clock cannot be turned off.

## 4.16 LCD Control Register L3

Table 4.16 shows the bit configuration of the LCD Control Register L3.

For write to the register L3, first set a value in the register A and then use the TL3A instruction.

Table 4.16 Bit Configuration of LCD Control Register L3

LCD Control Register L3		When reset: 1111 <sub>2</sub>	When powered down: State retained	W TL3A
L3 <sub>3</sub>	P2 <sub>3</sub> /SEG <sub>27</sub> pin function select bit	0	SEG <sub>27</sub>	
		1	P2 <sub>3</sub>	
L3 <sub>2</sub>	P2 <sub>2</sub> /SEG <sub>26</sub> pin function select bit	0	SEG <sub>26</sub>	
		1	P2 <sub>2</sub>	
L3 <sub>1</sub>	P2 <sub>1</sub> /SEG <sub>25</sub> pin function select bit	0	SEG <sub>25</sub>	
		1	P2 <sub>1</sub>	
L3 <sub>0</sub>	P2 <sub>0</sub> /SEG <sub>24</sub> pin function select bit	0	SEG <sub>24</sub>	
		1	P2 <sub>0</sub>	

Note 1: The letter W denotes “writable.”

#### 4.17 LCD Control Register C1

Table 4.17 shows the bit configuration of the LCD Control Register C1.

For write to the register C1, first set a value in the register A and then use the TC1A instruction.

Table 4.17 Bit Configuration of LCD Control Register C1

LCD Control Register C1		When reset: 1111 <sub>2</sub>	When powered down: State retained	W TC1A
C1 <sub>3</sub>	P0 <sub>3</sub> /SEG <sub>19</sub> pin function select bit	0	SEG <sub>19</sub>	
		1	P0 <sub>3</sub>	
C1 <sub>2</sub>	P0 <sub>2</sub> /SEG <sub>18</sub> pin function select bit	0	SEG <sub>18</sub>	
		1	P0 <sub>2</sub>	
C1 <sub>1</sub>	P0 <sub>1</sub> /SEG <sub>17</sub> pin function select bit	0	SEG <sub>17</sub>	
		1	P0 <sub>1</sub>	
C1 <sub>0</sub>	P0 <sub>0</sub> /SEG <sub>16</sub> pin function select bit	0	SEG <sub>16</sub>	
		1	P0 <sub>0</sub>	

Note 1: The letter W denotes “writable.”

#### 4.18 LCD Control Register C2

Table 4.18 shows the bit configuration of the LCD Control Register C2.

For write to the register C2, first set a value in the register A and then use the TC2A instruction.

Table 4.18 Bit Configuration of LCD Control Register C2

LCD Control Register C2		When reset: 1111 <sub>2</sub>	When powered down: State retained	W TC2A
C2 <sub>3</sub>	P1 <sub>3</sub> /SEG <sub>23</sub> pin function select bit	0	SEG <sub>23</sub>	
		1	P1 <sub>3</sub>	
C2 <sub>2</sub>	P1 <sub>2</sub> /SEG <sub>22</sub> pin function select bit	0	SEG <sub>22</sub>	
		1	P1 <sub>2</sub>	
C2 <sub>1</sub>	P1 <sub>1</sub> /SEG <sub>21</sub> pin function select bit	0	SEG <sub>21</sub>	
		1	P1 <sub>1</sub>	
C2 <sub>0</sub>	P1 <sub>0</sub> /SEG <sub>20</sub> pin function select bit	0	SEG <sub>20</sub>	
		1	P1 <sub>0</sub>	

Note 1: The letter W denotes “writable.”



#### 4.19 LCD Control Register C3

Table 4.19 shows the bit configuration of the LCD Control Register C3.

For write to the register C3, first set a value in the register A and then use the TC3A instruction.

Table 4.19 Bit Configuration of LCD Control Register C3

LCD Control Register C3		When reset: 11112	When powered down: State retained	W TC3A
C33	P33/SEG31 pin function select bit	0	SEG31	
		1	P33	
C32	P32/SEG30 pin function select bit	0	SEG30	
		1	P32	
C31	P31/SEG29 pin function select bit	0	SEG29	
		1	P31	
C30	P30/SEG28 pin function select bit	0	SEG28	
		1	P30	

Note 1: The letter W denotes “writable.”

## 5. Port Application Example

### 5.1 Key Input by Key Scan

When N-channel open-drain output is selected for the output mode of port D and the internal pullup transistor of port P0 is used, a key matrix can be configured by connecting an external circuit comprised of only keys to the chip.

Point : The external component needed for this application consists of only keys.

Specification : Port D outputs a low-level signal, and port P0 accepts 16 keys as its input.

Figure 5.1 shows an example of a key matrix circuit. Figure 5.2 shows key scan input timing.

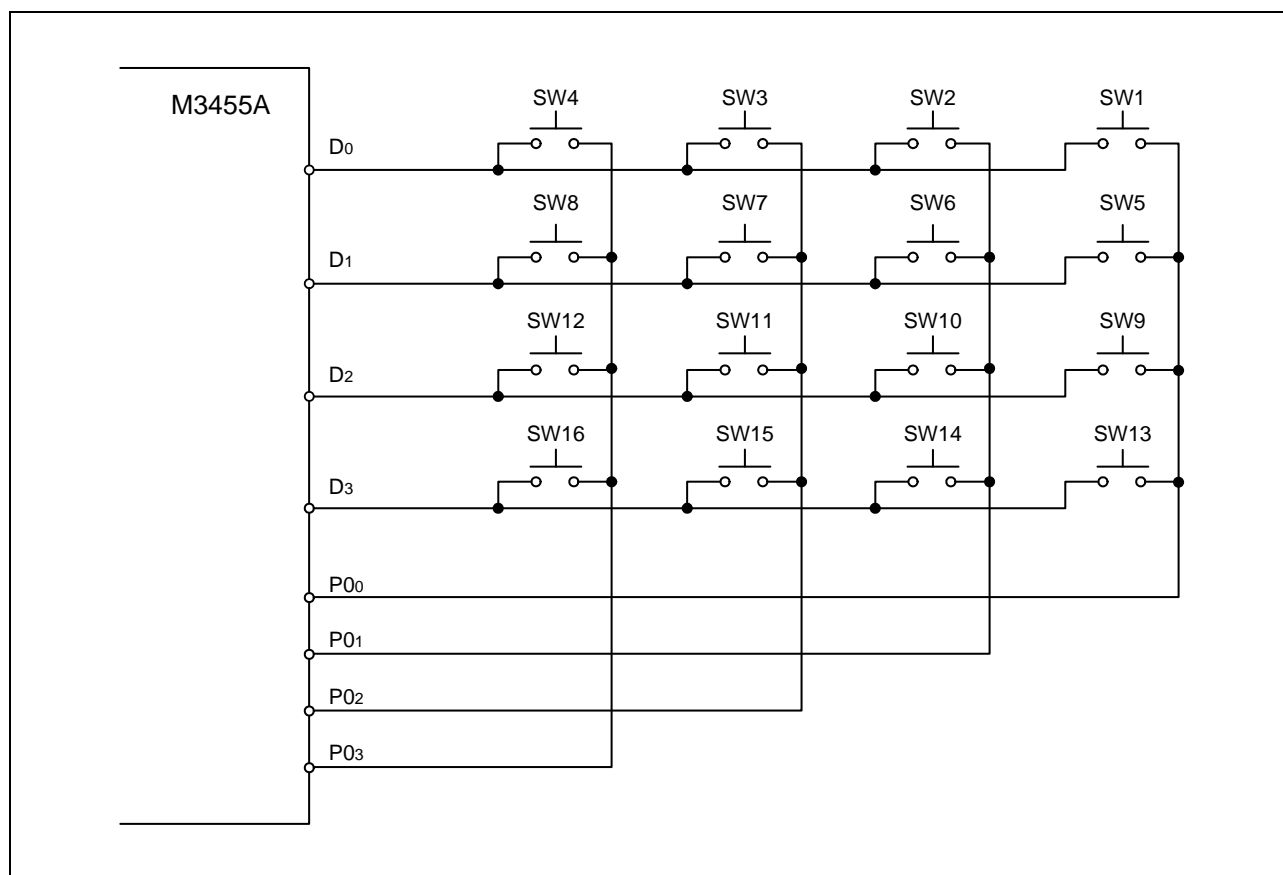


Figure 5.1 Example of a Key Matrix Circuit

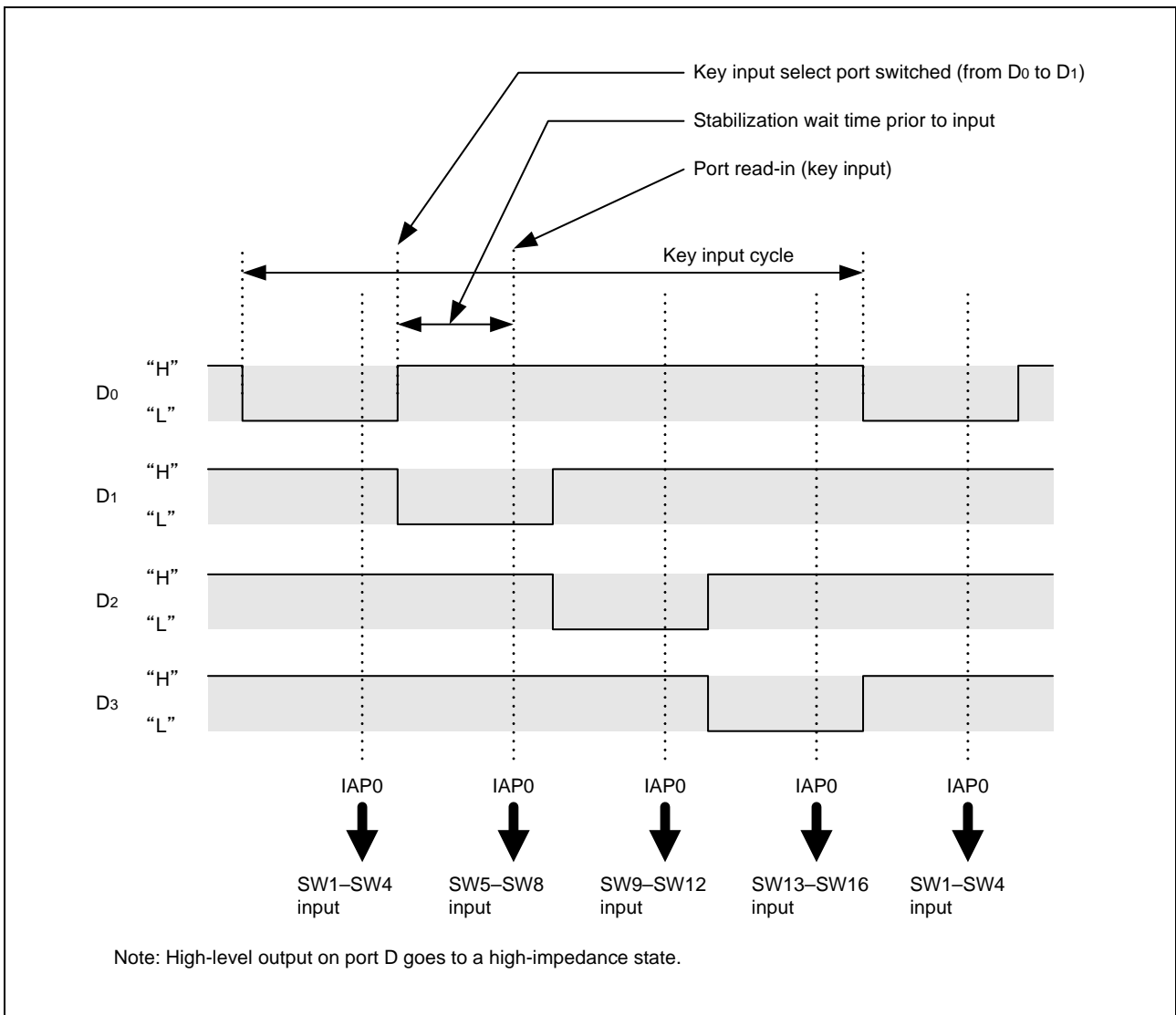


Figure 5.2 Key Scan Input Timing

## 6. Reference Documents

Data sheet

455A Group Data Sheet

(The latest version is available from the Renesas Technology Web site.)

Technical news / Technical Update

(The latest information is available from the Renesas Technology Web site.)

## 7. Sample Programs

Sample programs are available from the Renesas Technology Web site.

To download one, click the screen menu “Application Note” on the left side of 455A group Web site.

## Renesas Web Site and Where to Contact

Renesas Technology Web site:  
<http://japan.renesas.com/>

Where to contact:  
<http://japan.renesas.com/inquiry>  
[csc@renesas.com](mailto:csc@renesas.com)

Revision history	455A Group Input/Output Ports
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Rev.	Date	Description	
		Page	Points
1.00	2008.02.29	–	First edition issued

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