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4559 Group

Input/Output Ports

1. Abstract

This document shows an example of how to set the input/output ports of the 4559 group of Renesas microcomputers and an application example for using those ports.

2. Introduction

The application example explained in this document applies for use with the microcomputers and under the conditions described below.

• Microcomputer : 4559 group

Please note that the sample program for the 4559 group may somewhere in it manipulate the bits of unused functions for reasons of bit arrangement in the control registers. The values of these bits in a user system should be set to suit the usage condition of the system.

3. Input/Output Ports

3.1 Port P0

Port P0 permits 4 bits of data to be input or output to and from the port. Ports $P0_0$–$P0_3$ are shared with LCD segment output pins SEG_{16}–SEG_{19}. The pin function of these ports can be chosen to be input/output ports or LCD segment output pins by setting up the register C1.

The key-on wakeup function and the pullup transistor function of port P0 can be turned on or off by setting up the registers $K0_0$–$K0_1$ and register PU0, respectively.

Furthermore, the output mode of this port can be chosen to be N-channel open-drain output or CMOS output by setting up the registers $FR0_0$–$FR0_1$.

3.1.1 Port P0 Input/Output Method

- Input method

  For the ports $P0_0$–$P0_3$ used, set the corresponding register FR0i (i = 0–1) to 0 and then set the output latch of port P0i (i = 0–3) to 1 using the OP0A instruction. If the output latch is set to 0, a low-level signal will be input.

  When the IAP0 instruction is executed, the pin state of port P0 is transferred to the register A.

- Output method

  The content of register A is output to port P0 by the OP0A instruction.

  The output type of this port can be chosen to be N-channel open-drain output or CMOS output in 2-bit units by setting up the registers $FR0_0$–$FR0_1$.

3.2 Port P1

Port P1 permits 4 bits of data to be input or output to and from the port. Ports $P10_0$–$P1_3$ are shared with LCD segment output pins SEG_{20}–SEG_{23}. The pin function of these ports can be chosen to be input/output ports or LCD segment output pins by setting up the register C2.

The key-on wakeup function and the pullup transistor function of port P1 can be turned on or off by setting up the registers $K0_2$–$K0_3$ and register PU1, respectively.

Furthermore, the output mode of this port can be chosen to be N-channel open-drain output or CMOS output by setting up the registers $FR0_2$–$FR0_3$.

3.2.1 Port P1 Input/Output Method

- Input method

  For the ports $P1_0$–$P1_3$ used, set the corresponding register FR0i (i = 2–3) to 0 and then set the output latch of port P1i (i = 0–3) to 1 using the OP1A instruction. If the output latch is set to 0, a low-level signal will be input.

  When the IAP1 instruction is executed, the pin state of port P1 is transferred to the register A.

- Output method

  The content of register A is output to port P1 by the OP1A instruction.

  The output type of this port can be chosen to be N-channel open-drain output or CMOS output in 2-bit units by setting up the registers $FR0_2$–$FR0_3$.

3.3 Port P2

Port P2 permits 4 bits of data to be input or output to and from the port. Ports $P2_0$–$P2_3$ are shared with LCD segment output pins SEG_{24}–SEG_{27}. The pin function of these ports can be chosen to be input/output ports or LCD segment output pins by setting up the register L3.

The key-on wakeup function and the pullup transistor function of port P2 can be turned on or off by setting up the register K1 and register PU2, respectively.

Furthermore, the output mode of this port can be chosen to be N-channel open-drain output or CMOS output by setting up the register FR3.

3.3.1 Port P2 Input/Output Method

- Input method

  For the ports $P2_0$–$P2_3$ used, set the corresponding register FR3i (i = 0–3) to 0 and then set the output latch of port P2i (i = 0–3) to 1 using the OP2A instruction. If the output latch is set to 0, a low-level signal will be input.

  When the IAP2 instruction is executed, the pin state of port P2 is transferred to the register A.

- Output method

  The content of register A is output to port P2 by the OP2A instruction.

  The output type of this port can be chosen to be N-channel open-drain output or CMOS output in 1-bit units by setting up the registers $FR3_0$–$FR3_3$.

3.4 Port P3

Port P3 permits 4 bits of data to be input or output to and from the port. Ports $P3_0$–$P3_3$ are shared with LCD segment output pins SEG_{28}–SEG_{31}. The pin function of these ports can be chosen to be input/output ports or LCD segment output pins by setting up the register C3.

The key-on wakeup function and the pullup transistor function of port P3 can be turned on or off by setting up the register K2i (i = 2–3) and K3 and the register PU3, respectively.

Furthermore, the output mode of this port can be chosen to be N-channel open-drain output or CMOS output by setting up the registers $FR2_2$–$FR2_3$.

3.4.1 Port P3 Input/Output Method

- Input method

  For the ports $P3_0$–$P3_3$ used, set the corresponding register FR2i (i = 2–3) to 0 and then set the output latch of port P3i (i = 0–3) to 1 using the OP3A instruction. If the output latch is set to 0, a low-level signal will be input.

  When the IAP3 instruction is executed, the pin state of port P3 is transferred to the register A.

- Output method

  The content of register A is output to port P3 by the OP3A instruction.

  The output type of this port can be chosen to be N-channel open-drain output or CMOS output in 2-bit units by setting up the registers $FR2_2$–$FR2_3$.

3.5 Port D

Port D consists of six bitwise input/output ports and two bitwise output ports. Ports D_5, D_6 and D_7 are shared with the INT, X_{CIN} and X_{COUT} pins, respectively.

Furthermore, the output mode of ports D_0–D_5 can be chosen to be N-channel open-drain output or CMOS output by setting up the registers FR1 and $FR2_0$–$FR2_1$.

When the CLD instruction is executed, all pins of port D go to a high-impedance state or a high-level state depending on how the registers FR1i (i=0–3) and FR2i (i=0–1) are set.

3.5.1 Port D_0–D_5 Input/Output Method

Ports D_0–D_5 control input/output of data bitwise, or one bit at a time. Therefore, if data is to be input/output on ports D_0–D_5, one line of port D must first be selected with the data pointer register Y.

- Input method

  For the ports D_0–D_5 used, set the corresponding register FR1i (i = 0–3) and FR2i (i = 0–1) to 0 and then set the output latch of port Di (i = 0–5) to 1 using the SD instruction. If the output latch is set to 0, a low-level signal will be input.

  When the SZD instruction is executed, if the content of the port specified by the register Y is 0, the next instruction is skipped; if 1, the next instruction is executed.

- Output method

  Set the output level of ports D_0–D_5 in each corresponding output latch using the SD and RD instructions.

  The output modes of ports D_0–D_3 and ports D_4–D_5 can be chosen to be N-channel open-drain output or CMOS output in 1-bit units by setting up the register FR1 and registers $FR2_0$–$FR2_1$, respectively.

  When the SD instruction is executed, the port pin goes to a high-impedance or a high-level state depending on how the registers FR1i (i = 0–3) and FR2i (i = 0–1) are set.

  When the RD instruction is executed, the port pin goes to a low-level state.

3.5.2 Port D_6–D_7 Output Method

Ports D_6–D_7 control output of data bitwise, or one bit at a time. Therefore, if data is to be output on ports D_6–D_7, one line of port D must first be selected with the data pointer register Y.

Ports D_6–D_7 are shared with the X_{CIN} and X_{COUT} pins, respectively. To use these shared facilities as ports D_6–D_7, set the register RG2 to 1.

- Output method

  Set the output level of ports D_6–D_7 in each corresponding output latch using the SD and RD instructions.

  When the SD instruction is executed, the port pin goes to a high-impedance state.

  When the RD instruction is executed, the port pin goes to a low-level state.

Note: If the SD and RD instructions are used, do not set any value equal to or greater than "1000_2" in the register Y.

3.6 Port C

Port C permits 1 bit of data to be output from the port. Port C is shared with the CNTR pin. However, if the CNTR pin is used for input, no data can be output from this port.

3.6.1 Port C Output Method

- Output method
  The output mode of this port is CMOS. When the SCP instruction is executed, the port pin goes to a high-level state.
  When the RCP instruction is executed, the port pin goes to a low-level state.

Note: Actually output from the pin is a logical OR of CNTR output and port C output.

4. Related Registers

4.1 Timer Control Register W1

Table 4.1 shows the bit configuration of Timer Control Register W1.

For write to the register W1, first set a value in the register A and then use the TW1A instruction.

Furthermore, the TAW1 instruction may be used to transfer the content of register W1 to the register A.

Table 4.1 Bit Configuration of Timer Control Register W1

Timer Control Register W1		When reset: 0000_2		When powered down: State retained	R/W TAW1/TW1A
$W1_3$	Timer 1 count auto stop circuit select bit Note 2	0	Deselects timer 1 count auto stop circuit		
		1	Selects timer 1 count auto stop circuit		
$W1_2$	Timer 1 control bit	0	Stop (state retained)		
		1	Start		
$W1_1$	Timer 1 count source select bit Note 3	$W1_1$	$W1_0$	Count source	
		0	0	PWM signal (PWMOUT)	
		0	1	Prescaler output (ORCLK)	
$W1_0$		1	0	Timer 3 underflow signal (T3UDF)	
		1	1	CNTR input	

Note 1: The letter R denotes "readable," and the letter W denotes "writable."
Note 2: This function is usable only when the timer 1 count start synchronizing circuit is selected ($I1_0 = 1$).
Note 3: If CNTR input is selected for the timer 1 count source, port C output is disabled.
Note 4: : Unused bits during port setting.

4.2 Timer Control Register W2

Table 4.2 shows the bit configuration of Timer Control Register W2.

For write to the register W2, first set a value in the register A and then use the TW2A instruction.

Furthermore, the TAW2 instruction may be used to transfer the content of register W2 to the register A.

Table 4.2 Bit Configuration of Timer Control Register W2

Timer Control Register W2		When reset: 0000_2		When powered down: 0000_2	R/W TAW2/TW2A
$W2_3$	CNTR pin output control bit	0	Disables CNTR pin output		
		1	Enables CNTR pin output		
$W2_2$	PWM signal high period extend function control bit	0	Disables PWM signal high period extend function		
		1	Enables PWM signal high period extend function		
$W2_1$	Timer 2 control bit	0	Stop (state retained)		
		1	Start		
$W2_0$	Timer 2 count source select bit	0	X_{IN} input		
		1	Prescaler output (ORCLK) divided by 2		

Note 1: The letter R denotes "readable," and the letter W denotes "writable."
Note 2: : Unused bits during port setting.

4.3 Pullup Control Register PU0

Table 4.3 shows the bit configuration of Pullup Control Register PU0.

For write to the register PU0, first set a value in the register A and then use the TPU0A instruction.

Furthermore, the TAPU0 instruction may be used to transfer the content of register PU0 to the register A.

Table 4.3 Bit Configuration of Pullup Control Register PU0

Pullup Control Register PU0		When reset: 0000_2		When powered down: State retained	R/W TAPU0/TPU0A
$PU0_3$	Port $P0_3$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU0_2$	Port $P0_2$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU0_1$	Port $P0_1$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU0_0$	Port $P0_0$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

4.4 Pullup Control Register PU1

Table 4.4 shows the bit configuration of Pullup Control Register PU1.

For write to the register PU1, first set a value in the register A and then use the TPU1A instruction.

Furthermore, the TAPU1 instruction may be used to transfer the content of register PU1 to the register A.

Table 4.4 Bit Configuration of Pullup Control Register PU1

Pullup Control Register PU1		When reset: 0000_2		When powered down: State retained	R/W TAPU1/TPU1A
$PU1_3$	Port $P1_3$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU1_2$	Port $P1_2$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU1_1$	Port $P1_1$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU1_0$	Port $P1_0$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

4.5 Pullup Control Register PU2

Table 4.5 shows the bit configuration of Pullup Control Register PU2.

For write to the register PU2, first set a value in the register A and then use the TPU2A instruction.

Furthermore, the TAPU2 instruction may be used to transfer the content of register PU2 to the register A.

Table 4.5 Bit Configuration of Pullup Control Register PU2

Pullup Control Register PU2		When reset: 0000_2		When powered down: State retained	R/W TAPU2/TPU2A
$PU2_3$	Port $P2_3$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU2_2$	Port $P2_2$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU2_1$	Port $P2_1$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU2_0$	Port $P2_0$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

4.6 Pullup Control Register PU3

Table 4.6 shows the bit configuration of Pullup Control Register PU3.

For write to the register PU3, first set a value in the register A and then use the TPU3A instruction.

Furthermore, the TAPU3 instruction may be used to transfer the content of register PU3 to the register A.

Table 4.6 Bit Configuration of Pullup Control Register PU3

Pullup Control Register PU3		When reset: 0000_2		When powered down: State retained	R/W TAPU3/TPU3A
$PU3_3$	Port $P3_3$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU3_2$	Port $P3_2$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU3_1$	Port $P3_1$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		
$PU3_0$	Port $P3_0$ pullup transistor control bit	0	Turns pullup transistor off		
		1	Turns pullup transistor on		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

4.7 Port Output Mode Control Register FR0

Table 4.7 shows the bit configuration of Port Output Mode Control Register FR0.

For write to the register FR0, first set a value in the register A and then use the TFR0A instruction.

Table 4.7 Bit Configuration of Port Output Mode Control Register FR0

Port Output Mode Control Register FR0		When reset: 0000_2		When powered down: State retained	W TFR0A
$FR0_3$	Port $P1_2$ and $P1_3$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR0_2$	Port $P1_0$ and $P1_1$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR0_1$	Port $P0_2$ and $P0_3$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR0_0$	Port $P0_0$ and $P0_1$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		

Note 1: The letter W denotes “writable.”

4.8 Port Output Mode Control Register FR1

Table 4.8 shows the bit configuration of Port Output Mode Control Register FR1.

For write to the register FR1, first set a value in the register A and then use the TFR1A instruction.

Table 4.8 Bit Configuration of Port Output Mode Control Register FR1

Port Output Mode Control Register FR1		When reset: 0000_2		When powered down: State retained	W TFR1A
$FR1_3$	Port D_3 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_2$	Port D_2 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_1$	Port D_1 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_0$	Port D_0 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		

Note 1: The letter W denotes “writable.”

4.9 Port Output Mode Control Register FR2

Table 4.9 shows the bit configuration of Port Output Mode Control Register FR2.

For write to the register FR2, first set a value in the register A and then use the TFR2A instruction.

Table 4.9 Bit Configuration of Port Output Mode Control Register FR2

Port Output Mode Control Register FR2		When reset: 0000_2		When powered down: State retained	W TFR2A
$FR2_3$	Port $P3_2$ and $P3_3$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR2_2$	Port $P3_0$ and $P3_1$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR2_1$	Port D_5 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR2_0$	Port D_4 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		

Note 1: The letter W denotes “writable.”

4.10 Port Output Mode Control Register FR3

Table 4.10 shows the bit configuration of Port Output Mode Control Register FR3.

For write to the register FR3, first set a value in the register A and then use the TFR3A instruction.

Table 4.10 Bit Configuration of Port Output Mode Control Register FR3

Port Output Mode Control Register FR3		When reset: 0000_2		When powered down: State retained	W TFR3A
$FR3_3$	Port $P2_3$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR3_2$	Port $P2_2$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR3_1$	Port $P2_1$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR3_0$	Port $P2_0$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		

Note 1: The letter W denotes “writable.”

4.11 Key-on Wakeup Control Register K0

Table 4.11 shows the bit configuration of Key-on Wakeup Control Register K0.

For write to the register K0, first set a value in the register A and then use the TK0A instruction.

Furthermore, the TAK0 instruction may be used to transfer the content of register K0 to the register A.

Table 4.11 Bit Configuration of Key-on Wakeup Control Register K0

Key-on Wakeup Control Register K0		When reset: 0000_2		When powered down: State retained	R/W TAK0/TK0A
$K0_3$	Port $P1_2$ and $P1_3$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K0_2$	Port $P1_0$ and $P1_1$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K0_1$	Port $P0_2$ and $P0_3$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K0_0$	Port $P0_0$ and $P0_1$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

4.12 Key-on Wakeup Control Register K1

Table 4.12 shows the bit configuration of Key-on Wakeup Control Register K1.

For write to the register K1, first set a value in the register A and then use the TK1A instruction.

Furthermore, the TAK1 instruction may be used to transfer the content of register K1 to the register A.

Table 4.12 Bit Configuration of Key-on Wakeup Control Register K1

Key-on Wakeup Control Register K1		When reset: 0000_2		When powered down: State retained	R/W TAK1/TK1A
$K1_3$	Port $P2_3$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K1_2$	Port $P2_2$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K1_1$	Port $P2_1$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
$K1_0$	Port $P2_0$ key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

4.13 Key-on Wakeup Control Register K2

Table 4.13 shows the bit configuration of Key-on Wakeup Control Register K2.

For write to the register K2, first set a value in the register A and then use the TK2A instruction.

Furthermore, the TAK2 instruction may be used to transfer the content of register K2 to the register A.

Table 4.13 Bit Configuration of Key-on Wakeup Control Register K2

Key-on Wakeup Control Register K2		When reset: 0000_2	When powered down: State retained	R/W TAK2/TK2A
$K2_3$	Port $P3_2$ and $P3_3$ Note 3 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
$K2_2$	Port $P3_0$ and $P3_1$ Note 2 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
$K2_1$	INT pin return condition select bit	0	Level returned	
		1	Edge returned	
$K2_0$	INT pin key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: To disable the key-on wakeup function of ports $P3_0$ and $P3_1$ ($K2_2$ = 0), set the values of registers $K3_0$ and $K3_1$ to 0.

Note 3: To disable the key-on wakeup function of ports $P3_2$ and $P3_3$ ($K2_3$ = 0), set the values of registers $K3_2$ and $K3_3$ to 0.

Note 4: : Unused bits during port setting.

4.14 Key-on Wakeup Control Register K3

Table 4.14 shows the bit configuration of Key-on Wakeup Control Register K3.

For write to the register K3, first set a value in the register A and then use the TK3A instruction.

Furthermore, the TAK3 instruction may be used to transfer the content of register K3 to the register A.

Table 4.14 Bit Configuration of Key-on Wakeup Control Register K3

Key-on Wakeup Control Register K3		When reset: 0000_2	When powered down: State retained	R/W TAK3/TK3A
$K3_3$	Ports $P3_2$ and $P3_3$ Note 3 return condition select bit	0	Level returned	
		1	Edge returned	
$K3_2$	Ports $P3_2$ and $P3_3$ Note 3 active waveform/ level select bit	0	Falling waveform/low level	
		1	Rising waveform/high level	
$K3_1$	Ports $P3_0$ and $P3_1$ Note 2 return condition select bi	0	Level returned	
		1	Edge returned	
$K3_0$	Ports $P3_0$ and $P3_1$ Note 2 active waveform/ level select bit	0	Falling waveform/low level	
		1	Rising waveform/high level	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: To disable the key-on wakeup function of ports $P3_0$ and $P3_1$ ($K2_2$ = 0), set the values of registers $K3_0$ and $K3_1$ to 0.

Note 3: To disable the key-on wakeup function of ports $P3_2$ and $P3_3$ ($K2_3$ = 0), set the values of registers $K3_2$ and $K3_3$ to 0.

4.15 Clock Control Register RG

Table 4.15 shows the bit configuration of the Clock Control Register RG.

For write to the register RG, first set a value in the register A and then use the TRGA instruction.

Table 4.15 Bit Configuration of Clock Control Register RG

Clock Control Register RG		When reset: 000_2		When powered down: State retained	W TRGA
RG_2	Sub-clock (f(X_{CIN})) control bit Note 3	0	Enables sub-clock (f(X_{CIN})) to oscillate, with ports D_6 and D_7 unselected		
		1	Stops sub-clock (f(X_{CIN})) from oscillating, with ports D_6 and D_7 selected		
RG_1	Main clock (f(X_{IN})) control bit Note 3	0	Enables main clock (f(X_{IN})) to oscillate		
		1	Stops main clock (f(X_{IN})) from oscillating		
RG_0	On-chip oscillator (f(RING)) control bit Note 3	0	Enables on-chip oscillator (f(RING)) to oscillate		
		1	Stops on-chip oscillator (f(RING)) from oscillating		

Note 1: The letter W denotes “writable.”

Note 2: : Unused bits during port setting.

Note 3: Any oscillator circuit that is selected for the system clock cannot be turned off.

4.16 LCD Control Register L3

Table 4.16 shows the bit configuration of the LCD Control Register L3.

For write to the register L3, first set a value in the register A and then use the TL3A instruction.

Table 4.16 Bit Configuration of LCD Control Register L3

LCD Control Register L3		When reset: 1111_2		When powered down: State retained	W TL3A
$L3_3$	$P2_3$/SEG_{27} pin function select bit	0	SEG_{27}		
		1	$P2_3$		
$L3_2$	$P2_2$/SEG_{26} pin function select bit	0	SEG_{26}		
		1	$P2_2$		
$L3_1$	$P2_1$/SEG_{25} pin function select bit	0	SEG_{25}		
		1	$P2_1$		
$L3_0$	$P2_0$/SEG_{24} pin function select bit	0	SEG_{24}		
		1	$P2_0$		

Note 1: The letter W denotes “writable.”

4.17 LCD Control Register C1

Table 4.17 shows the bit configuration of the LCD Control Register C1.

For write to the register C1, first set a value in the register A and then use the TC1A instruction.

Table 4.17 Bit Configuration of LCD Control Register C1

LCD Control Register C1		When reset: 1111_2		When powered down: State retained	W TC1A
$C1_3$	$P0_3$/SEG_{19} pin function select bit	0	SEG_{19}		
		1	$P0_3$		
$C1_2$	$P0_2$/SEG_{18} pin function select bit	0	SEG_{18}		
		1	$P0_2$		
$C1_1$	$P0_1$/SEG_{17} pin function select bit	0	SEG_{17}		
		1	$P0_1$		
$C1_0$	$P0_0$/SEG_{16} pin function select bit	0	SEG_{16}		
		1	$P0_0$		

Note 1: The letter W denotes “writable.”

4.18 LCD Control Register C2

Table 4.18 shows the bit configuration of the LCD Control Register C2.

For write to the register C2, first set a value in the register A and then use the TC2A instruction.

Table 4.18 Bit Configuration of LCD Control Register C2

LCD Control Register C2		When reset: 1111_2		When powered down: State retained	W TC2A
$C2_3$	$P1_3$/SEG_{23} pin function select bit	0	SEG_{23}		
		1	$P1_3$		
$C2_2$	$P1_2$/SEG_{22} pin function select bit	0	SEG_{22}		
		1	$P1_2$		
$C2_1$	$P1_1$/SEG_{21} pin function select bit	0	SEG_{21}		
		1	$P1_1$		
$C2_0$	$P1_0$/SEG_{20} pin function select bit	0	SEG_{20}		
		1	$P1_0$		

Note 1: The letter W denotes “writable.”

4.19 LCD Control Register C3

Table 4.19 shows the bit configuration of the LCD Control Register C3.

For write to the register C3, first set a value in the register A and then use the TC3A instruction.

Table 4.19 Bit Configuration of LCD Control Register C3

LCD Control Register C3		When reset: 1111_2		When powered down: State retained	W TC3A
$C3_3$	$P3_3$/SEG_{31} pin function select bit	0	SEG_{31}		
		1	$P3_3$		
$C3_2$	$P3_2$/SEG_{30} pin function select bit	0	SEG_{30}		
		1	$P3_2$		
$C3_1$	$P3_1$/SEG_{29} pin function select bit	0	SEG_{29}		
		1	$P3_1$		
$C3_0$	$P3_0$/SEG_{28} pin function select bit	0	SEG_{28}		
		1	$P3_0$		

Note 1: The letter W denotes “writable.”

5. Port Application Example

5.1 Key Input by Key Scan

When N-channel open-drain output is selected for the output mode of port D and the internal pullup transistor of port P0 is used, a key matrix can be configured by connecting an external circuit comprised of only keys to the chip.

Point : The external component needed for this application consists of only keys.
Specification : Port D outputs a low-level signal, and port P0 accepts 16 keys as its input.

Figure 5.1 shows an example of a key matrix circuit. Figure 5.2 shows key scan input timing.

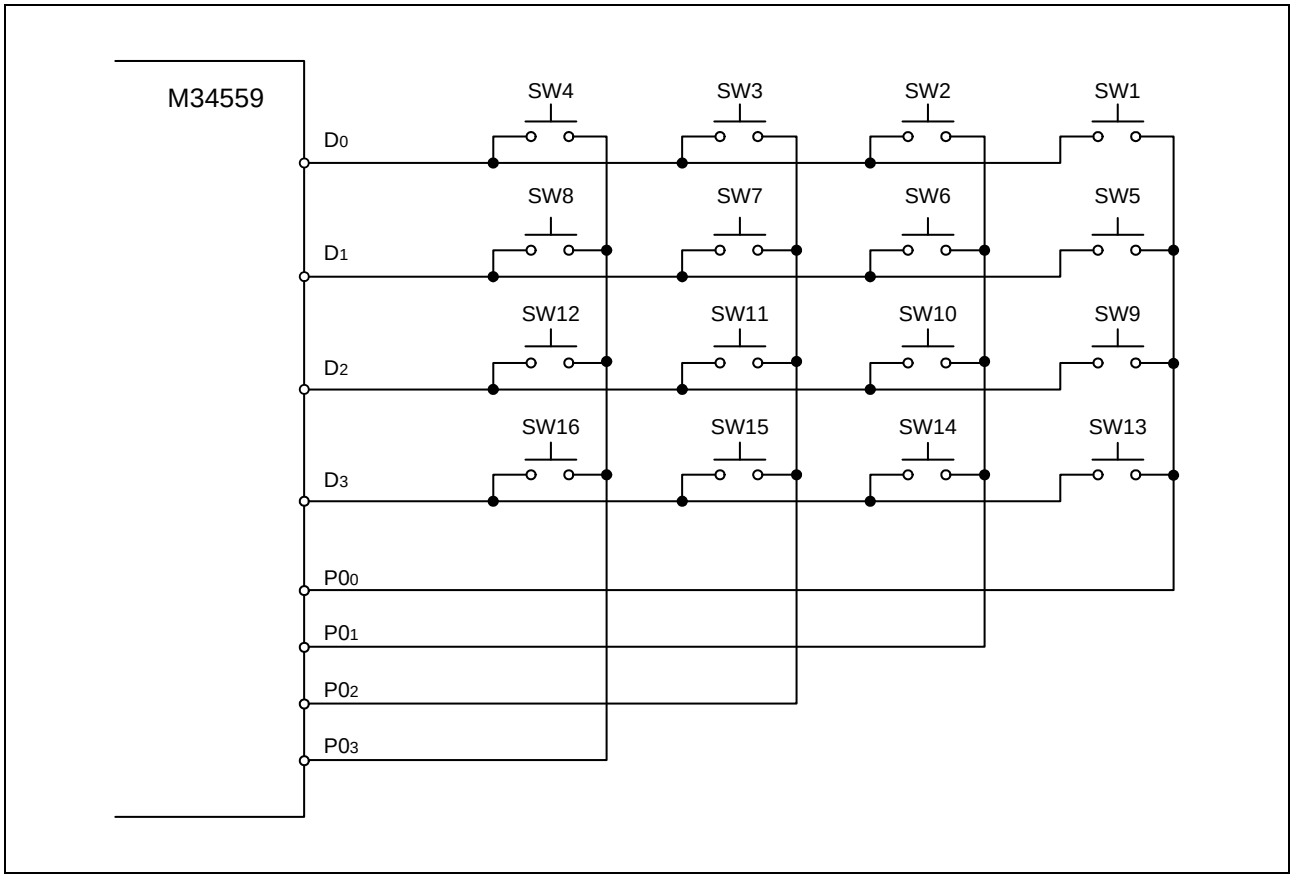
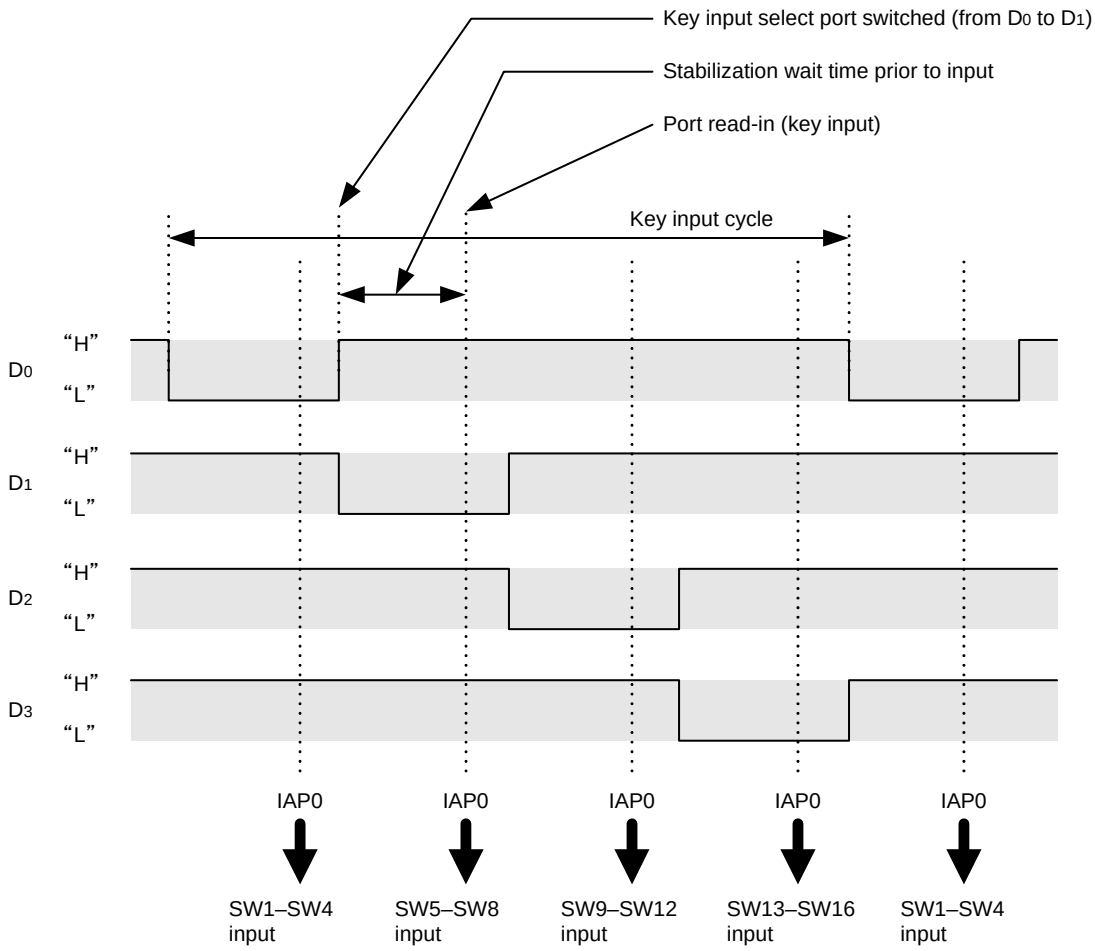


Figure 5.1 Example of a Key Matrix Circuit



Note: High-level output on port D goes to a high-impedance state.

Figure 5.2 Key Scan Input Timing

6. Reference Documents

Data sheet
4559 Group Data Sheet

The latest version is available from the Renesas Technology Web site.

7. Renesas Web Site and Where to Contact

Renesas Technology Web site:
http://japan.renesas.com/

Where to contact:
http://japan.renesas.com/inquiry
csc@renesas.com

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		Page	Points
1.00	2006.11.01	–	First edition issued

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