SDRAM Architecture, Signals and Routing Considerations for the RC32355/RC32351

Application Note AN-440

Notes

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Introduction

The RC32355/RC32351 devices are a "System on a Chip" containing a high performance 32-bit microprocessor. The microprocessor core is used extensively at the heart of the device to implement the most needed functionalities in software with minimal hardware support. The high performance microprocessor handles diverse general computing tasks and specific application tasks that would have required dedicated hardware. Specific application tasks implemented in software can include routing functions, fire wall functions, modem emulation, ATM SAR emulation, and others.

This application note provides information on board architecture, signal routing requirements, and system loading requirements that should be followed when designing an SDRAM-based memory subsystem capable of operating at the maximum system bus frequency of the processor.

Architectural Design

The SDRAM controller provides a glueless interface to industry standard SDRAMs and SDRAM SODIMMs. The SDRAM controller provides two chip selects (SDCSN[1:0]) with each chip select supporting two or four internal SDRAM banks. Two internal banks are supported when 16 Mb SDRAMs are used and four internal banks when 64 Mb, 128 Mb, or 256 Mb SDRAMs are used. Each SDRAM chip select (that is, external SDRAM bank) supports a 32-bit data path.

For maximum SDRAM speed, it is recommended that all SDRAM control and data signals be directly connected to the RC32355/RC32351. All other memory devices should be placed behind the data and address buffers. The SYSCLKP pin should be used to drive only the clocks on the SDRAM chips. It should not be used to drive any other device on the board.

The SDCLKINP clock is used to clock in the data from the SDRAM. The SDCLKINP signal should be tapped off from the SYSCLKP at the SDRAM. The length of the resulting SDCLKINP trace should match the SDRAM data trace length as much as possible. In no case should the length of the SDCLKINP trace exceed the length of the SDRAM data traces. The SDRAM data flow architecture for normally loaded systems is shown in Figure 1 below.

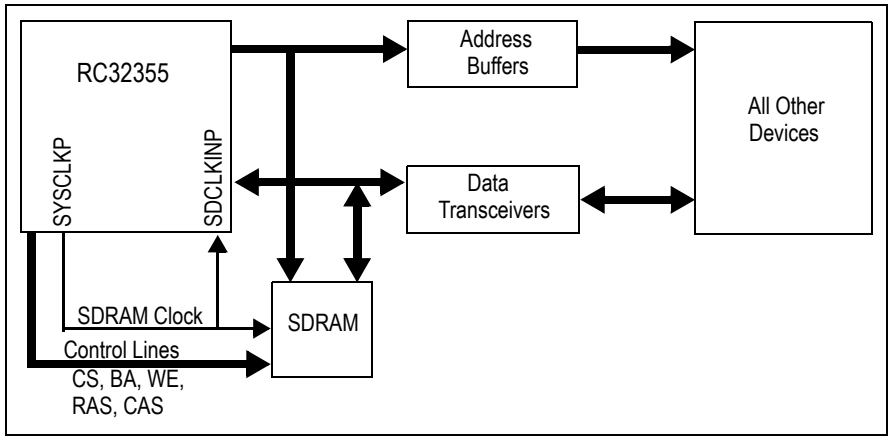

Figure 1 SDRAM Data Flow Architecture, Normally Loaded Systems

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The SDRAM data flow architecture for heavily loaded systems is shown in Figure 2 below. The timing of the data path through data transceivers must be considered when designing such systems.

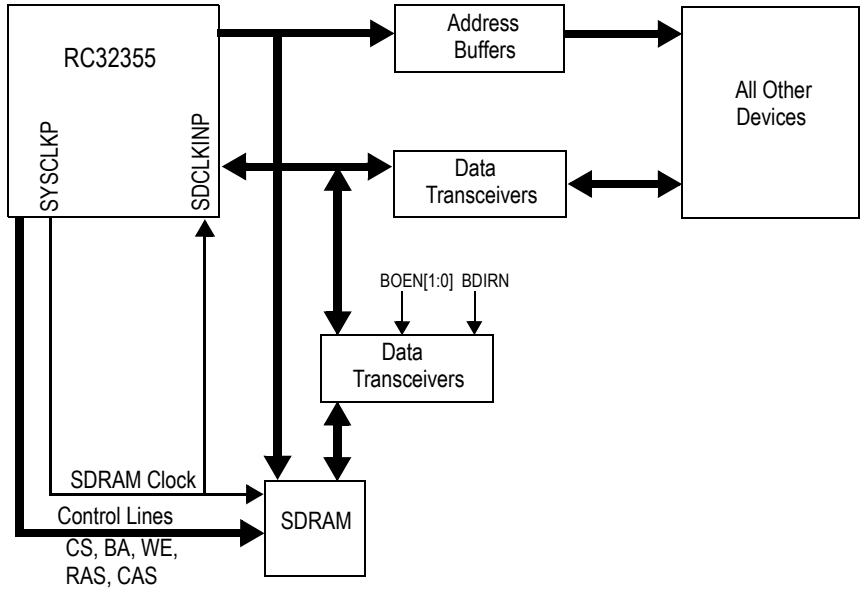

Figure 2 SDRAM Data Flow Architecture, Heavily Loaded Systems

Signal Routing

To provide the most margin for SDRAM hold times:

- *Keep all signals going to the SDRAM, address, data, and control signals as short as possible*
- *Match trace lengths as close as possible*
- *Minimize as much as possible the trace length for SYSCLKP (this is very important)*
- *Make the SYSCLKP trace the shortest SDRAM trace on the board*
- *Match the length of the SDCLKINP to the SDRAM data lines.*

Although this optimum configuration may not be achievable, the closer the layout conforms to this configuration, the greater the margin for SDRAM hold times.

System Loading

To support maximum speeds, reasonable SDRAM loading constraints must be followed. For high-speed operation, it is recommended that no more than 6 loads (total) be used. For example, a system with four discrete SDRAM chips, a PROM and possibly one other peripheral can be connected directly to the processor. It is acceptable to use a SODIMM or DIMM, provided it does not contain more than four chips. In addition, any unused clock lines should be left unconnected; otherwise, the loading on SYSCLKP could exceed the drive capability of the RC32355/RC32351 SYSCLKP pin.

It is possible to use more than four SDRAM chips or very large DIMMs at lower speeds. However, if the loading exceeds the above recommendation, users should buffer all of the control, address, and data lines accordingly. Because of the extra delay associated with this, higher system speeds are not achievable. Also, timing analysis should be done when designing such systems. To calculate maximum possible system speeds for specific designs, users should review the data sheet for the RC32355 or RC32351, both of which can be found on the IDT web page, as well as the data sheets for the buffers and other devices being used.

Notes

Connecting SDRAM Clocks

SDRAM accesses are expected to operate at the full bandwidth of the system clock (CLK). In order to accomplish this, the RC32355/351 provides an output clock (SYSCLKP) and accepts an input clock (SDCLKINP). Both clocks run at the same frequency as CLK. The output clock, SYSCLKP, should be connected to the SDRAM chips and returned to the RC32355/RC32351 through SDCLKINP. Figure 3 below shows the connection of SDRAM clocks.

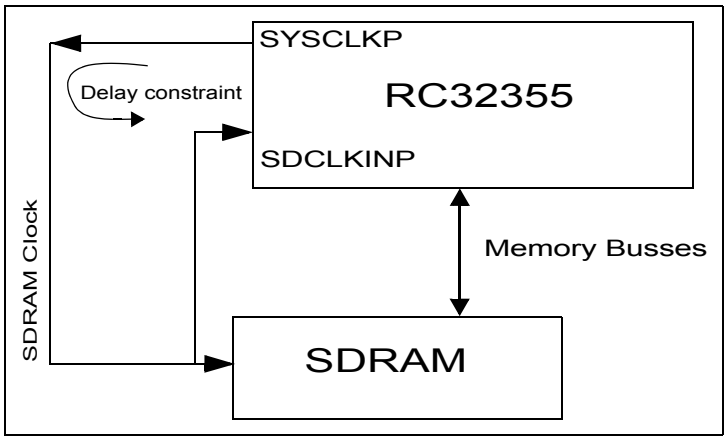

Figure 3 Connection of SDRAM Clocks

When accessing SDRAMs, the RC32355/RC32351 outputs all SDRAM control signals (such as RASN, MADDR, BWEN, SDWEN, etc.) relative to SYSCLKP. SDCLKINP is used to register SDRAM read data. This implies that all signals going to the SDRAM chips from the RC32355/RC32351 must meet setup and hold times relative to SYSCLKP, while signals going to theRC32355/RC32351 from the SDRAM chips (i.e., the SDRAM read data) must meet setup and hold times relative to SDCLKINP. Finally, as shown in Figure 3, the circuit board routing and load delay of the SDRAM clock must be within the limits specified in the data sheet.

SODIMM Support

The SDRAM controller can be configured to control SODIMMs. In this mode, the RC32355/RC32351 drives eight data masks (four on BWEN [3:0] and four on MADDR [20:17]). Because the RC32355/RC32351 data bus is 32-bits wide while SODIMMs support a 64-bit data path, either BWEN [3:0] or MADDR [20:17] will control the accessing of the correct word to the SODIMM, depending on the state of an internally decoded upper address bit. To connect SODIMMs to the RC32355/RC32351, connect the 32-bit data bus (MDATA [31:0]) to the 64-bit data bus of the SODIMM. MDATA [0] connects to SODIMM DATA [0] and SODIMM DATA [32]; MDATA [1] connects to SODIMM DATA [1] and SODIMM DATA [33], and so on. Connect MADDR [20:17] to the upper data masks of the SODIMM (DQM [7:4]) and BWEN [3:0] to the lower data masks (DQM [3:0]).

All remaining SDRAM control signals are connected as usual. SODIMM mode is enabled by setting the SODIMM Mode Enable (SOD) bit in the SDRAMC register. The SDRAMC register DTYPE and PS field is configured with the type of SDRAMs on the SODIMM. For SODIMMs that require two chip selects (SDCSN [0|1]), both SDRAM memory regions must be configured so that the two regions are equal, contiguous, and together total the amount of memory on the SODIMM. For an example, see Figure 4.

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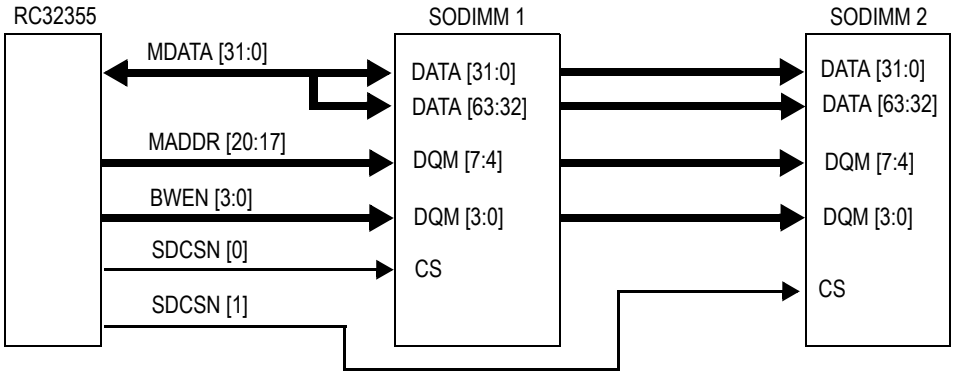

Figure 4 SODIMM Connection Example

SDRAM System Example

The purpose of this example is to show how to program the SDRAM controller with the RC32355/RC32351 and 128MB of SDRAM (SODIMM). Refer to Figure 4. Because the system uses two 64MB SODIMMs, one SODIMM must be connected to SDCSN [0] and the other to SDCSN [1]. Finally, because each of the two SODIMMs provides 64MB and is connected to one of the RC32355/RC32351's SDRAM chip-selects, the SDRAM Base and Mask registers could be programmed as follows:

SDRAM0BASE = 0x0000_0000
SDRAM0MASK = 0xFC00_0000 — 64MB

SDRAM1BASE = 0x0400_0000
SDRAM1MASK = 0xFC00_0000 — 64MB

Note: The above Base and Mask register programming will allocate 128MB of continuous SDRAM space starting at physical address 0x0000_0000. If each SODIMM is composed of eight 2Mbx8x4 SDRAM chips, the SDRAMC register must be programmed as follows:

SDRAMC.PS = 9-bit page (because the SODIMM is composed of eight 2Mbx8x4 SDRAM chips).

SDRAMC.DTYPE = 64Mbit SDRAM (because the SODIMM is composed of eight 2Mbx8x4 SDRAM chips).

SDRAMC.SOD = 1 (enable SODIMM mode).

Other SDRAM fields, such as CL, RCD, RP, and RC should be programmed to values consistent with those in the SODIMM's specification. Note that if DIMMs are used, they should contain a maximum of 8 chips. For example, if two DIMMs are used, each DIMM should contain no more than four chips.

Design Resources

Detailed information on the 79EB355 and 79EB351 evaluation boards, which are designed to support the maximum system bus frequencies, are available on the IDT web site (www.idt.com):

The SDRAM board architecture is shown in Figure 5.

Notes

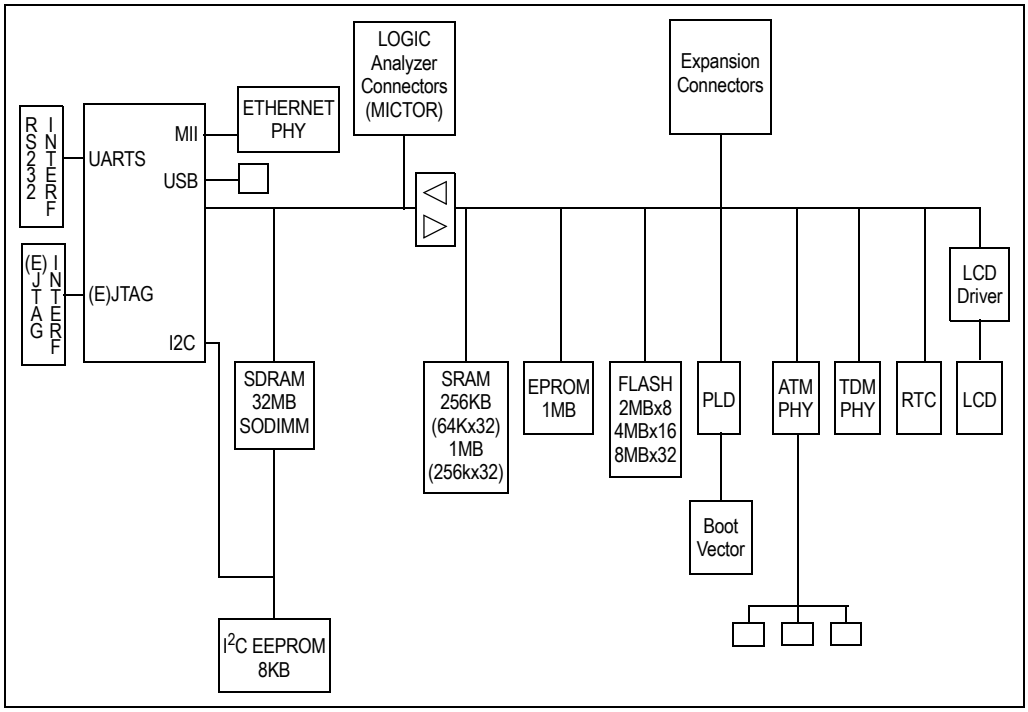

Figure 5 79EB355 Evaluation Board Block Diagram

Note: The RC32351 does not have I^2C or TDM bus interfaces.

References

RC32355 Data Sheet - IDT Inc.

RC32351 Data Sheet - IDT Inc.

RC32355 User Reference Manual - IDT Inc.

RC32351 User Reference Manual - IDT Inc.

79EB355 Evaluation Board Manual - IDT Inc.

79EB351 Evaluation Board Manual - IDT Inc.

Application Note 260 - SDRAM Architecture, Signals, and Routing - Paul Snell, IDT Inc.