Using the 79RC32438 Verilog Model

Application Note AN-431

Notes

By Rakesh Bhatia

Introduction

The RC32438 Verilog Model is designed to help verify correct connectivity on a PCB and/or the functionality of an FPGA interface. This document describes the contents of the available package and explains how to use the model.

Contents of the Verilog Model Package

The available package is composed of the following:

- MIPS 4Kc ("Jade") VMC model. This is a protected form of the CPU RTL using the SWIFT language.
- Encrypted RC32438 RTL.
- Simple boot memory model attached to chip select 0 - csn[0].
- Optional Simple DDR memory model attached to DDR chip select 0 - ddrcsn[0].
- System model that instantiates everything and creates the clocks, resets, and boot vector.

In addition to the above, the following files are provided:

- Makefile — Used to compile the executable VCS simulator.
- all_rtl-jade-ethinc.vp — All encrypted RC32438 RTL (except for Jade CPU core and encrypted Ethernet include file).
- boot_mem.v — Simple model of a 16-bit Boot ROM attached to device chip select 0.
- eth.v — Encrypted include file required for Ethernet block.
- jade_vmc_model.vcs.v — MIPS-4Kc VMC model.
- memory.jade_config — Used to customize MIPS-4Kc VMC model. This file should not require modification. See MIPS 4Kc Integrator's guide documentation for more details.
- system.v - Top-level Verilog file that instantiates everything and creates the clocks and resets
- program.srec - Sample program S-Record file.
- program.dis - Sample program disassembly.
- memmod0_0.mem - 8-bit wide hex memory image (LSB) loaded by the boot memory model.
- memmod0_1.mem - 8-bit wide hex memory image (MSB) loaded by the boot memory model.

Additional Requirements

In addition to the above, the following tools / licenses are required to use the Verilog Model effectively:

- FlexLM License File
- VCS 6.1 (Synopsys)
- SignalScan (or a waveform viewer tool)
- Executable from Unix

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The Verilog Model may be compiled using the VCS Verilog compiler. It has only been tested with version 6.1. The Jade VMC model requires a Flex license from MIPS (www.mips.com). An optional DDR Verilog memory model may be downloaded from Micron at www.micron.com (e.g. MT46V16M16). Sample boot code is provided and is automatically loaded into the boot memory model at startup. A user's own boot code may be used by replacing one or both of the hex image files. Several helper scripts are provided to convert S-Records into the required hex format.

Test Bench

Figure 1 below shows the sample test bench used in this model. Individual users can vary this test bench as required.

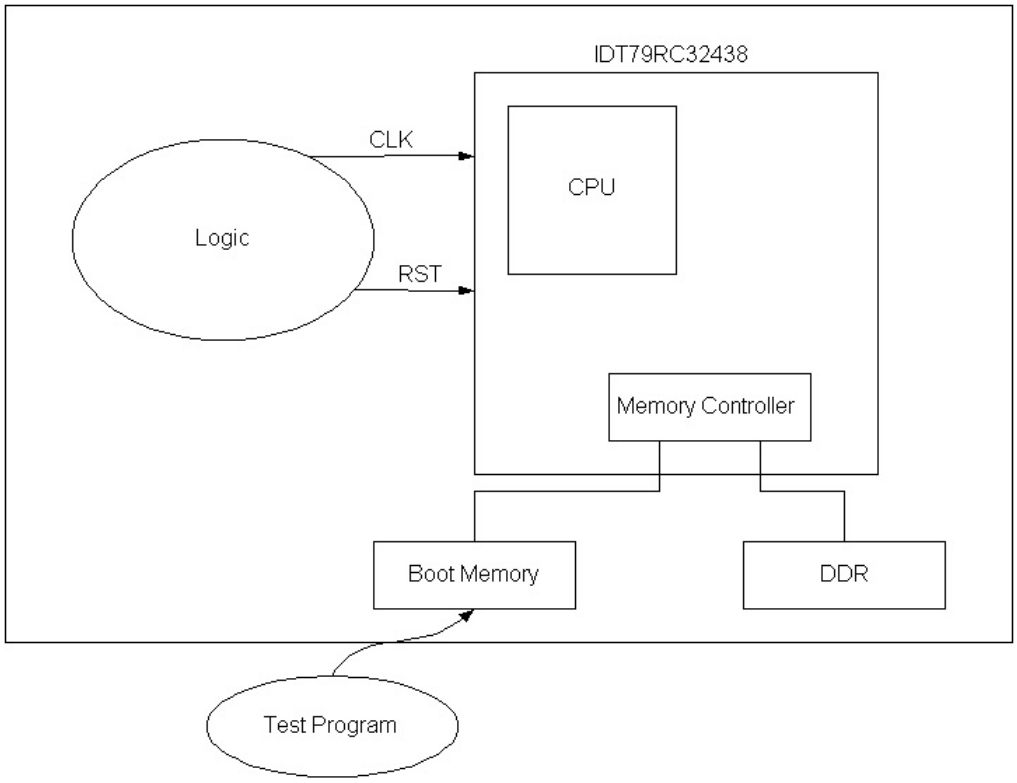

Figure 1 RC32438 Sample Test Bench

Using the Verilog Model

This section describes the various steps involved in using the model.

Compiling the Verilog Simulator

a) Customize the Makefile as follows:

- Choose the appropriate VCS command/path.
- Link in any desired PLI for signal dumping (e.g. Signal Scan, Debussy, etc.).
- Add any of your own RTL files.

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b) Customize the system.v file as follows:

- Instantiate any of your own models.
- Modify clocks, resets, pull up/down resistors, etc.
- Modify the boot vector (data driven during cold reset).
- Modify Signal Scan recording options or use your own.

c) Type 'gmake' to build the rc32438_bfm executable.

Compiling a Test

If you are using the sample test, skip this part and go to the next section, Running a Simulation.

If you are not using the sample test, perform the following steps:

- Generate an S-Record file with your existing compiler/tool chain.
- Convert the .srec format into a hex format required by the boot memory model. The following three helper scripts are provided for this:

  memmake — This is a Perl script that calls the next two scripts with parameters.

  srec2mem — This is an executable for Solaris that converts the S-Records into an intermediate memory image.

  memsplit — This is an executable for Solaris that converts that output of srec2mem into the 8-bit wide memory image file(s) required by the boot memory model.

  Note: To boot in 8-bit mode, it is necessary to change the memmake script. The '-o h' argument must be changed to '-o b'. Also, in this mode, only one hex image file is required:

  memmod0_0.mem.

Running a Simulation

Make sure that the Flex license from MIPS is correctly installed

Type in 'rc32438_bfm' from the command line

The simulation can be terminated by writing to the special offset address of 0x30002C in Device0 space.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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