QUALITY SEMICONDUCTOR, INC.

# High-speed Clocking Device Power Supply Decoupling

**Application Note AN-43**

In high-speed digital system, when all of the integrated circuits (IC) are dynamically switching, much noise can be coupled into the $V_{CC}$ supply and hence affect the IC performance. It is particularly important for a clocking device to have an adequate and proper decoupling. A good decoupling technique can minimize the power supply noise and keep the clocking output at its best quality. This is also true for a phase-locked loop based clock driver with internal analog circuits that can be sensitive to the power supply noise. Most decoupling practices use a capacitor to filter out the $V_{CC}$ noise as well as providing the instantaneous current for transient switching to prevent the local supply voltage dip. Some guidelines for decoupling clock buffers are given below.

1. Choosing the capacitor value based on the device loading. The bypass capacitor should be able to supply the transient current. For example, a clock driver with 10 outputs each driving a 70Ω transmission line (typical PCB trace impedance), the total current required is 10x5V/ 70Ω=714mA. Assuming an allowable $V_{CC}$ drop of 30mV, an output edge rate of 2ns, and first order calculation (I= CdV/dt =714mA), the minimum capacitor value is 714mA x 2ns / 30mV = 0.047µF. Therefore, the lower the line impedance, the higher the current required, and hence the bigger bypass capacitor. Normally, the minimum capacitor required is relatively small compared to the frequency bypass capacitor that also supplies the transient current.

2. Choosing the capacitor value based on the noise filtering range. Capacitors are not ideal. At certain frequency, they do not act like a capacitor but an effective series inductor or an effective series resistor. Therefore, at least two capacitors representing different capacitance range should be used to effectively filter a wider bandwidth of noise. The conventional approach is to connect a big capacitor such as 10µF to the $V_{CC}$ pins of each IC. It acts as a low frequency bypass and provides the transient current required. By connecting a small capacitor such as 0.1µF to each $V_{CC}$ pin, it acts as a high frequency bypass. If space permits, a third capacitor such as 0.01µF is recommended. This will provide a broad range of noise filtering and current supply.

3. Using capacitors with low inductance characteristic is essential. Surface-mount capacitors are recommended over the lead capacitors for its much smaller inductance. Tantalum or aluminum electrolytic capacitors are good small (0.1µF) decoupling capacitors, while MLC (multilayer ceramic) capacitors are suitable big (10µF) bypass capacitors. All capacitors should be placed as close as possible to each supply pin.

Some QSI clock management products have separate digital ($V_{CC}$) and analog/quiet ($AV_{CC}$ / $V_{CCQ}$) power supplies. In normal digital environment, it is not necessary to supply different power to analog $V_{CC}$ and digital $V_{CC}$. They can be connected to the board $V_{CC}$ with decoupling technique mentioned above. However, in some noisy environments, it is necessary to isolate the $AV_{CC}$ from $V_{CC}$. Practices such as adding a choke, a ferrite bead, a voltage regulator, or a small resistor (10~15Ω forming a low pass filter) are common. The users should be careful when adding a resistor. Depending on the current drawn into the analog circuit, the resistor can actually cause a large voltage drop, and force the $AV_{CC}$ operates out of its recommended range. For example, supplying $V_{CC}$ = 4.5V with a 47Ω resistor, there will be a voltage drop of 0.47V when current drawn by the analog circuit is 10mA. It results in the $AV_{CC}$ of 4.03V and can fail the IC's operation. Therefore, if a resistor is used, it is necessary to adjust its value in accordance to the design environment so that the $AV_{CC}$ will operate within its recommended range while composing an effective filter. Figure 1 shows a common decoupling approach. Under typical condition, the maximum trace length from a connector pad to the power plane via is 0.25 inch (assumes a 20-mil trace width).

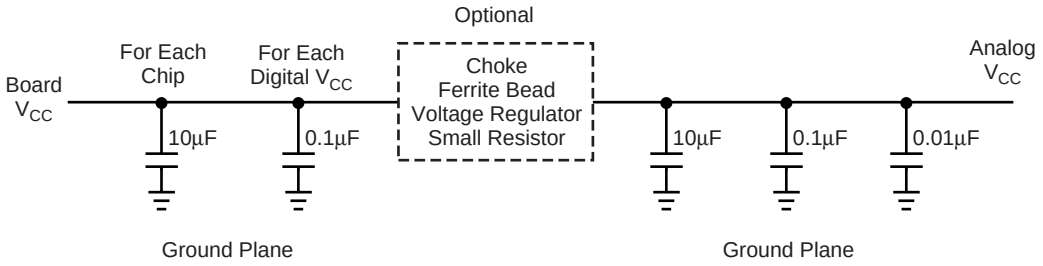


**Figure 1.**