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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## 4286 Group

### LVD/Clock Control

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#### 1. Summary

This document describes how to set the LVD/clock control of the 4286-group microcomputer.

#### 2. Introduction

The application example presented in this document applies to the microcomputers listed below for use under the conditions specified.

- Microcomputer : 4286 group

### 3. How to Set the LVD/Clock Control

#### 3.1 Clock Control

The system clock can be selected as shown in Table 3.1 by using or not using a frequency divide instruction. Figure 3.1 shows a configuration of the clock control circuit.

Table 3.1 Selection of the System Clock <sup>Note 1</sup>

	System clock	Instruction clock <sup>Note 2</sup>
Frequency divide instruction not used	$f(X_{IN})/8$	$f(X_{IN})/32$
CCK instruction executed	$f(X_{IN})$	$f(X_{IN})/4$
CCK2 instruction executed	$f(X_{IN})/2$	$f(X_{IN})/8$
CCK4 instruction executed	$f(X_{IN})/4$	$f(X_{IN})/16$

Note 1: Be sure that the selected system clock cycle is greater than or equal to the minimum instruction execution time (2.0  $\mu$ s).

Note 2: The instruction clock is the fundamental clock to control the CPU. The instruction clock is derived from the system clock by dividing it by 4. One instruction clock cycle produces a 1-machine cycle period <sup>Note 3</sup>.

Note 3: The machine cycle refers to the fundamental clock cycles synchronously with which instructions are executed.

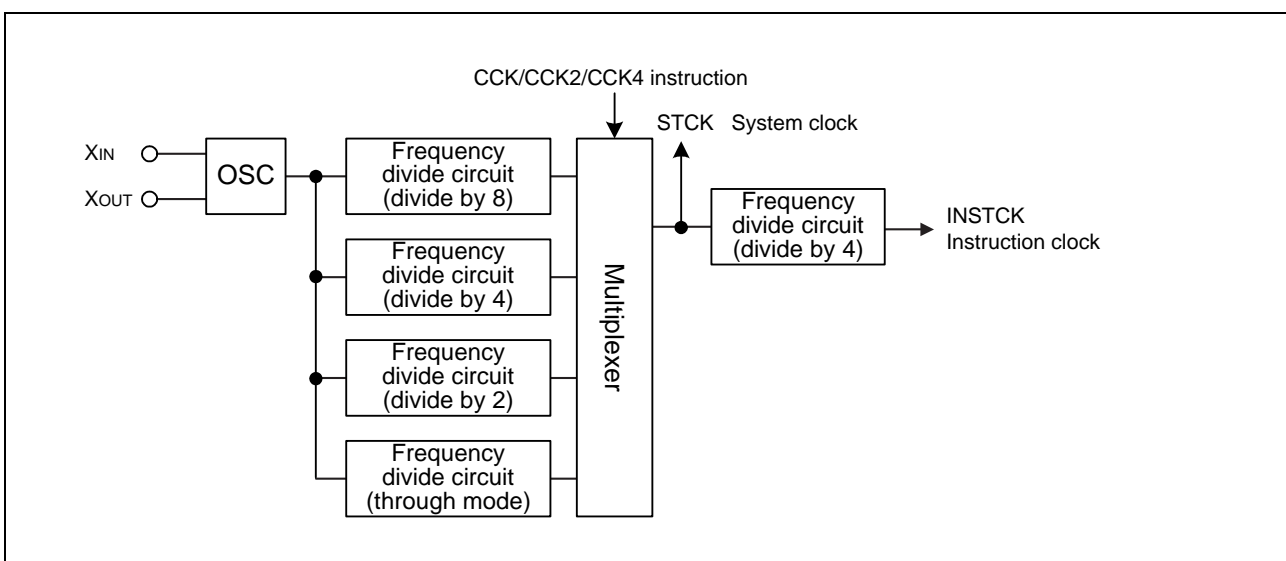


Figure 3.1 Configuration of the Clock Control Circuit

To use the frequency divide instructions (CCK/CCK2/CCK4 instructions), there are no limitations to their instruction execution address. Note, however, that the CCK, CCK2 and CCK4 instructions are executable only once. These instructions, if any executed after execution of the same or another instruction, have no effect and, therefore, no operation is performed.

### 3.2 LVD

If the CLVD instruction is executed, the voltage value at which a reset is generated changes.

CLVD instruction Not executed

Reset generated: 1.5 V (when  $T_a = 25^\circ\text{C}$ )

Reset deactivated: 1.7 V (when  $T_a = 25^\circ\text{C}$ )

CLVD instruction Executed

Reset generated and deactivated: 1.7 V (when  $T_a = 25^\circ\text{C}$ )

Figure 3.2 shows the voltage-down detection circuit's operating signal waveform.

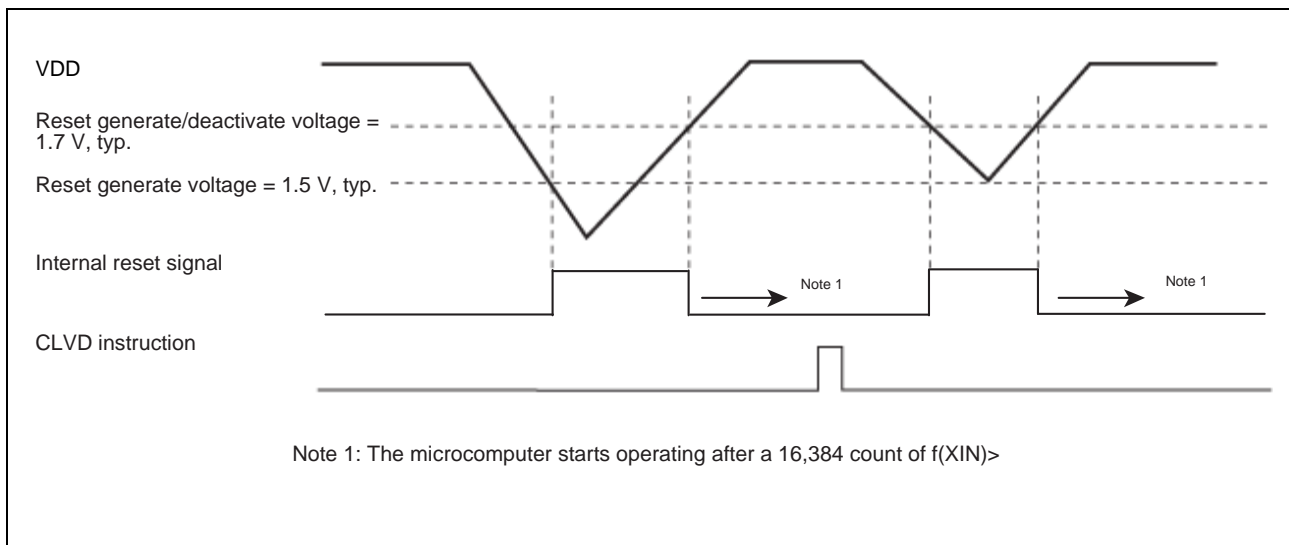


Figure 3.2 Voltage-Down Detection Circuit's Operating Signal Waveform

<Precautions>

The voltage-down detection voltage of this microcomputer is set below the lower-limit value of the power supply voltage stipulated as its recommended operating conditions. If, for example, the battery in an application system is replaced causing its power supply voltage to drop below the recommended operating voltage while the CPU is active and the clock stops oscillating erratically, not by an execution of the POF instruction, before the detection voltage (VDET) is reached. In that case, because no reset is generated, the system will not operate normally even when the power supply voltage rises above the recommended operating voltage again. Please be sure to check the resonator used in your product and the system clock frequency, and verify that your product operates satisfactorily with the resonator used.

Figure 3.3 shows the relationship between VDD and VDET.

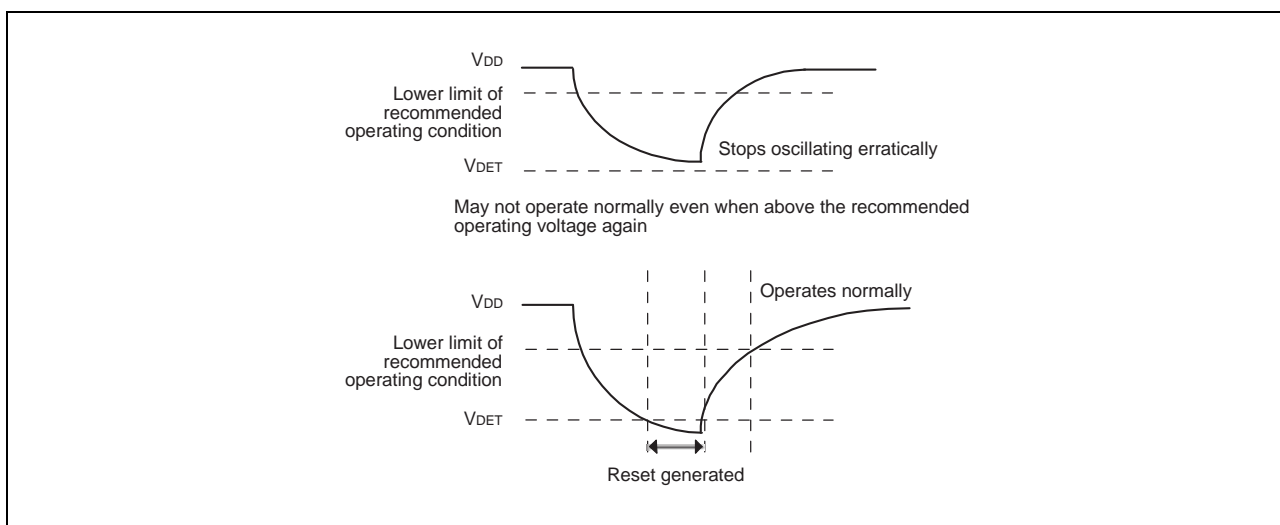


Figure 3.3 VDD and VDET

### 3.3 Frequency Divide Instructions and the CLVD Instruction

If you executed the CCK2 instruction, be sure to execute the CLVD instruction. However, this applies when operating with  $f(XIN) = 4 \text{ MHz}$ .

#### 4. Reference Documents

Datasheets

4286 Group Datasheet

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Technical news and technical updates

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REVISION HISTORY	4286 Group LVD/Clock Control
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Rev.	Date	Description	
		Page	Summary
1.00	2008.08.26	—	First Edition issued

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