Interfacing the RC32438 with the CompactFlash Storage Card

Application Note AN-397

Notes

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Introduction

The RC32438 device is a high performance, general-purpose, integrated processor that incorporates a 32-bit CPU core with a number of peripherals including:

- *A memory controller supporting double data rate SDRAM*
- *A separate memory/peripheral controller interfacing to EPROM, flash and I/O peripherals*
- *Two Ethernet MACs*
- *A 32-bit v.2.2 compatible PCI interface*
- *Other generic modules, such as two serial ports, I^2C, SPI, interrupt controller, GPIO, and DMA.*

The purpose of this document is to show the hardware interface between the RC32438 device and a CompactFlash storage card using the general memory and peripheral bus provided on the RC32438.

CompactFlash Modes

CompactFlash (CF) storage cards are required to support 3 modes of operation:

- *PC Card memory interface mode*
- *PC Card I/O interface mode*
- *True IDE mode.*

CF+ cards are not required to support the True IDE mode but may optionally do so. The task file registers provide the necessary registers for control and status information. One of the main differences between these modes is the way in which task file registers are mapped. For example, in the PC card memory interface mode, task file registers are mapped into common memory space. In the I/O interface mode and in the True IDE mode, these registers are mapped into the I/O address space. There are 8 registers in the Task File, and these are accessed by the address lines A0:A2, as described later in this document. The True IDE mode, described in this document, is the simplest to use with the RC32438 device.

True IDE Mode

A CF card is configured in True IDE mode only when the -OE input signal is grounded by the host during power-up. In this mode, the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In other words, no Memory or Attribute Registers are accessible to the host. The advantage of using True IDE mode is that it can be interfaced with a general bus on a system without using glue logic. Compared to the other two modes of operation, the True IDE mode requires only $\overline{CE1}$ to be asserted to perform a read or write operation. In the PC card memory or I/O modes, both $\overline{CE1}$ and $\overline{CE2}$ need to be asserted at the same time, which requires external logic gates.

RC32438 Memory and Peripheral Device Controller

The RC32438 device provides demultiplexed address and data bus and 6 chip selects. Flexible protocol configuration parameters include programmable wait states and post transaction delays. The various bus signals provided by the microprocessor are listed below:

MADDR[25:0] (address bus, MADDR[21:0] directly available as I/O pins, MADDR[25:22] are GPIO alternate functions)

MDATA[15:0] (data bus)

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OEN (output enable, may be used as Intel style read signal)

BWEN[1:0] (byte write enables, may be used as Intel style write signals)

RWN (Motorola style read/write signal)

CSN [5:0] (chip selects)

WAITACKN (configurable as Intel style wait signal or Motorola style transfer acknowledge signal)

BOEN (external data bus buffer output enable)

BDIRN (external data bus buffer direction).

Using some of these signals, a CF card can be connected to the memory and peripheral bus of the RC32438 device, as shown in the next section.

Hardware Interface

Figure 1 shows the hardware interface between a CF card and the RC32438 device. As shown in the figure, the interface requires minimum external logic. Unused signals in the True IDE mode and unused status signals are not shown. For clarity, power signals are also not shown.

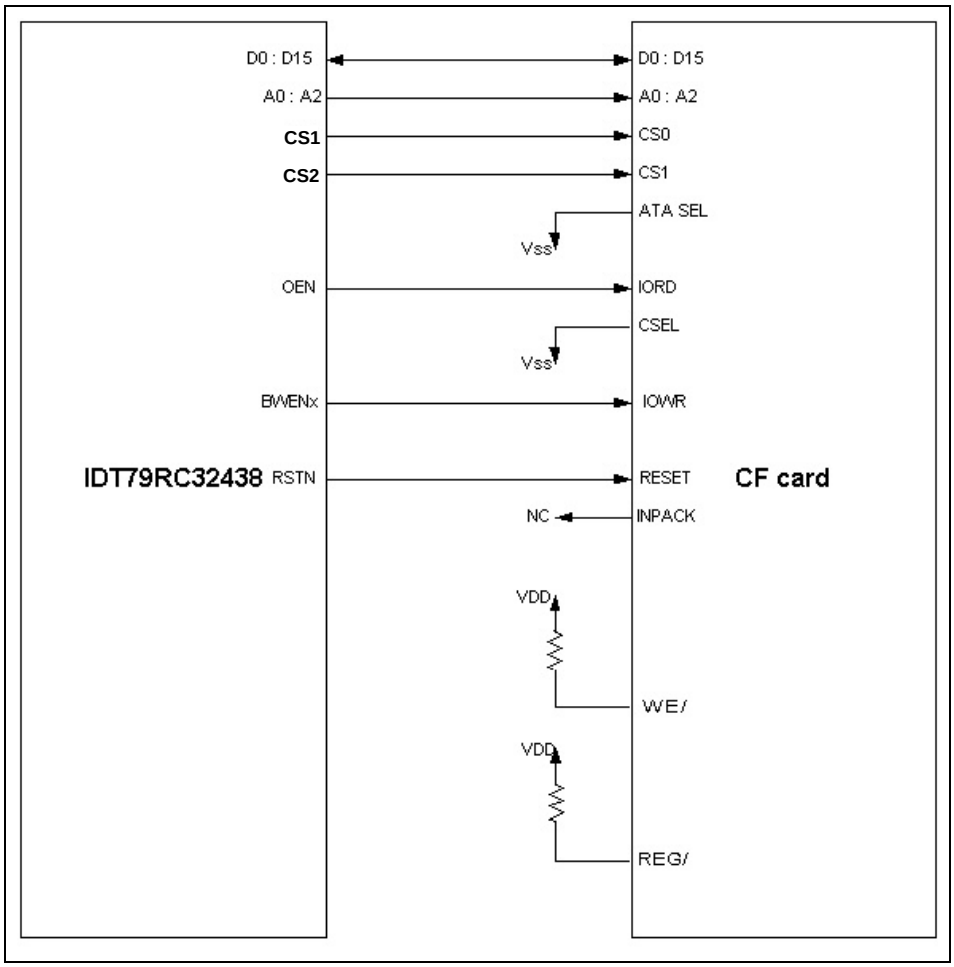

Figure 1 Example of CF Storage Card Interface to RC32438

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Signal Description

The features of various signals are described below:

D0:D15

In True IDE mode, all Task File operations are in byte mode on the low order bus and all data transfers use the 16-bit bus. The data bus D0:D15 provides a bi-directional path between the CF card and the micro-processor.

A0:A2

These signals are used to select one of the eight registers in the Task File.

$\overline{\text{CS1:CS2}}$

Chip selects are inputs to the CF card and are used to select either the Task File registers or Alternate Status register and device control register.

$\overline{\text{ATA SEL}}$

In order to ensure that the CF card is configured in True IDE mode, the host at power-up should ground the $\overline{\text{ATA SEL}}$ input pin to the CF card.

$\overline{\text{IORD}}$

The OEN signal of the RC32438 is asserted when data should be driven on by an external device on the memory and peripheral bus. This serves as a strobe to the $\overline{\text{IORD}}$ pin of the CF card, as specified in the True IDE mode spec.

$\overline{\text{CSEL}}$

This signal is used to configure a CF card as a Master or slave when multiple cards are being used in the system. In the above example, only one CF card is being used, therefore the $\overline{\text{CSEL}}$ is shown as grounded.

$\overline{\text{IOWR}}$

The IOWR/ signal serves as a strobe to pulse used to clock I/O data on the CF card's data bus into the storage card. The BWENx signals of the RC32438 provide this pulse as byte write enables.

$\overline{\text{Reset}}$

The RSTN signal of the RC32438 is asserted during a warm reset, thereby resetting the CF card.

$\overline{\text{Inpack}}$, $\overline{\text{WE}}$ and $\overline{\text{Reg}}$

These signals are not used in the True IDE mode.

Signals Not Used

The following CF card pins are not used or not connected in the example shown in Figure 1.

$\overline{\text{PCDIAG}}$: not used

$\overline{\text{DASP}}$: not used

$\overline{\text{INTRQ}}$: not used

IORDY: not used

$\overline{\text{IOIS16}}$: not used

Note that $\overline{\text{CD1}}$ and $\overline{\text{CD2}}$ should be connected to ground on the CF card.

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Timing

The interface shown in Figure 1 above will meet the timing requirements for the read and write transactions shown in the CompactFlash Card spec "CF+ and CompactFlash specification Revision 1.4". The RC32438 device offers several programmable timing parameters for read and write transactions occurring over its Memory and Peripheral bus. Depending upon the CompactFlash card used, it is recommended that the timings be verified and these parameters be programmed as required.

For read transactions, the programmable parameters are CSD, OED, RWS, PRD, and CSH. For write transactions, the programmable parameters include CSD, BWD, WW, PWD, CSH, and WDH. Using these programmable parameters provides for flexibility in choosing a CF card. Detailed descriptions and waveforms showing these parameters are shown in Chapter 6, Device Controller, of the RC32438 User Reference Manual. To provide a better view of the programmable parameters, an example of a read transaction is shown in Figure 2.

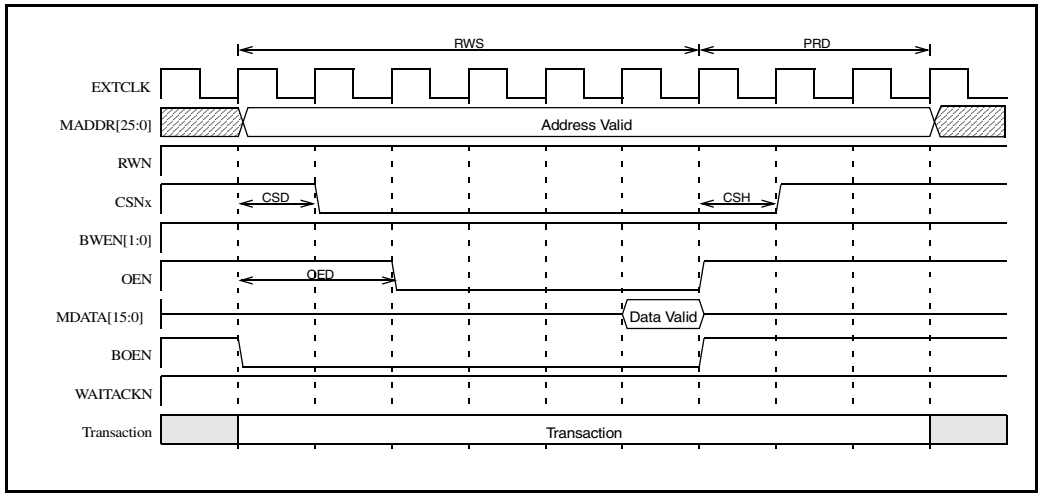

Figure 2 Generic Device Read Transaction

Conclusion

The memory and peripheral bus of the RC32438 device provides a simple-to-use and inexpensive method of interfacing to CompactFlash cards as described in this document. The actual logic or timing has not been verified in a lab environment.

References

1. IDT79RC32438 Integrated Communications Processor User Reference Manual
2. CF+ and CompactFlash Storage Card Specification Rev1.4 - CompactFlash Association

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