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38D5 Group

Timer X Operation (IGBT Output Mode: IGBT Control Signal Output)

1. Abstract

The following article introduces and shows an example of how to use the Timer X Operation (IGBT Output Mode: IGBT Control Signal Output) on the 38D5 Group device.

2. Introduction

The application explained in this document applies to the following MCU and parameter(s):
Applicable MCU: 38D5 Group
Oscillation frequency: 8 MHz

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the user system operating parameters.

3. Explanation of IGBT Control Signal Output

3.1 Description of IGBT Output Mode

The 38D5 Group MCU has IGBT output mode as one of the functions of Timer X (16-bit timer). In IGBT output mode, IGBT control signal is output from the TXOUT1 pin according to the timer X count value. When no trigger is input from INT0 pin, the period and the duty of IGBT control signal are determined by the timer X and the compare register 1 and the period does not change. When a trigger is input from the INT0 pin, the period and the the duty of IGBT control signal are determined by the timer X, the compare register 1, and the trigger input from INT0 pin and the period changes.

When the timer X output 1 edge switch bit (bit 5 at the timer X control register 1, address 002Eh) is set to 0 and start at "L" output is selected, the MCU operates as follows:

After the timer X count starts, "H" (Note) is output from the TXOUT1 pin by the trigger input from INT0 pin or the timer X underflow. ("L" (Note) is output until a trigger is input from the TXOUT1 pin or the timer X underflows in the first period after the timer X counts starts). When the timer X count value and the value of the compare register 1 are equal, "L" (Note) is output. The trigger input from INT0 pin is valid while "L" (Note) is output from the TXOUT1 pin. As for trigger input, the following options are available.

- Active edge (falling or raising)
- Sampling clock of the noise filter (determined as a valid signal when the level has corresponded four times continuously in the sampling clock)
- Four types of delay time

When the timer X output 1 control bit or the timer X output 2 control bit (bit 3 or 4 at the timer X control register 1) is set to 1, the timer X count stop bit (bit 6 at the timer X mode register, address 002Dh) becomes 1 by input from INT1 or INT2 pin and the timer X stops counting. Then, output from TXOUT1 pin can be fixed to "L" (Note). The active edge (falling or rising) can be selected for each input from INT1 pin and INT2 pin.

After timer X count starts, the previous set value of the compare register 1 is valid until a trigger is input from INT0 pin or timer X underflows. However, "L" is output regardless of the set value of compare registers in the first period after the timer X count starts.

When using IGBT output mode, confirm the following points. (Also refer to section 4, Notes on timer X: IGBT output mode of this document).

- Set the port direction register shared with the INT0 pin to input mode and the port direction register shared with TXOUT1 pin to output mode.
- When using the TXOUT1 pin switching to port output, the port latch value may be changed by the read modiy write instructions to the port P6 register.
- The port shared with TXOUT1 pin (P65) becomes input mode at reset. Therefore, stablize the level externally by using pull-down resistor or pull-up resistor and so on.
- Set the timer X register (expansion) to "00h".

Note. When the timer X output 1 edge switch bit is set to 1, this level is inverted.

3.2 IGBT Control Signal Output

Outline:
- IGBT control signal of 20 μs period and five μs "H" width is output, starting from "L" output. (Active level for IGBT is "H")
- When a trigger signal ("H"→ "L") is input to the INT0 pin during "L" output, the output level becomes "H" and the timer X restarts from the setting of the timer X latch value.

Specifications:
- Select f(XIN) = 8 MHz (One count 125 ns) as the timer X count source.
- The initial value of the timer X is 159 and the timer X underflow period is 20 μs.
- The set value of the compare register is 120 and "L" width is 15 μs when there is no trigger input from the INT0 pin. Therefore, the "H" width becomes 5 μs.
- Select f(XIN)/2 for the noise filter sampling clock and "no delay" as an external trigger delay time.
- The active edge for the INT0 input signal is the falling edge.

Figure 3.1 shows the Connection Diagram of Timer and Frequency Division Ratio, Figure 3.2 shows the TXOUT1 Output Waveform, Figure 3.3 and 3.4 show the Relevant Register Settings, and Figure 3.5 shows the Control Procedure.

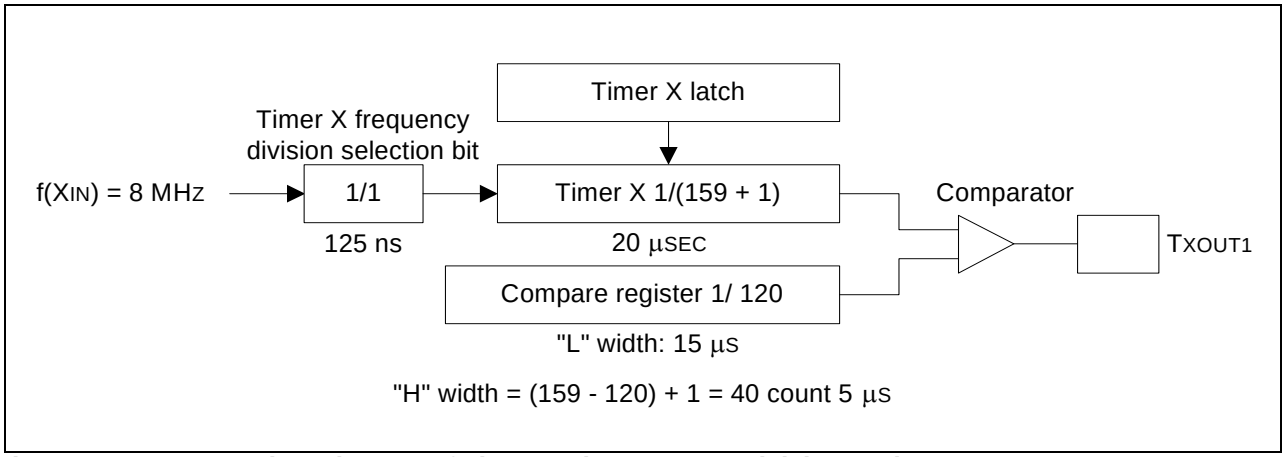


Figure 3.1 Connection Diagram of Timer and Frequency Division Ratio

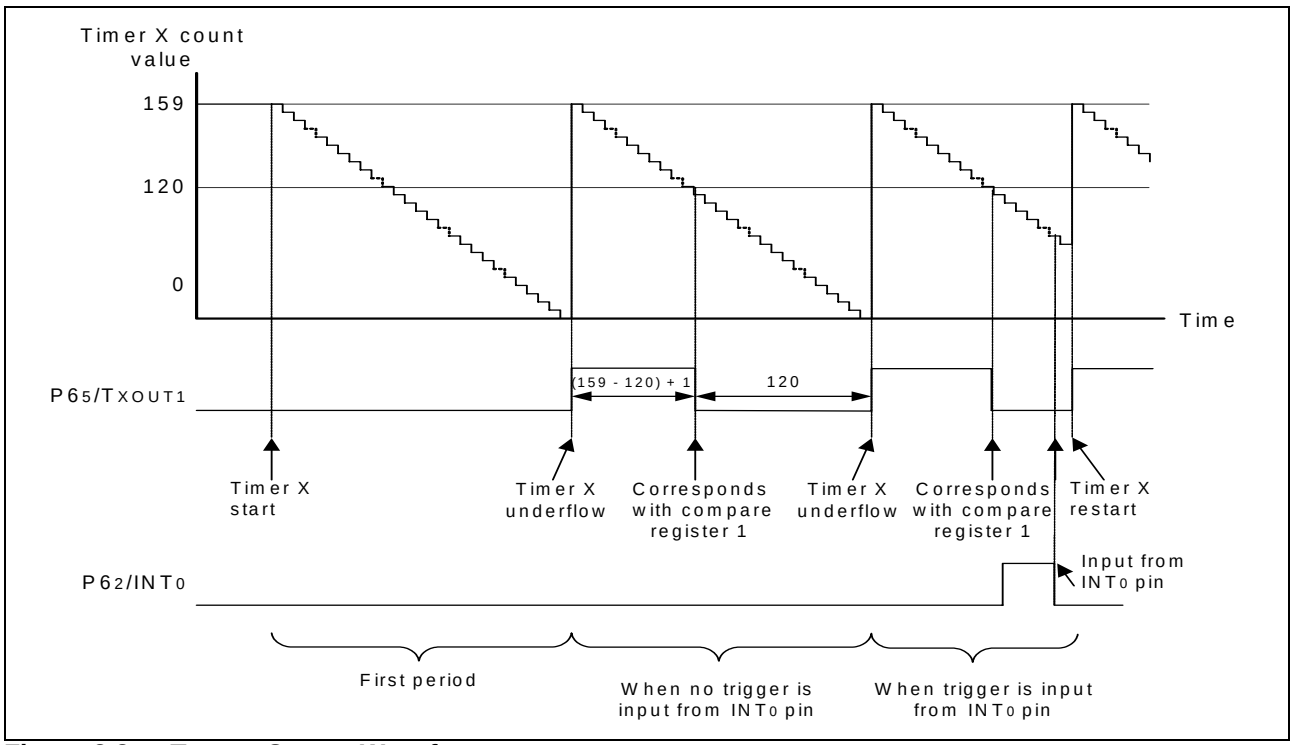
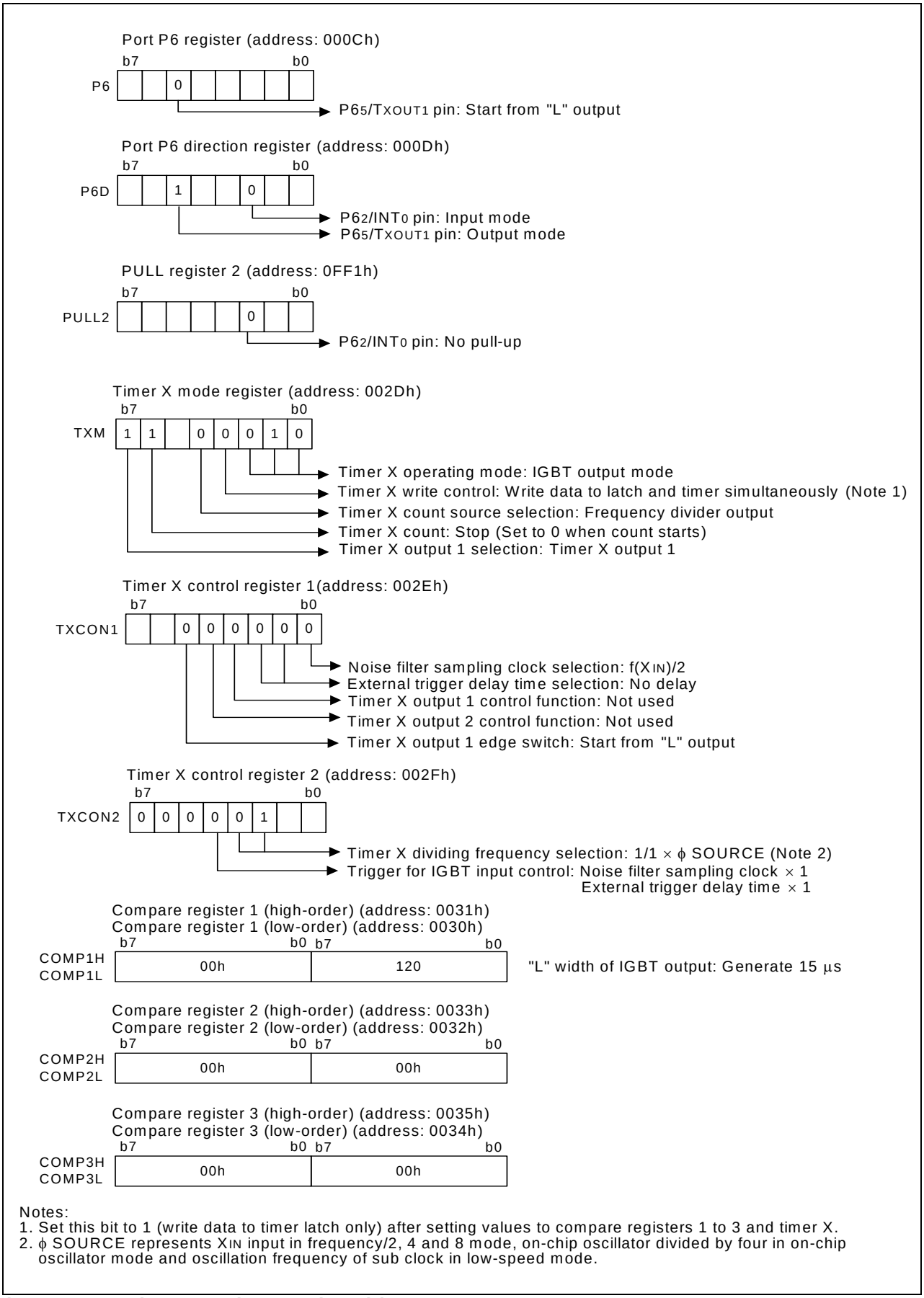


Figure 3.2 TXOUT1 Output Waveform



Notes:
1. Set this bit to 1 (write data to timer latch only) after setting values to compare registers 1 to 3 and timer X.
2. ϕ SOURCE represents XIN input in frequency/2, 4 and 8 mode, on-chip oscillator divided by four in on-chip oscillator mode and oscillation frequency of sub clock in low-speed mode.

Figure 3.3 Relevant Register Settings (1)

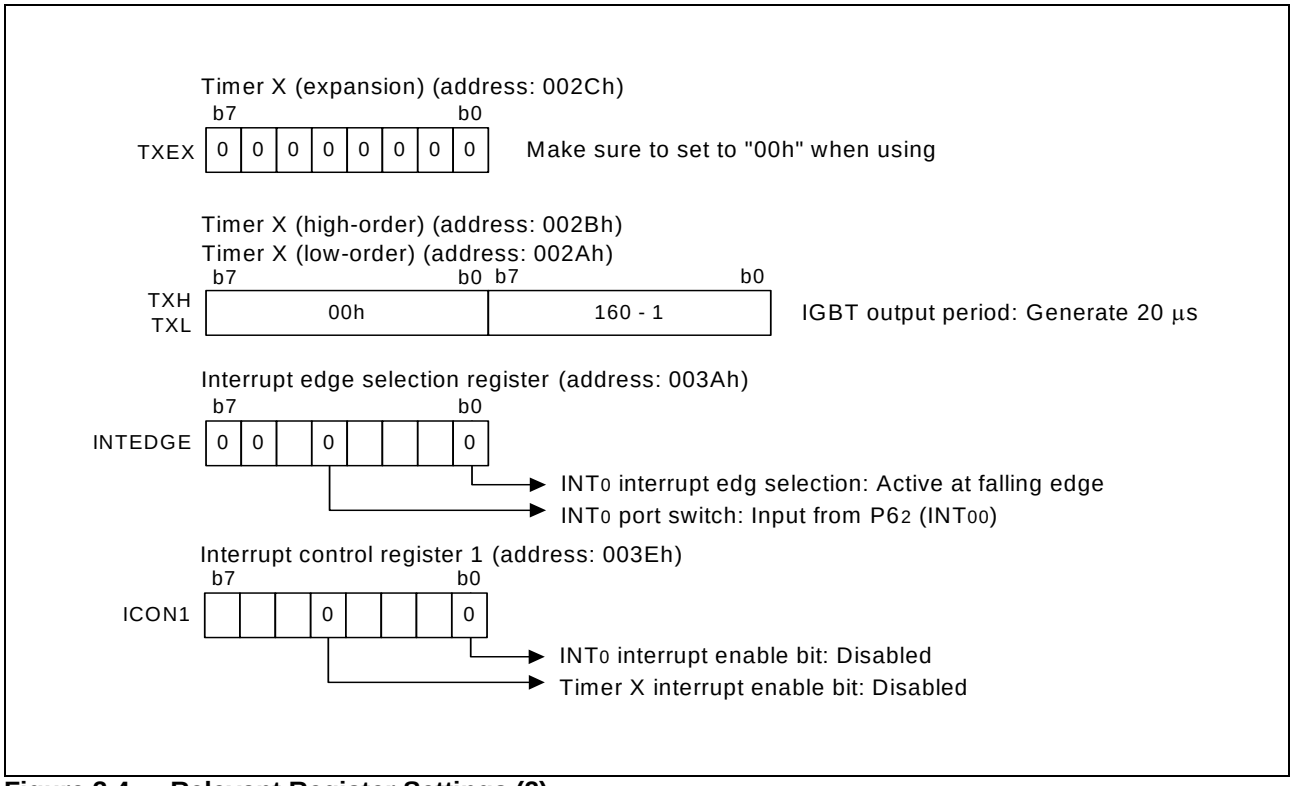
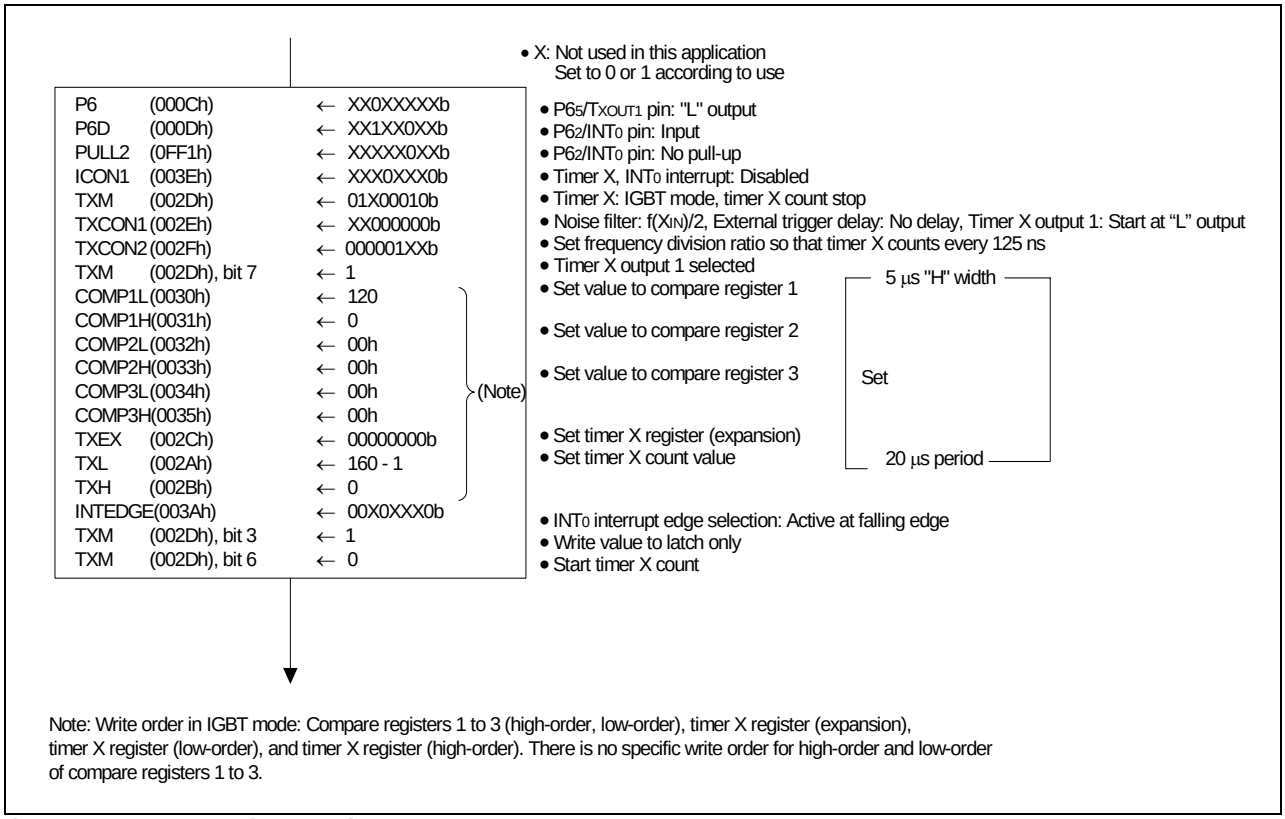


Figure 3.4 Relevant Register Settings (2)



Note: Write order in IGBT mode: Compare registers 1 to 3 (high-order, low-order), timer X register (expansion), timer X register (low-order), and timer X register (high-order). There is no specific write order for high-order and low-order of compare registers 1 to 3.

Figure 3.5 Control Procedure

4. Notes on Timer X (IGBT Output Mode)

(1) Write order of the timer X

In IGBT output mode, do not write 1 to the timer X register (expansion). When 1 is already writtent to the timer X register (expansion), make sure to write 0 to the register before using. The write order to registers is the compare registers 1 to 3 (high-order and low-order) first, followed by the timer X register (expansion), the timer X register (low-order) and the timer X register (high-order). There is no specific write order for high-order and low-order of compare registers 1 to 3. Make sure to write data to both high-order and low-order of compare registers 1 to 3 and timer X registers.

(2) Read order of the timer X

The read order of the timer X is common in all mode, which is the timer X register (expansion) first, followed by the timre X register (high-order) and timer X register (low-order). When reading the timer X register (expansion) is not necessary, the read order is the timer X register (high-order) first and then the timer X register (low-order). There is no specific read order for the compare registers 1 to 3.

Write and read operations to the timer X registers should be performed in 16-bit units. If write/read operation is aborted, the normal operation can not be performed.

(3)Writing to the timer X

One of two options (simaltaneous writing to both the timer and the timer latch or writing to the timer latch only) can be selected at the timer X write control bit (b3) of the timer X mode register (adrress: 002Dh). When selectiong writing to the latch only, a value is set to the timer latch after writing a value to the address of the timer X and timer is updated at the next underflow. After reset is released, the timer X write control bit becomes 1 (simultaneous writing to both the timer and the timer latch) and when a value is written to the address of timer X, the value is set to both timer and timer latch at the same time. Even when selecting writing to the timer latch only, writing to high order latch and an underflow occurs almost at the same timing, the value is set to the timer and the timer latch simultaneously. At this time, count may be stopped during writing operation to the high-order timer latch. (Refer to Section 5. “Notes on Timer Count Stop When Writing to the Timer Latch Only” in this document).

Do not switch the timer count source during timer count operation. Switch timer count source only after count operation is stopped.

(4) Setting of the timer X mode register

Make sure to set the write control bit of the timer X mode register to 1 (writing to the latch only) in IGBT output mode.

(5) Timer X output control function

When using the timer X output control function (INT_1, INT_2) at setting IGBT output mode, set INT_1, INT_2 to “H” when active at the falling edge is selected and “L” when active at the rising edge is selected before switching to IGBT output mode.

(6) Port $P6_5$ latch

When reading the port P6 while waveform is output from the T_{XOUT1} pin in IGBT mode, the pin state (level) is read. When executing read modify write instructions at this time, the pin state (level) is reflected to the port latch and the value at the bit 5 may be changed. Then, if the $P6_5/T_{XOUT1}$ pin is switched from timer X output to I/O port (output mode) after this, the unexpected level may be output due to the changed value. Therefore, when swithcing, set a given value to the port latch first.

Read modify write instruction: Read one-byte of data from memory, modify the data, and write the data back to the original memory. CLB, SEB, ASL, LSR, ROL, ROR, RRF, DEC, INC,COM

(7)When 0000h is set to the compare register 1 (Previous value: other than 0000h)

"H" signal is output for one period at the following period after writing data to the timer X and the compare register 1. Then, "L" signal is output while the timer X counts down "3FFFFh" and this operation is repeated. (The timer X output 1 edge switch bit is set to 0: When "L" output start and no INT0 trigger input)

Figure 4.1 shows the Example of IGBT Control Signal Output When 0000h is set to Compare Register 1 (Previous value: Other Than 0000h)

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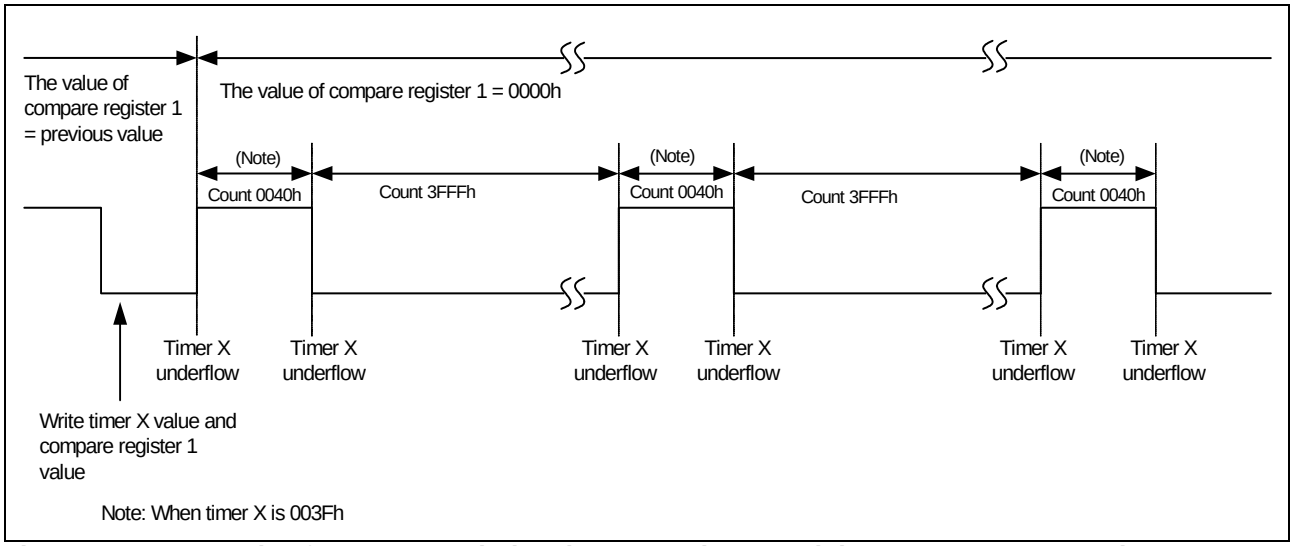

Figure 4.1 Example of IGBT Control Signal Output When 0000h is set to Compare Register 1 (Previous value: Other Than 0000h)

(8) When setting the same values to the timer X and the compare register 1

TXOUT1 output becomes "H" at the underflow immediately after writing values to the timer and the compare register 1. Then, the timer X value is reloaded and corresponds with the value of the compare register 1 and TXOUT1 output becomes "L". The width of "H" at this time is one count of the timer X count source. (The timer X output 1 polarity switch bit is set to 0: When starting from "L" output start and no INT0 trigger input)

Figure 4.2 shows the Example of IGBT Control Signal Output When Same Value is set to Timer X and Compare Register 1.

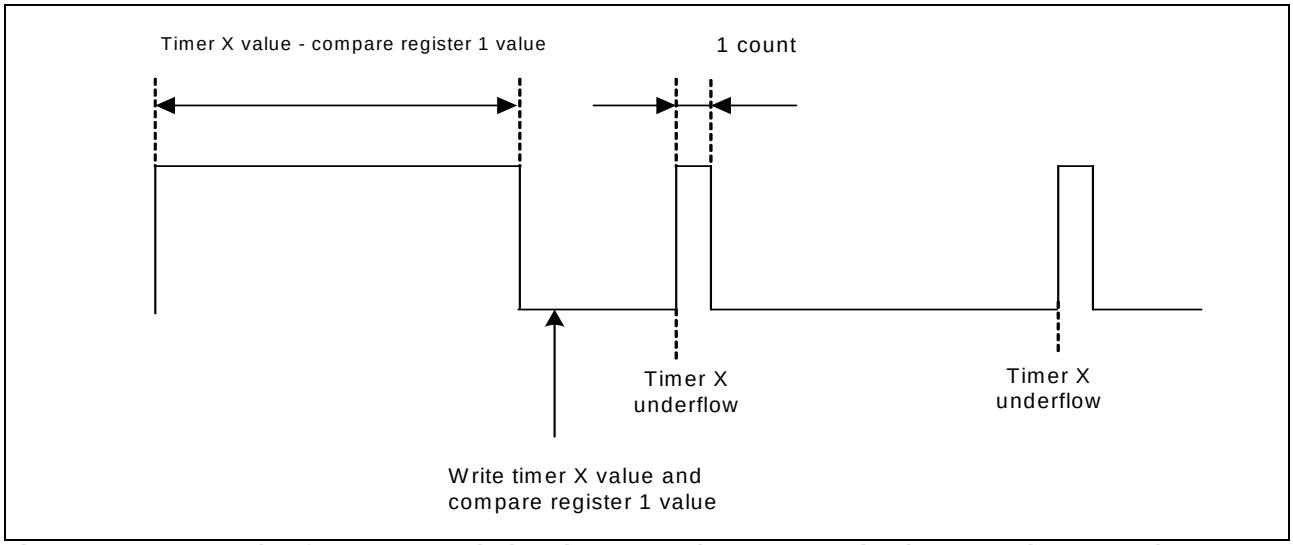

Figure 4.2 Example of IGBT Control Signal Output When Same Value is set to Timer X and Compare Register 1

(9) Time between trigger input to INT0 pin and invert of TXOUT1 output waveform polarity

In IGBT output mode, a trigger input from the INT0 pin is valid only while the opposite polarity level from the active level is output. (When “H” is active in IGBT, the trigger input is valid only while the TXOUT1 output level is held “L”). The TXOUT1 output level is switched to the active level by valid trigger input from the INT0 pin. (When “H” is active in IGBT, the output level of TXOUT1 is switched to “H”). At this time, time difference is generated between the input of the valid edge of INT0 signal and the polarity invert to the active level. This time difference is caused by level determination time with the noise filter (determine whether the signals become the same level for continuous four times) and delay time by the delay circuit.

The sampling clock of the noise filter can be selected by the noise filter sampling clock selection bit (bit 0 at the timer X control register 1). Delay time by the delay circuit can be set by the external trigger delay time selection bits (bit 2 and 1 at the timer X control register 1).

Figure 4.3 shows the Example of IGBT Control Signal Output of TXOUT1 Pin by Trigger Input to INT0 pin.

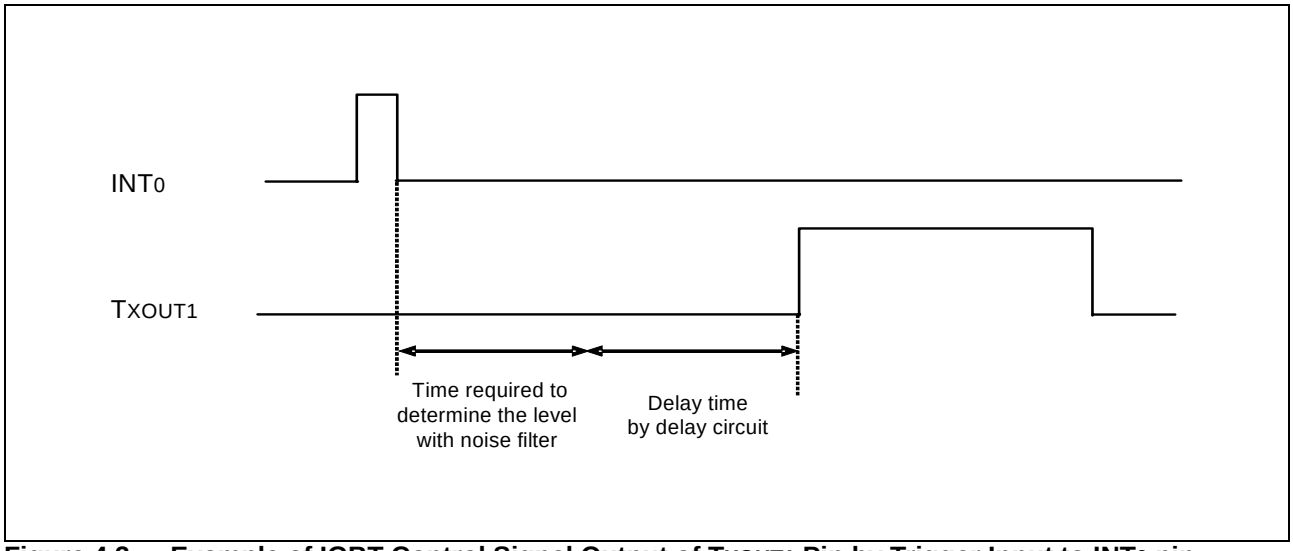

Figure 4.3 Example of IGBT Control Signal Output of TXOUT1 Pin by Trigger Input to INT0 pin

5. Notes on Timer Count Stop When Writing Data to Timer Latch Only

When writing to the timer latch (Note) and the timer X underflow occurs almost simultaneously while selecting writing to the timer latch only, the timer X operate as follows.

- Timer count source ≤ Internal system clock ϕ
  Timer count does not stop and starts counting with the new timer value.

- Timer count source > Internal system clock ϕ
  Timer count stops for the maximum one cycle of the system clock. When write operation (internal system clock ϕ) is complete, count starts with the new timer value.

Note: Timer 2, 3, or 4: Timer latch, Timer X or Y: High-order timer latch

6. Sample Programming Code

Download a sample program from the Renesas Technology website.
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7. Reference Document

Datasheet
38D5 Group Data sheet
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REVISION HISTORY	38D5 Group Timer X Operation (IGBT Output Mode: IGBT Control Signal Output)

Rev.	Date	Description	
		Page	Summary
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