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## 38D5 Group

### RRF Register Application

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#### 1. Abstract

The following article introduces and shows an example of how to use the RRF Register Application on the 38D5 Group device.

#### 2. Introduction

The application explained in this document applies to the following MCU and parameter(s):

Applicable MCU: 38D5 Group

Frame frequency: 8 MHz

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

### 3. Contents

#### 3.1 RRF Register Application

Outline: Comparison between how to set display data on the LCD panel and the number of cycles when using the RRF register and instruction.

Specifications:

- Segment output SEG0 to SEG23 and common COM0 to COM3 are used.
- Frame frequency = 61 Hz
- Duty ratio = 4, Bias value = 1/3
- “M38d5” is displayed

Number of bytes: 240 bytes when using the RRF instruction, 200 bytes when using the RRF register

Number of cycles: 480 cycles when using the RRF instruction, 320 cycles when using the RRF register

Figure 3.1 shows a Segment Allocation Example, Figure 3.2 shows the Circuit Example (When Using External Dividing Resistor), Figure 3.3 shows the LCD Display RAM Map, Figure 3.4 shows a LCD Display RAM Setting Example, Figure 3.5 and 3.6 show the Relevant Register Settings, and Figure 3.7 shows the Control Procedure When Using RRF Instruction, and Figure 3.8 shows the Control Procedure When Using RRFR Register.

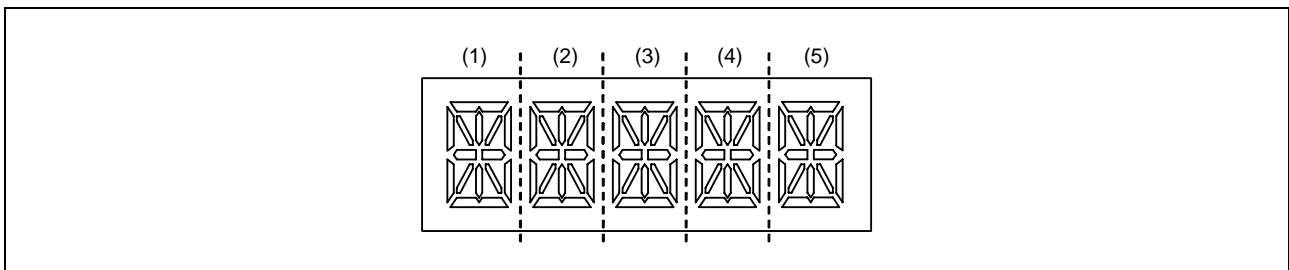


Figure 3.1 Segment Allocation Example

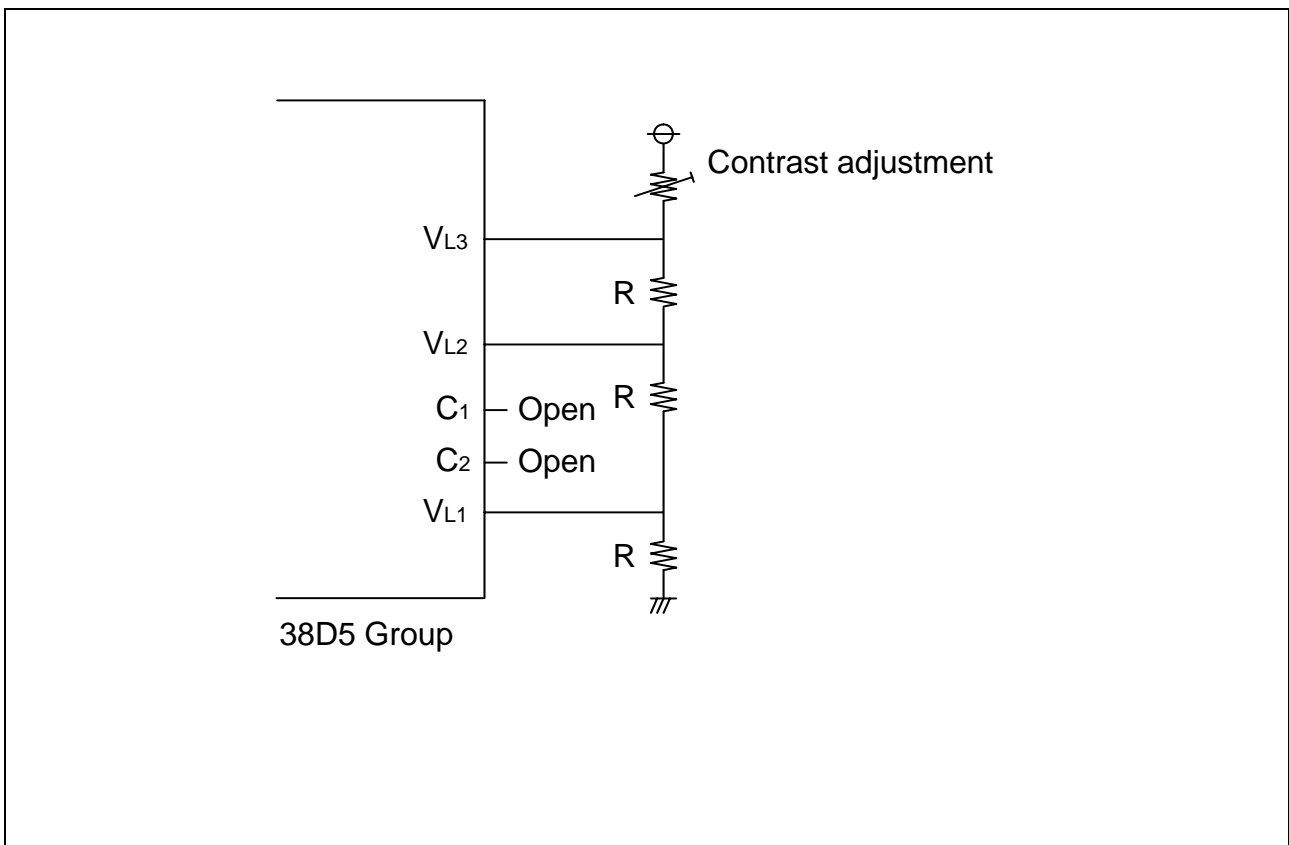


Figure 3.2 Circuit Example (When Using External Dividing Resistor)

		4COM × 36SEG									
		Bit		7	6	5	4	3	2	1	0
Address											
0840h	LRAM0	Not used (Can generally be used as RAM)						SEG0			
0841h	LRAM1							SEG1			
0842h	LRAM2							SEG2			
0843h	LRAM3							SEG3			
0844h	LRAM4							SEG4			
0845h	LRAM5							SEG5			
0846h	LRAM6							SEG6			
0847h	LRAM7							SEG7			
0848h	LRAM8							SEG8			
0849h	LRAM9							SEG9			
084Ah	LRAM10							SEG10			
084Bh	LRAM11							SEG11			
084Ch	LRAM12							SEG12			
084Dh	LRAM13							SEG13			
084Eh	LRAM14							SEG14			
084Fh	LRAM15							SEG15			
0850h	LRAM16							SEG16			
0851h	LRAM17							SEG17			
0852h	LRAM18							SEG18			
0853h	LRAM19							SEG19			
0854h	LRAM20							SEG20			
0855h	LRAM21							SEG21			
0856h	LRAM22							SEG22			
0857h	LRAM23							SEG23			
0858h	LRAM24							SEG24			
0859h	LRAM25							SEG25			
085Ah	LRAM26							SEG26			
085Bh	LRAM27							SEG27			
085Ch	LRAM28							SEG28			
085Dh	LRAM29							SEG29			
085Eh	LRAM30							SEG30			
085Fh	LRAM31							SEG31			
0860h	LRAM32							SEG32			
0861h	LRAM33							SEG33			
0862h	LRAM34							SEG34			
0863h	LRAM35							SEG35			
						COM3	COM2	COM1	COM0		

Figure 3.3 LCD Display RAM Map

4COM × 36SEG

Address	Bit	7	6	5	4	3	2	1	0	Digit
						COM3	COM2	COM1	COM0	
0840h	LRAM0					d	c	b	a	→ (1)
0841h	LRAM1					h	g	f	e	→ (1)
0842h	LRAM2					k	j		i	→ (1)
0843h	LRAM3					n	m		l	→ (1)
0844h	LRAM4					d	c	b	a	→ (2)
0845h	LRAM5					h	g	f	e	→ (2)
0846h	LRAM6					k	j		i	→ (2)
0847h	LRAM7					n	m		l	→ (2)
0848h	LRAM8					d	c	b	a	→ (3)
0849h	LRAM9					h	g	f	e	→ (3)
084Ah	LRAM10					k	j		i	→ (3)
084Bh	LRAM11					n	m		l	→ (3)
084Ch	LRAM12					d	c	b	a	→ (4)
084Dh	LRAM13					h	g	f	e	→ (4)
084Eh	LRAM14					k	j		i	→ (4)
084Fh	LRAM15					n	m		l	→ (4)
0850h	LRAM16					d	c	b	a	→ (5)
0851h	LRAM17					h	g	f	e	→ (5)
0852h	LRAM18					k	j		i	→ (5)
0853h	LRAM19					n	m		l	→ (5)
0854h	LRAM20									
0855h	LRAM21									
0856h	LRAM22									
0857h	LRAM23									
0858h	LRAM24									
0859h	LRAM25									
085Ah	LRAM26									
085Bh	LRAM27									
085Ch	LRAM28									
085Dh	LRAM29									
085Eh	LRAM30									
085Fh	LRAM31									
0860h	LRAM32									
0861h	LRAM33									
0862h	LRAM34									
0863h	LRAM35									

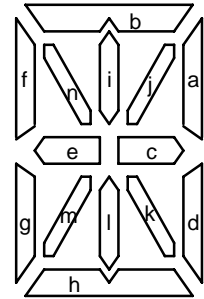


Figure 3.4 LCD Display RAM Setting Example

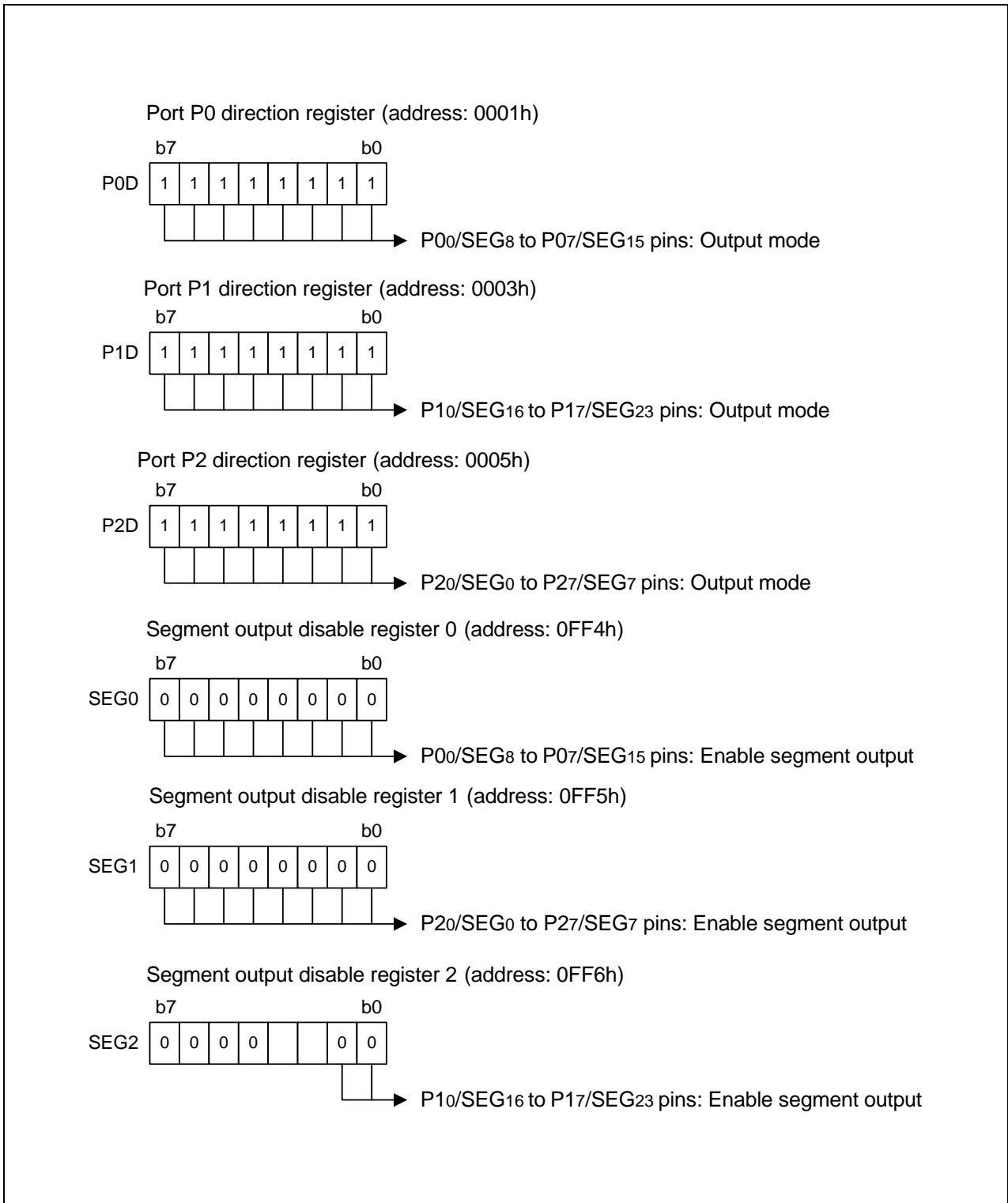


Figure 3.5 Relevant Register Settings (1)

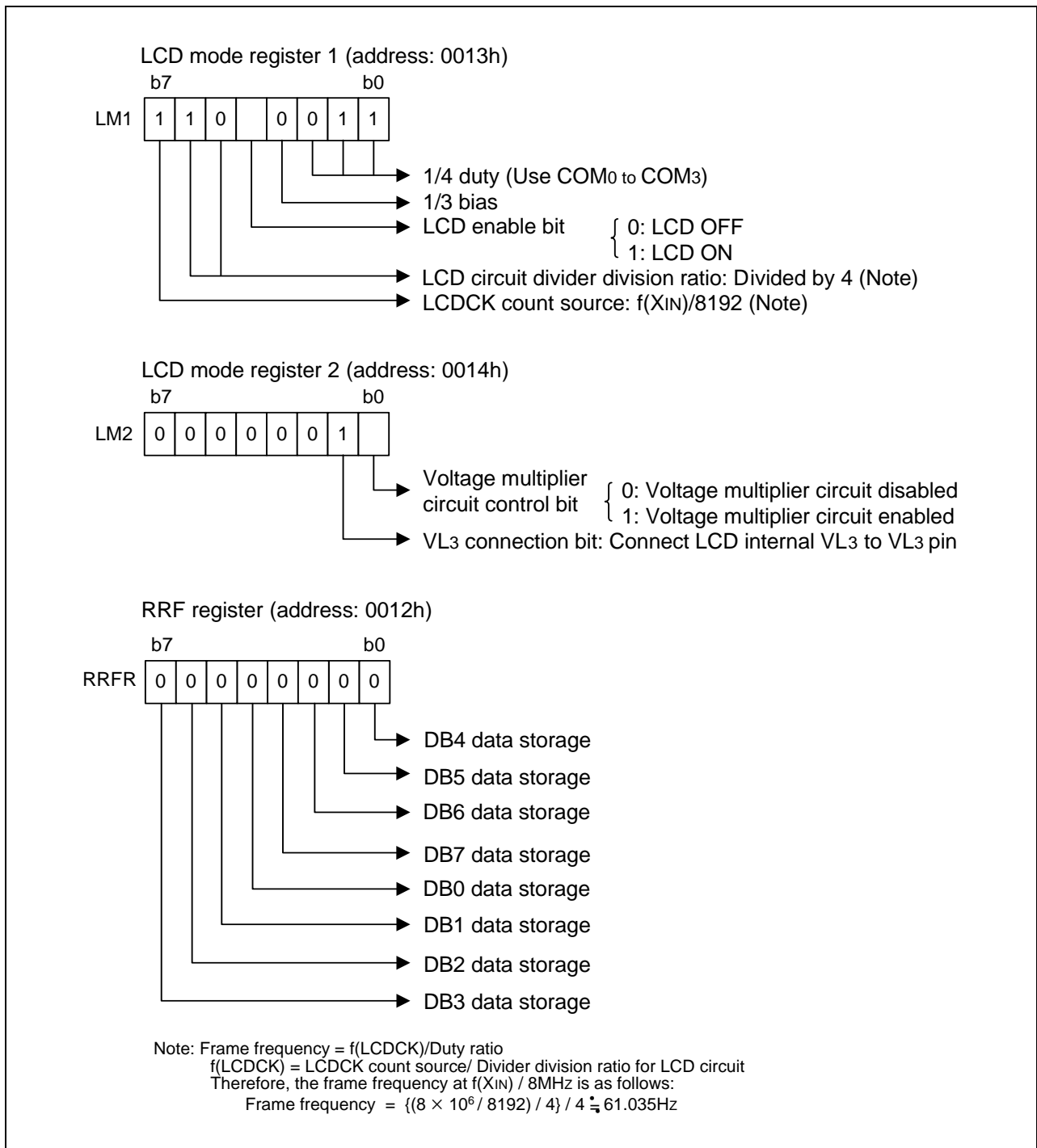


Figure 3.6 Relevant Register Settings (2)



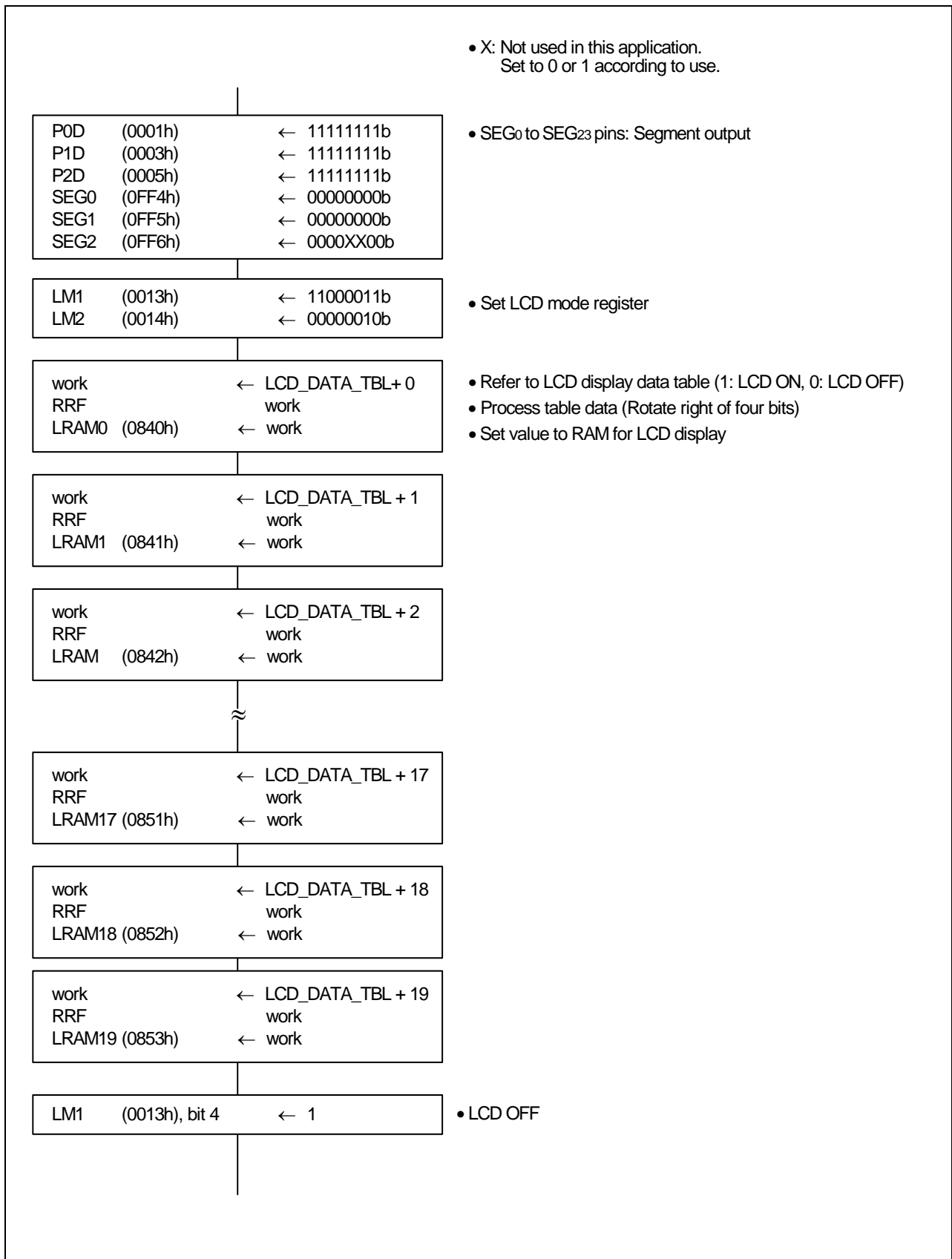


Figure 3.7 Control Procedure When Using RRF Instruction

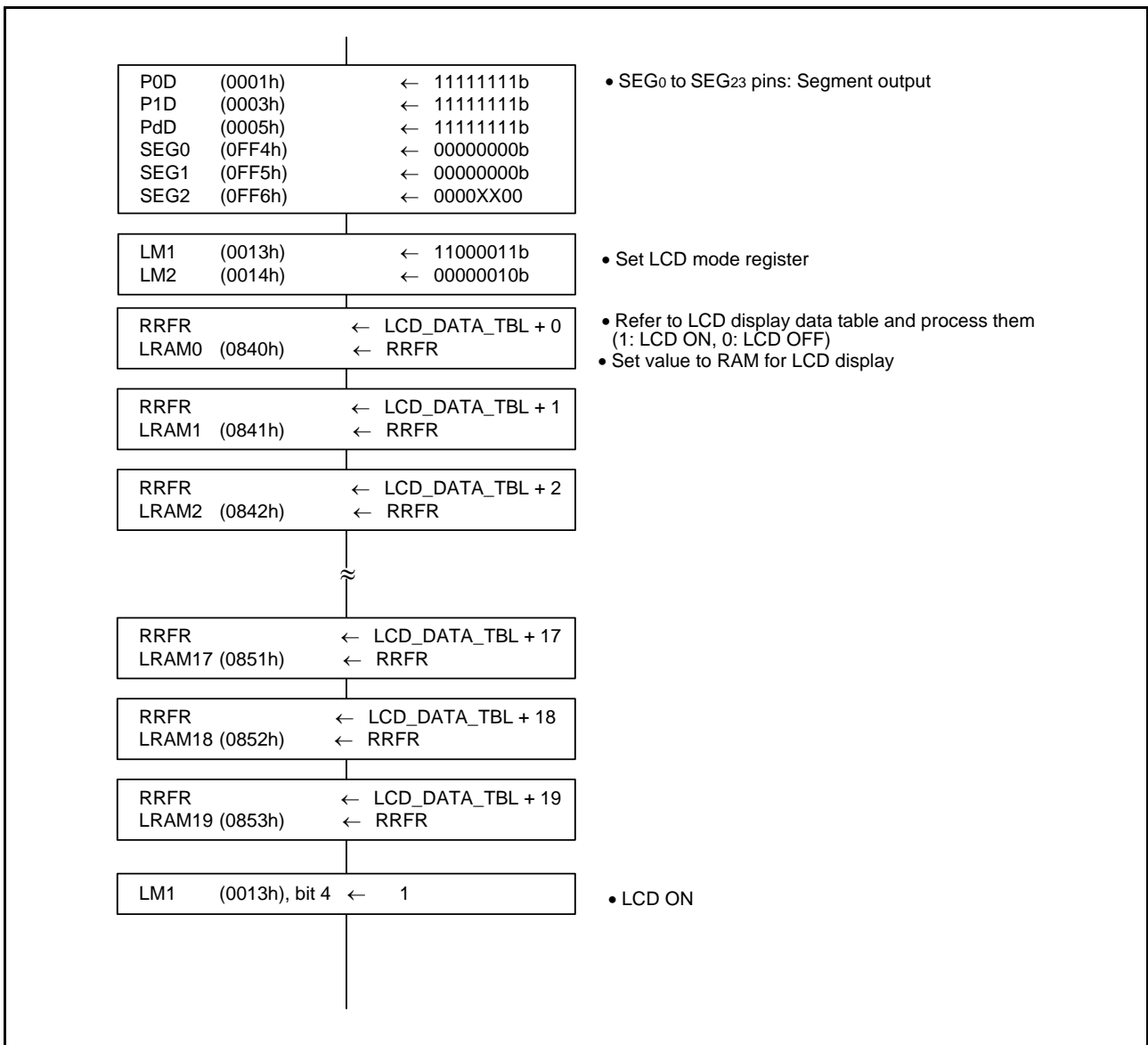


Figure 3.8 Control Procedure When Using RRF Register

#### **4. Sample Programming Code**

Download a sample program from the Renesas Technology website.  
To download, click “Application Notes” in the left side menu on the page of the 38D5 Group.

#### **5. Reference Document**

Datasheet  
38D5 Group Datasheet  
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REVISION HISTORY	38D5 Group RRF Register Application
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Rev.	Date	Description	
		Page	Summary
1.00	Sep 15, 2006	-	First Edition issued
2.00	Jan 21, 2008	6	VL3 connection bit revised

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