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38D5 Group
List of Registers

1. Abstract

The following article introduces and shows the SFR registers of the 38D5 Group.

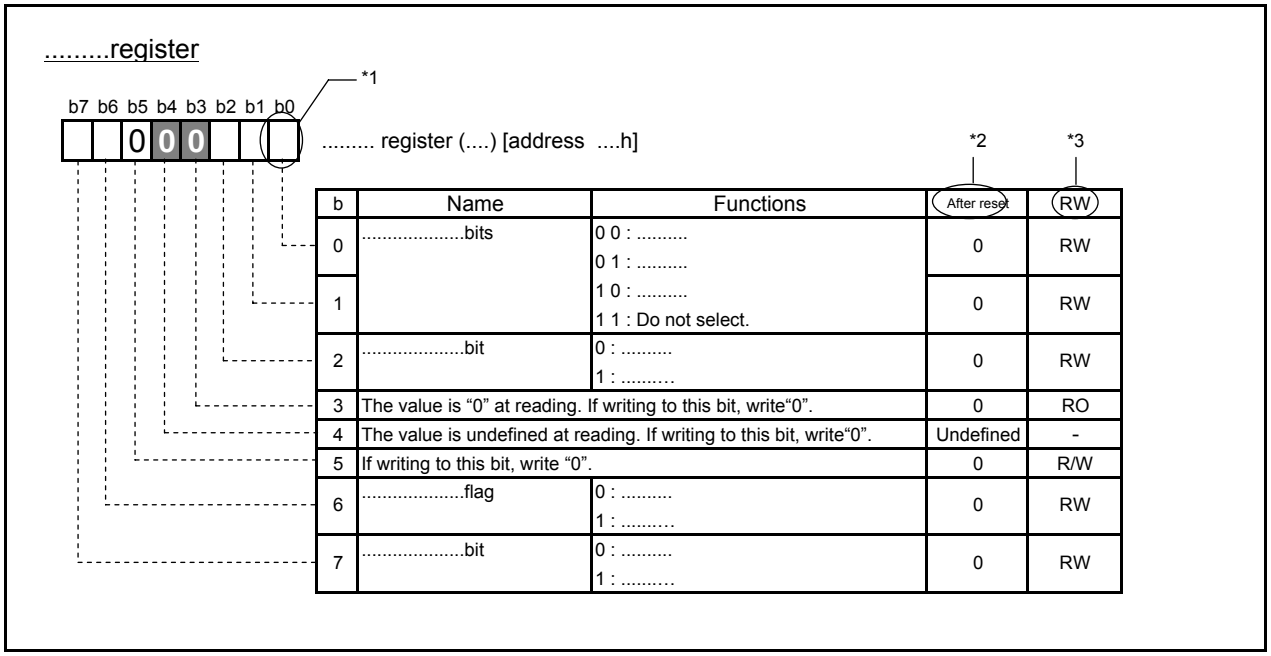
2. Introduction

The explanation of this issue is applied to the following MCU:

Applicable MCU: 38D5 Group

3. Structure of Register

The following is an example of the SFR register structure figure used in this application note and definitions of codes or abbreviations used in this figure are explained below.



b	Name	Functions	After reset	RW
0	.....bits	0 0 : ..... 0 1 : ..... 1 0 : ..... 1 1 : Do not select.	0	RW
1			0	RW
2	.....bit	0 : ..... 1 :	0	RW
3	The value is “0” at reading. If writing to this bit, write“0”.		0	RO
4	The value is undefined at reading. If writing to this bit, write“0”.		Undefined	-
5	If writing to this bit, write “0”.		0	R/W
6	.....flag	0 : ..... 1 :	0	RW
7	.....bit	0 : ..... 1 :	0	RW

*1

Blank	: Set “1” or “0” to this bit according to use.
0	: If writing to this bit, write "0".
1	: If writing to this bit, write "1".
×	: This bit is not used in the specific mode or state.
	: Nothing is arranged for this bit.

*2

0	: “0” after reset
1	: “1” after reset
Undefined	: Undefined after reset

*3

RW	: Read enabled. Write enabled.
RO	: Read enabled. This value depends on each bit at writing.
WO	: Write enabled. Undefined at reading.
-	: Undefined at reading. This value depends on each bit at writing.

4. List of Registers

Port Pi register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi register (Pi) (i = 0 to 6)

[addresses 0000h, 0002h, 0004h, 0006h, 0008h, 000Ah, 000Ch]

b	Name	Functions	After reset	RW
0	Port Pi_0	· In output mode Write: Port latch Read: Port latch or output of peripheral function (Note) · In input mode Write: Port latch Read: Value of pin	0	RW
1	Port Pi_1		0	RW
2	Port Pi_2		0	RW
3	Port Pi_3		0	RW
4	Port Pi_4		0	RW
5	Port Pi_5		0	RW
6	Port Pi_6		0	RW
7	Port Pi_7		0	RW

Note: The output value is read when shared output function is selected at the following ports.
$P5_0/RTP_0$, $P5_1/RTP_1$, $P6_3/T_{XOUT2}$, $P6_5/T_{XOUT1}$

Fig. 4.1 Structure of Port Pi register (i = 0 to 6)

Port P7 register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0

Port P7 register (P7) [address 000Eh]

b	Name	Functions	After reset	RW
0	Port $P7_0$	The value is the value of each pin at reading. If writing to these bits, write "0".	0	RO
1	Port $P7_1$		0	RO
2	Port $P7_2$	· In output mode Write: Port latch Read: Output of peripheral function (Note) · In input mode Write: Port latch Read: Value of pin	0	RW
3	Port $P7_3$		0	RW
4	Port $P7_4$		0	RW
5	The values are "0" at reading. If writing to these bits, write "0".		0	RO
6			0	RO
7			0	RO

Note: The output value is read when shared output function is selected.
$P7_2/T_{2OUT}$/CKOUT, $P7_3/PWM_0/T_{3OUT}$, $P7_4/PWM_1/T_{4OUT}$

Fig. 4.2 Structure of Port P7 register

Port Pi direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (PiD) (i = 0 to 6)

[addresses 0001h, 0003h, 0005h, 0007h, 0009h, 000Bh, 000Dh]

b	Name	Functions	After reset	RW
0	Port Pi_0 direction register	0: Input mode 1: Output mode	0	WO
1	Port Pi_1 direction register	0: Input mode 1: Output mode	0	WO
2	Port Pi_2 direction register	0: Input mode 1: Output mode	0	WO
3	Port Pi_3 direction register	0: Input mode 1: Output mode	0	WO
4	Port Pi_4 direction register	0: Input mode 1: Output mode	0	WO
5	Port Pi_5 direction register	0: Input mode 1: Output mode	0	WO
6	Port Pi_6 direction register	0: Input mode 1: Output mode	0	WO
7	Port Pi_7 direction register	0: Input mode 1: Output mode	0	WO

Notes: 1. In port(s) P0 to P3 set to input mode, pull-up resistor can be controlled by segment output disable registers 0 to 2 (addresses 0FF4h to 0FF6h) (refer to Fig.4.53, Fig.4.54).
In port(s) set to output mode, pull-up resistor is not connected.
In ports P4 to P6, pull-up resistor can be controlled by PULL registers 1 to 3 (addresses 0FF0h to 0FF2h).
In port(s) set to output mode, each corresponding pull-up control bit becomes invalid and pull-up resistor is not connected.
2. In output mode, output structure of port $P4_1$ pin can be selected at $P4_1$/TxD P-channel output disable bit (bit 4 at UART control register (address 001Bh).
3. In output mode, output structure of port $P4_5$ pin can be selected at $P4_5$/SOUT2 P-channel output disable bit (bit 4 at serial I/O2 control register (address 001Dh)).

Fig. 4.3 Structure of Port Pi direction register (i = 0 to 6)

Port P7 direction register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0 0 0 0 Port P7 direction register (P7D) [address 000Fh]

b	Name	Functions	After reset	RW
0	The values are "0" at reading. If writing to these bits, write "0".		0	RO
1			0	RO
2	Port P72 direction register (Note)	0: Input mode 1: Output mode	0	WO
3	Port P73 direction register (Note)	0: Input mode 1: Output mode	0	WO
4	Port P74 direction register (Note)	0: Input mode 1: Output mode	0	WO
5	The values are "0" at reading. If writing to these bits, write "0".		0	RO
6			0	RO
7			0	RO

Note: Pull-up resistor can be controlled by PULL register 3 (address 0FF2h).
In port(s) set to output mode, each corresponding pull-up control bit becomes invalid and pull-up resistor is not connected.

Fig. 4.4 Strucutre of Port P7 direction register

CPU mode register 2

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0 0 0 0 CPU mode register 2 (CPUM2) [address 0011h]

b	Name	Functions	After reset	RW
0	On-chip oscillator stop bit (Note 1)	0: Oscillating 1: Stop oscillating	(Note 2)	RW
1	If writing to this bit, write "0". Do not write "1".		0	RW
2	The values are "0" at reading. If writing to these bits, write "0".		0	RO
3			0	RO
4			0	RO
5			0	RO
6	If writing to these bits, write "0". Do not write "1".		0	RW
7			0	RW

Notes: 1. When the on-chip oscillator is selected by the watchdog timer count source selection bit 2 (bit 5 of watchdog timer control register (address 0029_{16})), the on-chip oscillator does not stop even when the on-chip oscillator stop bit is set to “1”. Also, when the low-speed mode is set, the on-chip oscillator stops regardless of the value of this bit in the QzROM version. The on-chip oscillator does not stop in the flash memory version, so set this bit to “1” to stop the oscillation. In on-chip oscillator mode, even if this bit is set to "1", the on-chip oscillator does not stop in the flash memory version, but stops in the QzROM version.
2. Flash memory version, the OSCSEL pins of the QzROM version = L: 1, the OSCSEL pin of the QzROM version = H: 0.

Fig. 4.5 Structure of CPU mode register 2

RRF register

b7 b6 b5 b4 b3 b2 b1 b0

RRF register (RRFR) [address 0012h]

b	Functions	After reset	RW
0	DB4 data storage	0	RW
1	DB5 data storage	0	RW
2	DB6 data storage	0	RW
3	DB7 data storage	0	RW
4	DB0 data storage	0	RW
5	DB1 data storage	0	RW
6	DB2 data storage	0	RW
7	DB3 data storage	0	RW

Fig. 4.6 Structure of RRF register

LCD mode register 1

b7 b6 b5 b4 b3 b2 b1 b0

LCD mode register 1 (LM1) [address 0013h]

b	Name	Functions	After reset	RW
0	Duty ratio selection bits	b2 b1 b0 0 0 0: 1 (Static) (Note 1) 0 0 1: 2 (Use COM0, COM1)	0	RW
1		0 1 0: 3 (Use COM0 to COM2) 0 1 1: 4 (Use COM0 to COM3) 1 0 0: Do not select.	0	RW
2		1 0 1: Do not select. 1 1 0: Do not select. 1 1 1: 8 (Use COM0 to COM7)	0	RW
3	Bias control bit (Note1)	0: 1/3 bias 1: 1/2 bias	0	RW
4	LCD enable bit	0: LCD OFF 1: LCD ON	0	RW
5	LCD circuit divider division ratio selection bits	b6 b5 0 0: Clock input	0	RW
6		0 1: 2 division of clock input 1 0: 4 division of clock input 1 1: 8 division of clock input	0	RW
7	LCDCK count source selection bit (Note 2)	0: f(XCIN)/32 1: ϕSOURCE/8192 ϕSOURCE: f(XIN) (Frequency/2, 4, or 8 mode) f(XCIN) (Low-speed mode) f(OCO)/4 (On-chip oscillator mode)	0	RW

Notes: 1. When selecting duty ratio of 1 at duty ratio selection bits, write "1" to bias control bit.
2. LCDCK is a clock for LCD timing controller.

Fig. 4.7 Structure of LCD mode register 1

LCD mode register 2

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

LCD mode register 2 (LM2) [address 0014h]

b	Name	Functions	After reset	RW
0	Voltage multiplier circuit control bit	0: Voltage multiplier circuit disabled Pins $P7_0/INT_{01}$, $P7_1/INT_{11}$ (Note) 1: Voltage multiplier circuit enabled Pins C_1, C_2	0	RW
1	V_{L3} connection bit	0: Connect LCD internal V_{L3} to V_{CC} 1: Connect LCD internal V_{L3} to V_{L3} pin	0	RW
2	The values are "0" at reading. If writing to these bits, write "0".		0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Note: When disabling voltage multiplier circuit, pins C_1 and C_2 function as input ports $P7_0/INT_{01}$ and $P7_1/INT_{11}$.

Fig. 4.8 Structure of LCD mode register 2

AD control register

b7 b6 b5 b4 b3 b2 b1 b0

AD control register (ADCON) [address 0015h]

b	Name	Functions	After reset	RW
0	Analog input pin selection bits	b2 b1 b0 0 0 0 : $P5_0/AN_0$ 0 0 1 : $P5_1/AN_1$ 0 1 0 : $P5_2/AN_2$ 0 1 1 : $P5_3/AN_3$ 1 0 0 : $P5_4/AN_4$ 1 0 1 : $P5_5/AN_5$ 1 1 0 : $P5_6/AN_6$ 1 1 1 : $P5_7/AN_7$	0	RW
1			0	RW
2			0	RW
3	AD conversion completion bit	0: Conversion in progress 1: Conversion completed	1	RW (Note1)
4	AD conversion clock selection bit	0: ϕSOURCE/2 1: ϕSOURCE/8 ϕSOURCE: f(X_{IN}) (Frequency/2, 4, or 8 mode) f(OCO)/4 (Low-speed mode, On-chip oscillator mode)	0	RW
5	ADKEY enable bit (Note 2)	0: Disabled 1: Enabled	0	RW
6	10-bit or 8-bit conversion switch bit	0: 10-bit AD 1: 8-bit AD	0	RW
7	ADKEY selection bit	0: Disabled 1: Enabled	0	RW

Notes: 1. This bit can be set to "0" but not to "1" by program.
2. When ADKEY enable bit is set to “1”, analog input pin selection bit becomes invalid.
Do not execute A/D conversion by protram while ADKEY is enabled.
Values in analog input pin selection bits are not changed by enabling ADKEY.

Fig. 4.9 Structure of AD control register

AD conversion register (low-order)

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0 0

AD conversion register (low-order) (ADL) [address 0016h]

b	Name	Functions	After reset	RW
0	VREF input switch bit	0: Automatic 1: ON	0 (Note 2)	WO
1	The values are "0" at reading. If writing to these bits, write "0".		0	RO
2			0	RO
3			0	RO
4			0	RO
5			0	RO
6	A/D conversion results in 10-bit AD mode can be read. The values at reading in 8-bit AD mode are undefined.	In 10-bit AD mode: b7 … b0 = b1 b0	Undefined	RO
7	If writing to these bits, write "0".		Undefined	RO

Notes: 1. Do not read this register while A/D conversion is executed.
2. The value is undefined at reading.

Fig. 4.10 Structure of AD conversion register (low-order)

AD conversion register (high-order)

b7 b6 b5 b4 b3 b2 b1 b0

AD conversion register (high-order) (ADH) [address 0017h]

b	Functions	After reset	RW
0	A/D conversion results can be read.	Undefined	RO
1	If writing to these bits,	Undefined	RO
2	write “00h”.	Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

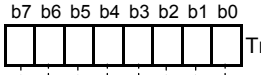
In 10-bit AD mode: b7 … b0 = b9 b8 b7 b6 b5 b4 b3 b2

In 8-bit AD mode: b7 … b0 = b7 b6 b5 b4 b3 b2 b1 b0

Note: Do not read this register while A/D conversion is executed.

Fig. 4.11 Structure of AD conversion register (high-order)

Transmit buffer register

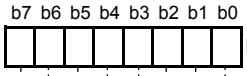


Transmit buffer register (TB) [address 0018h]

b	Functions	After reset	RW
0	Transmit data is written to this buffer register.	Undefined	WO
1	Write transmit data.	Undefined	WO
2		Undefined	WO
3		Undefined	WO
4		Undefined	WO
5		Undefined	WO
6		Undefined	WO
7		Undefined	WO

Note: This register is located at the same address as receive buffer register.
This register is write-only.

Receive buffer register



Receive buffer register (RB) [address 0018h]

b	Functions	After reset	RW
0	Receive data is read in this buffer register.	Undefined	RO
1	Read receive data.	Undefined	RO
2		Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

Note: This register is located at the same address as transmit buffer register.
This register is read-only.

Fig. 4.12 Structures of Transmit buffer register and Receive buffer register

Serial I/O1 status register

b7 b6 b5 b4 b3 b2 b1 b0

1 | | | | | | | |

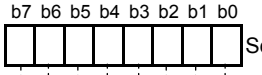
Serial I/O1 status register (SIO1STS) [address 0019h]

b	Name	Functions	After reset	RW
0	Transmit buffer empty flag (TBE) (Note1)	0 : Buffer register full 1 : Buffer register empty	0	RO
1	Receive buffer full flag (RBF) (Note 1, 2)	0 : Buffer register empty 1 : Buffer register full	0	RO
2	Transmit shift register shift completion flag (TSC)(Note1)	0 : Transmit shift in progress 1 : Transmit shift completed	0	RO
3	Overrun error flag (OE) (Note3)	0 : No overrun error 1 : Overrun error	0	RO
4	Parity error flag (PE) (Note3)	0 : No parity error 1 : Parity error	0	RO
5	Framing error flag (FE) (Note3)	0 : No framing error 1 : Framing error	0	RO
6	Summing error flag (SE) (Note3)	0 : (OE) U (PE) U (FE) = 0 1 : (OE) U (PE) U (FE) = 1	0	RO
7	The value is “1” at reading. If writing to this bit, write “1”.		1	RO

Note: 1. If writing to these bits, write "0".
2. This bit becomes "0" when receive buffer register is read.
3. These bits become "0" by writing to this register. If writing to these bits, write “0” .

Fig. 4.13 Structure of Serial I/O1 status register

Serial I/O1 control register



Serial I/O1 control register (SIO1CON) [address 001Ah]

b	Name	Functions	After reset	RW
0	BRG count source selection bit (CSS)	0: ϕSOURCE 1: ϕSOURCE/4 ϕSOURCE: f(XIN) (Frequency/2, 4, or 8 mode) f(XCIN) (Low-speed mode) f(OCO)/4 (On-chip oscillator mode)	0	RW
1	Serial I/O1 synchronous clock selection bit (SCS)	In clock synchronous serial I/O mode 0: BRG output divided by 4 1: External clock input In UART mode 0: BRG output divided by 16 1: External clock input divided by 16	0	RW
2	$\overline{SRDY1}$ output enable bit (SRDY)	0: Output disabled (Pin P43: I/O port) 1: Output enabled (Pin P43: $\overline{SRDY1}$ output pin)	0	RW
3	Transmit interrupt source selection bit (TIC)	0: When transmit buffer register becomes empty (TBE = 1) 1: When transmit shift operation is completed (TSC = 1)	0	RW
4	Transmit enable bit (TE)	0: Transmission disabled 1: Transmission enabled	0	RW
5	Receive enable bit (RE)	0: Reception disabled 1: Reception enabled	0	RW
6	Serial I/O1 mode selection bit (SIOM)	0: UART mode 1: Clock synchronous serial I/O mode	0	RW
7	Serial I/O1 enable bit (SIOE)	0: Serial I/O1 disabled (Pins P40 to P43: I/O port) 1: Serial I/O1 enabled (Pins P40 to P43: Serial I/O1 function pins)	0	RW

Fig. 4.14 Structure of Serial I/O1 control register

UART control register

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1					

UART control register (UARTCON) [address 001Bh]

b	Name	Functions	After reset	RW
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	RW
1	Parity enable bit (PARE)	0: Parity disabled 1: Parity enabled	0	RW
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	RW
3	Stop bit length selection bit (STPS)	0: 1 stop bit 1: 2 stop bits	0	RW
4	$P4_1$/TxD P-channel output disable bit (POFF)	In output mode 0: CMOS output 1: N-channel open drain output In input mode, this bit is invalid.	0	RW
5	The values are "1" at reading. If writing to these bits, write "1".		1	RO
6			1	RO
7			1	RO

Fig. 4.15 Structure of UART control register

Baud rate generator

b7	b6	b5	b4	b3	b2	b1	b0

Baud rate generator (BRG) [address 001Ch]

b	Functions	After reset	RW
0	Set the frequency divide value of BRG count source.	Undefined	RW
1	Baud rate generator divides the frequency of the count source by (n + 1)	Undefined	RW
2	when n is the value written to BRG.	Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Note: Write to this register only while transmit/receive operation is stopped.

Fig. 4.16 Structure of Baud rate generator

Serial I/O2 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O2 control register (SIO2CON) [address 001Dh]

b	Name	Functions	After reset	RW
0	Internal synchronous clock selection bits	b2 b1 b0 0 0 0: ϕSOURCE/8 0 0 1: ϕSOURCE/16 0 1 0: ϕSOURCE/32	0	RW
1		0 1 1: ϕSOURCE/64 1 0 0: Do not select. 1 0 1: Do not select. 1 1 0: ϕSOURCE/128	0	RW
2		1 1 1: ϕSOURCE/256 ϕSOURCE: f(XIN) (Frequency/2, 4, or 8 mode) f(XCIN) (Low-speed mode) f(OCO)/4 (On-chip oscillator mode)	0	RW
3	Serial I/O2 port selection bit	0: Pins P45, P46 = I/O port 1: Pins P45, P46 = SOUT2, SCLK2 signal output	0	RW
4	P45/SOUT2 P-channel output disable bit	In output mode 0: CMOS output 1: N-channel open drain output In input mode, this bit is invalid.	0	RW
5	Transfer direction selection bit	0: LSB first 1: MSB first	0	RW
6	Serial I/O2 synchronous clock selection bit	0: External clock 1: Internal clock	0	RW
7	$\overline{SRDY2}$ output selection bit	0: Pin P47 = I/O port 1: Pin P47 pin = $\overline{SRDY2}$ signal output	0	RW

Fig. 4.17 Structure of Serial I/O2 control register

Serial I/O2 register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O2 register (SIO2) [address 001Fh]

b	Functions	After reset	RW
0	This is a shift register for serial transmission and reception. · When transmitting: Write transmit data. Do not write while transmission is in progress. · When receiving: Read receive data. Do not read while reception is in progress.	Undefined	RW
1		Undefined	RW
2		Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Fig. 4.18 Structure of Serial I/O2 register

Timer 1 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 1 register (T1) [address 0020h]

b	Functions	After reset	RW
0	· Set the count initial value. This register count (n + 1) times when the set value is n. · Write value to both latch and timer simultaneously at writing. · The value is the count value of timer 1 at reading.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.19 Structure of Timer 1 register

Timer 2 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 2 register (T2) [address 0021h]

b	Functions	After reset	RW
0	· Set the count initial value. This register count (n + 1) times when the set value is n. · This register operates as follows at writing. When timer 2 write control bit = “0”: Write value to both latch and timer simultaneously. When timer 2 write control bit = “1”: Write value to latch only. · The value is the count value of timer 2 at reading.	1	RW
1		0	RW
2		0	RW
3		0	RW
4		0	RW
5		0	RW
6		0	RW
7		0	RW

Notes: 1. This register is used to generate waiting time at reset and exiting from stop mode.
2. When underflow and writing to timer latch occur almost at the same time while selecting writing to timer latch only, the value is set to timer and timer latch simultaneously. At this time, counting is stopped during writing to timer latch.

Fig. 4.20 Structure of Timer 2 register

Timer 3 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 3 register (T3) [address 0022h]

b	Functions	After reset	RW
0	· Set the count initial value. This register count (n + 1) times when the set value is n.	1	RW
1		1	RW
2	· This register operates as follows at writing. When timer 3 write control bit = “0”: Write value to both latch and timer simultaneously. When timer 3 write control bit = “1”: Write value to latch only.	1	RW
3		1	RW
4		1	RW
5	· The value is the count value of timer 3 at reading.	1	RW
6		1	RW
7		1	RW

Note: When underflow and writing to timer latch occur almost at the same time while selecting writing to timer latch only, the value is set to timer and timer latch simultaneously. At this time, counting is stopped during writing to timer latch.

Fig. 4.21 Structure of Timer 3 register

Timer 4 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 4 register (T4) [address 0023h]

b	Functions	After reset	RW
0	· Set the count initial value. This register count (n + 1) times when the set value is n.	1	RW
1		1	RW
2	· This register operates as follows at writing. When timer 4 write control bit = “0”: Write value to both latch and timer simultaneously. When timer 4 write control bit = “1”: Write value to latch only.	1	RW
3		1	RW
4		1	RW
5	· The value is the count value of timer 4 at reading.	1	RW
6		1	RW
7		1	RW

Note: When underflow and writing to timer latch occur almost at the same time while selecting writing to timer latch only, the value is set to timer and timer latch simultaneously. At this time, counting is stopped during writing to timer latch.

Fig. 4.22 Structure of Timer 4 register

PWM01 register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 0 | | | | | PWM01 register (PWM01) [address 0024h]

b	Name	Functions	After reset	RW
0	PWM0 set bits	b1 b0 0 0 : Not extended 0 1 : Extended once in four periods 1 0 : Extended twice in four periods 1 1 : Extended three times in four periods	0	RW
1			0	RW
2	PWM1 set bits	b3 b2 0 0 : Not extended 0 1 : Extended once in four periods 1 0 : Extended twice in four periods 1 1 : Extended three times in four periods	0	RW
3			0	RW
4	The values are "0" at reading. If writing to these bits, write "0".		0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.23 Structure of PWM01 register

Timer 12 mode register

b7 b6 b5 b4 b3 b2 b1 b0

| | | | | | | | | Timer 12 mode register (T12M) [address 0025h]

b	Name	Functions	After reset	RW
0	Timer 1 count stop bit	0 : Count 1 : Stop count	0	RW
1	Timer 2 count stop bit	0 : Count 1 : Stop count	0	RW
2	Timer 1 count source selection bits	b3 b2 0 0 : Frequency divider for timer 1 0 1 : f(XCIN) 1 0 : Underflow of timer Y 1 1 : Do not select.	0	RW
3			0	RW
4	Timer 2 count source selection bits	b5 b4 0 0 : Underflow of timer 1 0 1 : f(XCIN) 1 0 : Frequency divider for timer 2 1 1 : Do not select.	0	RW
5			0	RW
6	Timer 2 output selection bit	0 : Pin P72 = I/O port 1 : Pin P72 = Timer 2 output	0	RW
7	T2OUT output edge switch bit	0 : Start at “L” output 1 : Start at “H” output	0	RW

Fig. 4.24 Structure of Timer 12 mode register

Timer 34 mode register

b7 b6 b5 b4 b3 b2 b1 b0

0 Timer 34 mode register (T34M) [address 0026h]

b	Name	Functions	After reset	RW
0	Timer 3 count stop bit	0 : Count 1 : Stop count	0	RW
1	Timer 4 count stop bit	0 : Count 1 : Stop count	0	RW
2	Timer 3 count source selection bit	0 : Frequency divider for timer 3 1 : Underflow of timer 2	0	RW
3	Timer 4 count source selection bit	b4 b3 0 0 : Frequency divider for timer 4	0	RW
4		0 1 : Underflow of timer 3 1 0 : Underflow of timer 2 1 1 : f(XIN)	0	RW
5	Timer 3 operation mode selection bit	0 : Timer mode 1 : PWM mode	0	RW
6	Timer 4 operation mode selection bit	0 : Timer mode 1 : PWM mode	0	RW
7	The value is "0" at reading. If writing to this bit, write "0".		0	RO

Fig. 4.25 Structure of Timer 34 mode register

Timer 1234 mode register

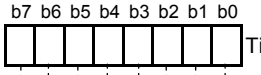
b7 b6 b5 b4 b3 b2 b1 b0

0 Timer 1234 mode register (T1234M) [address 0027h]

b	Name	Functions	After reset	RW
0	T3OUT output edge switch bit	0 : Start at "L" output 1 : Start at "H" output	0	RW
1	T4OUT output edge switch bit	0 : Start at "L" output 1 : Start at "H" output	0	RW
2	Timer 3 output selection bit	0 : Pin P73 = I/O port 1 : Pin P73 = Timer 3 output	0	RW
3	Timer 4 output selection bit	0 : Pin P74 = I/O port 1 : Pin P74 = Timer 4 output	0	RW
4	Timer 2 write control bit	0 : Write to latch and timer simultaneously 1 : Write to latch only	0	RW
5	Timer 3 write control bit	0 : Write to latch and timer simultaneously 1 : Write to latch only	0	RW
6	Timer 4 write control bit	0 : Write to latch and timer simultaneously 1 : Write to latch only	0	RW
7	The value is "0" at reading. If writing to this bit, write "0".		0	RO

Fig. 4.26 Structure of Timer 1234 mode register

Timer 1234 frequency division selection register



Timer 1234 frequency division selection register (PRE1234) [address 0028h]

b	Name	Functions	After reset	RW
0	Timer 1 frequency division selection bits	b1 b0 0 0: 1/16 × ϕSOURCE 0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE	0	RW
1			0	RW
2	Timer 2 frequency division selection bits	b3 b2 0 0: 1/16 × ϕSOURCE 0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE	0	RW
3			0	RW
4	Timer 3 frequency division selection bits	b5 b4 0 0: 1/16 × ϕSOURCE 0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE	0	RW
5			0	RW
6	Timer 4 frequency division selection bits	b7 b6 0 0: 1/16 × ϕSOURCE 0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE	0	RW
7			0	RW

Note: ϕSOURCE: f(XIN) Frequency/2, 4, or 8 mode
f(XCIN) Low-speed mode
f(OCO)/4 On-chip oscillator mode

Fig. 4.27 Structure of Timer 1234 frequency division selection register

Watchdog timer control register

b7 b6 b5 b4 b3 b2 b1 b0

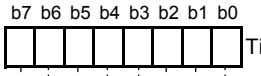
Watchdog timer control register (WDTCON) [address 0029h]

b	Name	Functions	After reset	RW
0	Watchdog timer H		1	RO
1			1	RO
2			1	RO
3			1	RO
4			1	RO
5	Watchdog timer count source selection bit 2 (Note1)	0 : ϕSOURCE 1 : f(OCO)/4 (Note2) ϕSOURCE: f(X_{IN}) (Frequency/2, 4, or 8 mode) f(X_{CIN}) (Low-speed mode) f(OCO)/4 (On-chip oscillator mode)	0	RW
6	STP instruction function selection bit (Note1, 2)	0 : Enter stop mode by execution of STP instruction 1 : Internal reset by execution of STP instruction	0	RW
7	Watchdog timer count source selection bit (Note1)	0 : ϕSOURCE/1024 1 : ϕSOURCE/4	0	RW

Notes: 1. These bits can be written only once after reset is released.
After being written once, these bits are locked and cannot be rewritten.
2. When selecting on-chip oscillator by setting "1" to watchdog timer count source selection bit 2, on-chip oscillator is forced to oscillate and can not be stopped.
At this time, set STP instruction function selection bit to "1".
3. Watchdog timer is set to “FFh” by writing to this register.

Fig. 4.28 Structure of Watchdog timer control register

Timer X register (low-order, high-order)



Timer X register (low-order, high-order) (TXL, TXH) [addresses 002Ah, 002Bh]

b	Functions	After reset	RW
0	· Set the count initial value. This register count (n + 1) times when the set value is n.	1	RW
1	When timer X register (expansion) is set, timer X operates as 18-bit counter. · These registers operate as follows at writing.	1	RW
2	When timer X write control bit = “0”: Write value to latch and timer simultaneously. When timer X write control bit = “1”: Write value to latch only.	1	RW
3	This operation is not affected by timer X count stop bit. · Write order in timer mode, pulse output mode, event counter mode,	1	RW
4	and pulse width measurement mode: Expansion, low-order, and high-order · Write order in IGBT output mode, PWM mode:	1	RW
5	Compare registers 1, 2, and 3, expansion, low-order, and high-order (Write order of compare registers (high-order, low-order) is not determined).	1	RW
6	· The value at reading is the count value of timer X at reading. · Read order: Expansion, high-order, low-order	1	RW
7	(Read order of compare registers is not determined).	1	RW

Note: When underflow and writing to high-order timer latch occur almost at the same time while selecting writing to timer latch only, the value is set to timer and timer latch simultaneously. At this time, counting is stopped during writing to the high-order timer latch.

Fig. 4.29 Structure of Timer X register (low-order, high-order)

Timer X register (expansion)

b7 b6 b5 b4 b3 b2 b1 b0

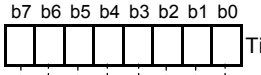
0 0 0 0 0 0 □ □ Timer X register (expansion) (TXEX) [address 002Ch]

b	Functions	After reset	RW
0	· Set the count initial value. These registers count (n+1) times when the set value is n. · This register operates as follows at writing. When timer X write control bit = "0": Write value to expansion latch and expansion counter simultaneously. When timer X write control bit = "1": Write value to expansion latch only. This operation is not affected by timer X count stop bit. · Write order in timer mode, pulse output mode, event counter mode and pulse width measurement mode: Expansion, low-order, and high-order Write order in IGBT output mode and PWM mode: Compare registers 1, 2 and 3, expansion, low-order, and high-order (Write order of compare registers (low-order, high-order) is not determined). · The value is the count value of timer X at reading. · Read order: Expansion, high-order and low-order (Read order of compare registers is not determined).	0	RW
1		0	RW
2	The values are "0" at reading. If writing to these bits, write "0".	0	RO
3		0	RO
4		0	RO
5		0	RO
6		0	RO
7		0	RO

Notes. 1. Timer X operates as 18-bit counter when values are set to this register after reset.
2. Do not write "1" to this register in IGBT output mode and PWM mode.
When "1" has already written to this register, make sure to write "0" to this register before use.

Fig. 4.30 Structure of Timer X register (expansion)

Timer X mode register

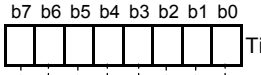


Timer X mode register (TXM) [address 002Dh]

b	Name	Functions	After reset	RW
0	Timer X operating mode bits	b2 b1 b0 0 0 0: Timer mode	0	RW
1		0 0 1: Pulse output mode 0 1 0: IGBT output mode	0	RW
2		0 1 1: PWM mode 1 0 0: Event counter mode 1 0 1: Pulse width measurement mode 1 1 0: Do not select. 1 1 1: Do not select.	0	RW
3	Timer X write control bit	0: Write to latch and timer simultaneously 1: Write to latch only	0	RW
4	Timer X count source selection bit	0: Frequency divider output 1: f(X_{CIN})	0	RW
5	Data for control of event counter window	0: Event counter enabled 1: Event counter disabled	0	RW
6	Timer X count stop bit	0: Count 1: Stop count	0	RW
7	Timer X output 1 selection bit	0: Pin $P6_5$ = I/O port 1: Pin $P6_5$ = Timer X output 1	0	RW

Fig. 4.31 Structure of Timer X mode register

Timer X control register 1



Timer X control register 1 (TXCON1) [address 002Eh]

b	Name	Functions	After reset	RW
0	Noise filter sampling clock selection bit	0 : f(XIN)/2 1 : f(XIN)/4	0	RW
1	External trigger delay time selection bits	b2 b1 0 0: Not delayed	0	RW
2		0 1: (4/f(XIN))μs 1 0: (8/f(XIN))μs 1 1: (16/f(XIN))μs	0	RW
3	Timer X output control bit 1	0: INT1 (P66/INT10 or P71/INT11) interrupt signal not used 1: INT1 (P66/INT10 or P71/INT11) interrupt signal used	0	RW
4	Timer X output control bit 2	0: P64/INT2 interrupt signal not used 1: P64/INT2 interrupt signal used	0	RW
5	Timer X output 1 edge switch bit	0: Start at "L" output 1: Start at "H" output	0	RW
6	CNTR0 active edge switch bits	Depends on timer X operation mode	0	RW
7		(Refer to table 4.1 below)	0	RW

Fig. 4.32 Structure of Timer X control register1

Table 4.1 Function of CNTR0 active edge switch bits

Timer X operation mode	Set value b7 b6	Timer function/CNTR0 pin function	CNTR0 Interrupt request occurrence source
Timer mode	0 0	External interrupt pin	CNTR0 input signal falling edge (No influence on timer count)
	0 1		CNTR0 input signal rising edge (No influence on timer count)
	1 0		Input signal falling edge and rising edge (No influence on timer count)
	1 1		
Pulse output mode	0 0		Input signal falling edge (No influence on timer count)
	0 1		Input signal rising edge (No influence on timer count)
	1 0		Input signal falling edge and rising edge (No influence on timer count)
	1 1		
IGBT output mode	0 0		Input signal falling edge (No influence on timer count)
	0 1		Input signal rising edge (No influence on timer count)
	1 0		Input signal falling edge and rising edge (No influence on timer count)
	1 1		
PWM mode	0 0		Input signal falling edge (No influence on timer count)
	0 1		Input signal rising edge (No influence on timer count)
	1 0		Input signal falling edge and rising edge (No influence on timer count)
	1 1		
Event counter mode	0 0	Count at rising edge	Input signal falling edge
	0 1	Count at falling edge	Input signal rising edge
	1 0	Count at both edges	Input signal falling edge and rising edge
	1 1	Count at both edges	Input signal falling edge and rising edge
Pulse width measurement mode	0 0	Measure "H" width	Input signal falling edge
	0 1	Measure "L" width	Input signal rising edge
	1 0	Do not select.	
	1 1		

Note: Set bit 7 to "0" in pulse width measurement mode.

Timer X control register 2

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 Timer X control register 2 (TXCON2) [address 002Fh]

b	Name	Functions	After reset	RW
0	Timer X output 2 selection bit	0: Pin P6$_3$ = I/O port 1: Pin P6$_3$ = Timer X output 2	0	RW
1	Timer X output 2 edge switch bit	0: Start at "L" output 1: Start at "H" output	0	RW
2	Timer X dividing frequency selection bits	b3 b2 0 0: 1/16 × ϕSOURCE	0	RW
3		0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE ϕSOURCE : f(X$_{IN}$) (Frequency/2, 4 or 8 mode) f(X$_{CIN}$) (Low-speed mode) f(OCO)/4 (On-chip oscillator mode)	0	RW
4	Trigger for IGBT input control bit	0: Noise filter sampling clock × 1 External trigger delay time ×1 1: Noise filter sampling clock × 2 External trigger delay time ×2	0	RW
5	The values are "0" at reading. If writing to these bits, write "0".		0	RO
6			0	RO
7			0	RO

Fig. 4.33 Structure of Timer X control register 2

Compare register 1, 2, 3 (low-order, high-order)

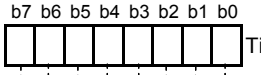
b7 b6 b5 b4 b3 b2 b1 b0
Compare register 1 (low-order, high-order) (COMP1L, COMP1H) [addresses 0030h, 0031h]
Compare register 2 (low-order, high-order) (COMP2L, COMP2H) [addresses 0032h, 0033h]
Compare register 3 (low-order, high-order) (COMP3L, COMP3H) [addresses 0034h, 0035h]

b	Functions	After reset	RW
0	· Set values of compare registers.	0	RW
1	· Write order in IGBT output mode and PWM mode:	0	RW
2	Compare registers 1, 2, and 3, expansion, low-order, and high-order	0	RW
3	(Write order of compare registers (high-order, low-order) is not determined).	0	RW
4	· Read order: Expansion, high-order, and low-order	0	RW
5	(Read order of compare registers is not determined).	0	RW
6		0	RW
7		0	RW

Note: Set the smaller value than the timer X register setting value. Do not set 00h.

Fig. 4.34 Structure of Compare register 1, 2, 3 (low-order, high-order)

Timer Y register (low-order, high-order)



Timer Y register (low-order, high-order) (TYL, TYH) [addresses 0036h, 0037h]

b	Functions	After reset	RW
0	· Set the count initial value. These registers count (n+1) times when the set value is n. · These registers operate as follows at writing. When timer Y write control bit = "0": Write value to latch and timer simultaneously. When timer Y write control bit = "1": Write value to latch only. Write from high-order to low-order. This operation is not affected by timer Y count stop bit. · The value is the count value of timer Y at reading. Read from high-order to low-order.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Note: When underflow and writing to high-order timer latch occur almost at the same time while selecting writing to timer latch only, the value is set to timer and timer latch simultaneously. At this time, counting is stopped during writing to the high-order timer latch.

Fig. 4.35 Structure of Timer Y register (low-order, high-order)

Timer Y mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer Y mode register (TYM) [address 0038h]

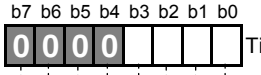
b	Name	Functions	After reset	RW
0	Real time port 1 control bit	0: Real time port function of pin $P5_0$/RTP_0 invalid 1: Real time port function of pin $P5_0$/RTP_0 valid	0	RW
1	Real time port 2 control bit	0: Real time port function of pin $P5_1$/RTP_1 invalid 1: Real time port function of pin $P5_1$/RTP_1 valid	0	RW
2	RTP_0 data for real time port	0: "L" output from pin $P5_0$/RTP_0 1: "H" output from pin $P5_0$/RTP_0	0	RW
3	RTP_1 data for real time port	0: "L" output from pin $P5_1$/RTP_1 1: "H" output from pin $P5_1$/RTP_1	0	RW
4	Timer Y operation mode bits	b5 b4 0 0: Timer mode 0 1: Period measurement mode 1 0: Event counter mode 1 1: Pulse width HL continuous measurement mode	0	RW
5			0	RW
6	$CNTR_1$ active edge switch bit	Depends on timer Y operation mode (Refer to table 4.2 below)	0	RW
7	Timer Y count stop bit	0: Count 1: Stop count	0	RW

Fig. 4.36 Structure of Timer Y mode register

Table 4.2 Function of $CNTR_1$ active edge switch bit

Timer Y operation mode	Set value	Timer function/$CNTR_1$ pin function	$CNTR_1$ Interrupt request occurrence source
Timer mode	"0"	External interrupt pin	$CNTR_1$ input signal falling edge (No influence on timer count)
	"1"		$CNTR_1$ input signal rising edge (No influence on timer count)
Period measurement mode	"0"	Measure the period from falling edge to falling edge	Input signal falling edge
	"1"	Measure the period from rising edge to rising edge	Input signal rising edge
Event counter mode	"0"	Count at rising edge	Input signal falling edge
	"1"	Count at falling edge	Input signal rising edge
Pulse width HL continuous measurement mode	"0"	Measure "H" and "L" pulse widths	Input signal falling and rising edges
	"1"		

Timer Y control register



Timer Y control register (TYCON) [address 0039h]

b	Name	Functions	After reset	RW
0	Timer Y write control bit	0: Write value to both latch and timer simultaneously 1: Write value to latch only	0	RW
1	Timer Y count source selection bit	0: Frequency divider output 1: f(XCIN)	0	RW
2	Timer Y frequency division selection bits	b3 b2 0 0: 1/16 × ϕSOURCE	0	RW
3		0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE ϕSOURCE: f(XIN) (Frequency/2, 4, or 8 mode) f(XCIN) (Low-speed mode) f(OCO)/4 (On-chip oscillator mode)	0	RW
4	The values are "0" at reading. If writing to these bits, write "0".		0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.37 Structure of Timer Y control register

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 Interrupt edge selection register (INTEDGE) [address 003Ah]

b	Name	Functions	After reset	RW
0	INT_0 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
1	INT_1 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
2	INT_2 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
3	Timer Y/$CNTR_1$ interrupt switch bit	0: Timer Y interrupt 1: $CNTR_1$ interrupt	0	RW
4	INT_0 input port switch bit	0: Input from port $P6_2$ (INT_{00}) 1: Input from port $P7_0$ (INT_{01})	0	RW
5	INT_1 input port switch bit	0: Input from port $P6_6$ (INT_{10}) 1: Input from port $P7_1$ (INT_{11})	0	RW
6	If writing to this bit, write “0”. Do not write “1”.		0	RW
7	The value is “0” at reading. If writing to this bit, write “0”.		0	RO

Fig.4.38 Structure of interrupt edge selection register

CPU mode register

b7 b6 b5 b4 b3 b2 b1 b0

CPU mode register (CPUM) [address 003Bh]

b	Name	Functions	After reset	RW
0	Processor mode bit	b1 b0 0 0: Single-chip mode	0	RW
1		0 1: Do not select. 1 0: Do not select. 1 1: Do not select.	0	RW
2	Stack page selection bit	0: 0 page 1: 1 page	0	RW
3	Internal system clock selection bit	0: Select main clock (including OCO, X_{IN}) 1: Select X_{CIN} - X_{COUT}	0	RW
4	Port X_C switch bit (Note 4)	0: I/O port function (stop oscillating) 1: X_{CIN} - X_{COUT} oscillation function	0	RW
5	X_{IN} - X_{OUT} oscillation stop bit (Note 5)	0: Oscillating 1: Stop oscillating	(Note 1)	RW
6	Main clock division ratio selection bit	0 0: f (X_{IN})/2 (frequency/2 mode) (Note 3) 0 1: f (X_{IN})/8 (frequency/8 mode)	1	RW
7	(Note 2)	1 0: f (X_{IN})/4 (frequency/4 mode) 1 1: On-chip oscillator	(Note1)	RW

Notes: 1. Flash memory version, the OSCSEL pins of the QzROM version = L: 1, the OSCSEL pin of the QzROM version = H: 0.
2. Valid only when internal system clock selection bit (bit 3) is set to "0".
3. 12.5MHz < f(X_{IN}) ≤16MHz is not available in frequency/2 mode.
4. In low-speed mode, the X_{CIN} - X_{COUT} oscillation stops if the port X_C switch bit is set to “0”.
5. In X_{IN} mode, the X_{IN} - X_{OUT} oscillation does not stop even if the X_{IN} - X_{OUT} oscillation stop bit is set to “1”.

Fig. 4.39 Structure of CPU mode register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [address 003Ch]

b	Name	Functions	After reset	RW
0	INT_0 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
1	INT_1 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
2	INT_2 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
3	Key input interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
4	Timer X interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
5	Timer 1 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
6	Timer 2 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
7	Timer 3 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)

Note: Each bit can be set to "0" but not to "1" by program.

Fig.4.40 Structure of Interrupt request register 1

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

Interrupt request register 2 (IREQ2) [address 003Dh]

b	Name	Functions	After reset	RW
0	Timer 4 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
1	Serial I/O1 receive interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
2	Serial I/O1 transmit interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
3	Serial I/O2 transmit/receive interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
4	$CNTR_0$ interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
5	Timer Y/$CNTR_1$ interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
6	AD conversion interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
7	The value is "0" at reading. If writing to this bit, write "0".		0	RO

Note: Each bit can be set to "0" but not to "1" by program.

Fig.4.41 Structure of Interrupt request register 2

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [address 003Eh]

b	Name	Functions	After reset	RW
0	INT_0 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
1	INT_1 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
2	INT_2 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
3	Key input interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
4	Timer X interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
5	Timer 1 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
6	Timer 2 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
7	Timer 3 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW

Fig.4.42 Structure of Interrupt control register 1

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

Interrupt control register 2 (ICON2) [address 003Fh]

b	Name	Functions	After reset	RW
0	Timer 4 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
1	Serial I/O1 receive interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
2	Serial I/O1 transmit interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
3	Serial I/O2 transmit/receive interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
4	$CNTR_0$ interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
5	Timer Y/$CNTR_1$ interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
6	AD conversion interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
7	If writing to this bit, write “0”. Do not write “1” to this bit.		0	RW

Fig.4.43 Structure of Interrupt control register 2

LCD display RAM (at 4COM × 36SEG)

address		bit 7	6	5	4	3	2	1	0	After reset	RW
						COM_3	COM_2	COM_1	COM_0		
0840h	LRAM0	Not used. (This area can be used as normal RAM)				SEG_0				Undefined	RW
0841h	LRAM1					SEG_1				Undefined	RW
0842h	LRAM2					SEG_2				Undefined	RW
0843h	LRAM3					SEG_3				Undefined	RW
0844h	LRAM4					SEG_4				Undefined	RW
0845h	LRAM5					SEG_5				Undefined	RW
0846h	LRAM6					SEG_6				Undefined	RW
0847h	LRAM7					SEG_7				Undefined	RW
0848h	LRAM8					SEG_8				Undefined	RW
0849h	LRAM9					SEG_9				Undefined	RW
084Ah	LRAM10					SEG_{10}				Undefined	RW
084Bh	LRAM11					SEG_{11}				Undefined	RW
084Ch	LRAM12					SEG_{12}				Undefined	RW
084Dh	LRAM13					SEG_{13}				Undefined	RW
084Eh	LRAM14					SEG_{14}				Undefined	RW
084Fh	LRAM15					SEG_{15}				Undefined	RW
0850h	LRAM16					SEG_{16}				Undefined	RW
0851h	LRAM17					SEG_{17}				Undefined	RW
0852h	LRAM18					SEG_{18}				Undefined	RW
0853h	LRAM19					SEG_{19}				Undefined	RW
0854h	LRAM20					SEG_{20}				Undefined	RW
0855h	LRAM21					SEG_{21}				Undefined	RW
0856h	LRAM22					SEG_{22}				Undefined	RW
0857h	LRAM23					SEG_{23}				Undefined	RW
0858h	LRAM24					SEG_{24}				Undefined	RW
0859h	LRAM25					SEG_{25}				Undefined	RW
085Ah	LRAM26					SEG_{26}				Undefined	RW
085Bh	LRAM27					SEG_{27}				Undefined	RW
085Ch	LRAM28					SEG_{28}				Undefined	RW
085Dh	LRAM29					SEG_{29}				Undefined	RW
085Eh	LRAM30					SEG_{30}				Undefined	RW
085Fh	LRAM31					SEG_{31}				Undefined	RW
0860h	LRAM32					SEG_{32}				Undefined	RW
0861h	LRAM33					SEG_{33}				Undefined	RW
0862h	LRAM34					SEG_{34}				Undefined	RW
0863h	LRAM35					SEG_{35}				Undefined	RW

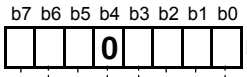
Fig.4.44 Structure of LCD display RAM (at 4COM × 36SEG)

LCD display RAM (at 8COM × 32SEG)

address	bit	7	6	5	4	3	2	1	0	After reset	RW
		COM_7	COM_6	COM_5	COM_4	COM_3	COM_2	COM_1	COM_0		
0840h	LRAM0	SEG_0								Undefined	RW
0841h	LRAM1	SEG_1								Undefined	RW
0842h	LRAM2	SEG_2								Undefined	RW
0843h	LRAM3	SEG_3								Undefined	RW
0844h	LRAM4	SEG_4								Undefined	RW
0845h	LRAM5	SEG_5								Undefined	RW
0846h	LRAM6	SEG_6								Undefined	RW
0847h	LRAM7	SEG_7								Undefined	RW
0848h	LRAM8	SEG_8								Undefined	RW
0849h	LRAM9	SEG_9								Undefined	RW
084Ah	LRAM10	SEG_{10}								Undefined	RW
084Bh	LRAM11	SEG_{11}								Undefined	RW
084Ch	LRAM12	SEG_{12}								Undefined	RW
084Dh	LRAM13	SEG_{13}								Undefined	RW
084Eh	LRAM14	SEG_{14}								Undefined	RW
084Fh	LRAM15	SEG_{15}								Undefined	RW
0850h	LRAM16	SEG_{16}								Undefined	RW
0851h	LRAM17	SEG_{17}								Undefined	RW
0852h	LRAM18	SEG_{18}								Undefined	RW
0853h	LRAM19	SEG_{19}								Undefined	RW
0854h	LRAM20	SEG_{20}								Undefined	RW
0855h	LRAM21	SEG_{21}								Undefined	RW
0856h	LRAM22	SEG_{22}								Undefined	RW
0857h	LRAM23	SEG_{23}								Undefined	RW
0858h	LRAM24	SEG_{24}								Undefined	RW
0859h	LRAM25	SEG_{25}								Undefined	RW
085Ah	LRAM26	SEG_{26}								Undefined	RW
085Bh	LRAM27	SEG_{27}								Undefined	RW
085Ch	LRAM28	SEG_{28}								Undefined	RW
085Dh	LRAM29	SEG_{29}								Undefined	RW
085Eh	LRAM30	SEG_{30}								Undefined	RW
085Fh	LRAM31	SEG_{31}								Undefined	RW
0860h	LRAM32	Not used. (This area can be used as normal RAM).								Undefined	RW
0861h	LRAM33									Undefined	RW
0862h	LRAM34									Undefined	RW
0863h	LRAM35									Undefined	RW

Fig.4.45 Structure of LCD display RAM (at 8COM × 32SEG)

Flash memory control register 0



Flash memory control register 0 (FMCR0) [address 0FE0h]

b	Name	Functions	After reset	RW
0	RY/$\overline{BY}$ status flag	0: Busy (During automatic writing/erasing) 1: Ready	1	RO
1	CPU rewrite mode select bit (Note 1)	0: CPU rewrite mode invalid 1: CPU rewrite mode valid	0	RW
2	User block 1 E/W enable bit (Notes 1, 2)	0: E/W disabled (1800h - 7FFFh) 1: E/W enabled (1800h - 7FFFh)	0	RW
3	Flash memory reset bit (Notes 3, 4)	0: Flash memory in operation 1: Flash memory reset	0	RW
4	If writing to this bit, write “0”. Do not write “1”.		0	RW
5	User ROM area select bit (Note 5)	0: Access to boot ROM area 1: Access to user ROM area	0	RW
6	Program status flag	0: Ends normally 1: Ends in error	0	RO
7	Erase status flag	0: Ends normally 1: Ends in error	0	RO

Notes. 1. In order to set this bit to "1", write this bit to "1" continuously after writing "0" .
In order to set this bit to "0", write this bit to "0" .
2. This bit can be written only when the CPU rewrite mode select bit is set to "1".
3. The flash memory can be reset only when the CPU rewrite mode select bit (bit 1) is set to "1".
Fix this bit to "0" when the CPU rewrite mode select bit is set to "0".
4. When this bit is set to "1" (reset the flash memory control circuit), access to the flash memory is impossible for 10 μs.
5. Write to this bit by a program on the RAM.
6. This register is only in the flash memory version.

Fig.4.46 Structure of Flash memory control register 0

Flash memory control register 1

b7	b6	b5	b4	b3	b2	b1	b0
0		0	0	0	0		

Flash memory control register 1 (FMCR1) [address 0FE1h]

b	Name	Functions	After reset	RW
0	Erase suspend enable bit (Note 1)	0: Suspend invalid 1: Suspend valid	0	RW
1	Erase suspend request bit (Note 1)	0: Erase restart (No request) 1: Erase suspend (Request issued)	0	RW
2	If writing to this bit, write “0”. Do not write “1”.		0	RO
3			0	RO
4			0	RO
5			0	RO
6	Erase suspend flag	0: Erase active 1: Erase inactive (Erase suspend mode)	1	RO
7	If writing to this bit, write “0”. Do not write “1”.		0	RW

Notes: 1. In order to set this bit to "1", write this bit to "1" continuously after writing "0" .
In order to set this bit to "0", write this bit to "0" .
2. Valid only when the erase suspend enable bit (bit 0) is set to "1".
3. This register is only in the flash memory version.

Fig.4.47 Structure of Flash memory control register 1

Flash memory control register 2

b7	b6	b5	b4	b3	b2	b1	b0
0	1	0		0	1	0	1

Flash memory control register 2 (FMCR2) [address 0FE2h]

b	Name	Functions	After reset	RW
0	If writing to this bit, write “1”. Do not write “0”.		1	RO
1	If writing to this bit, write “0”. Do not write “1”.		0	RO
2	If writing to this bit, write “1”. Do not write “0”.		1	RO
3	If writing to this bit, write “0”. Do not write “1”.		0	RO
4	User block 0 E/W enable bit (Notes 1, 2)	0: E/W disabled (8000h - FFFFh) 1: E/W enabled (8000h - FFFFh)	0	RW
5	If writing to this bit, write “0”. Do not write “1”.		0	RO
6	If writing to this bit, write “1”. Do not write “0”.		1	RO
7	If writing to this bit, write “0”. Do not write “1”.		0	RO

Notes: 1. In order to set this bit to "1", write this bit to "1" continuously after writing "0" .
In order to set this bit to "0", write this bit to "0" .
2. This bit can be written only when the CPU rewrite mode select bit (bit 1 in the flash memory control register 0 (address 0FE0h)) is set to "1"
3. This register is only in the flash memory version.

Fig.4.48 Structure of Flash memory control register 2

PULL register 1

b7 b6 b5 b4 b3 b2 b1 b0

PULL register 1 (PULL1) [address 0FF0h]

b	Name	Functions	After reset	RW
0	$P5_0$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
1	$P5_1$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
2	$P5_2$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
3	$P5_3$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
4	$P5_4$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
5	$P5_5$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
6	$P5_6$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
7	$P5_7$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW

Note: In port(s) set to output mode, each corresponding bit becomes invalid and pull-up register is not connected.

Fig.4.49 Structure of PULL register 1

PULL register 2

b7 b6 b5 b4 b3 b2 b1 b0

PULL register 2 (PULL2) [address 0FF1h]

b	Name	Functions	After reset	RW
0	$P6_0$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
1	$P6_1$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
2	$P6_2$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
3	$P6_3$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
4	$P6_4$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
5	$P6_5$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
6	$P6_6$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
7	$P6_7$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW

Note: In port(s) set to output mode, each corresponding bit becomes invalid and pull-up register is not connected.

Fig.4.50 Structure of PULL register 2

PULL register 3

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0			

PULL register 3 (PULL3) [address 0FF2h]

b	Name	Functions	After reset	RW
0	$P4_0$ to $P4_3$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
1	$P4_4$ to $P4_7$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
2	$P7_2$ to $P7_4$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
3	If writing to this bit, write "0". Do not write "1".		0	RW
4	The values are "0" at reading. If writing to these bits, write "0".		0	RO
5			0	RO
6			0	RO
7			0	RO

Note: In port(s) set to output mode, each corresponding bit becomes invalid and pull-up register is not connected.

Fig.4.51 Structure of PULL register 3

Clock output control register

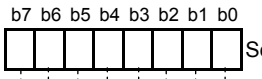
b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

Clock output control register (CKOUT) [address 0FF3h]

b	Name	Functions	After reset	RW
0	$P7_2$ clock output control bits	b1 b0 0 0: Timer 2 output	0	RW
1		0 1: System clock ϕ output 1 0: X_{CIN} frequency signal output 1 1: Do not select.	0	RW
2	The valaues are “0” at reading. If writing to these bits, write “0”.		0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Fig.4.52 Structure of Clock output control register

When port P0 direction register is in output mode:
Segment output disable register 0

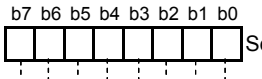


Segment output disable register 0 (SEG0) [address 0FF4h]

b	Name	Functions	After reset	RW
0	Segment output disable bit 0	0: Segment output SEG_8 1: Output port $P0_0$	1	RW
1	Segment output disable bit 1	0: Segment output SEG_9 1: Output port $P0_1$	1	RW
2	Segment output disable bit 2	0: Segment output SEG_{10} 1: Output port $P0_2$	1	RW
3	Segment output disable bit 3	0: Segment output SEG_{11} 1: Output port $P0_3$	1	RW
4	Segment output disable bit 4	0: Segment output SEG_{12} 1: Output port $P0_4$	1	RW
5	Segment output disable bit 5	0: Segment output SEG_{13} 1: Output port $P0_5$	1	RW
6	Segment output disable bit 6	0: Segment output SEG_{14} 1: Output port $P0_6$	1	RW
7	Segment output disable bit 7	0: Segment output SEG_{15} 1: Output port $P0_7$	1	RW

Fig.4.53 Structure of Segment output disable register 0

When port P2 direction register is in output mode:
Segment output disable register 1

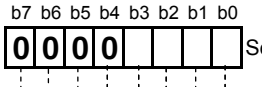


Segment output disable register 1 (SEG1) [address 0FF5h]

b	Name	Functions	After reset	RW
0	Segment output disable bit 8	0: Segment output SEG_0 1: Output port $P2_0$	1	RW
1	Segment output disable bit 9	0: Segment output SEG_1 1: Output port $P2_1$	1	RW
2	Segment output disable bit 10	0: Segment output SEG_2 1: Output port $P2_2$	1	RW
3	Segment output disable bit 11	0: Segment output SEG_3 1: Output port $P2_3$	1	RW
4	Segment output disable bit 12	0: Segment output SEG_4 1: Output port $P2_4$	1	RW
5	Segment output disable bit 13	0: Segment output SEG_5 1: Output port $P2_5$	1	RW
6	Segment output disable bit 14	0: Segment output SEG_6 1: Output port $P2_6$	1	RW
7	Segment output disable bit 15	0: Segment output SEG_7 1: Output port $P2_7$	1	RW

Fig.4.54 Structure of Segment output disable register 1

When port P1, 3 direction registers are in output mode:
Segment output disable register 2

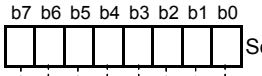


Segment output disable register 2 (SEG2) [address 0FF6h]

b	Name	Functions	After reset	RW
0	Segment output disable bit 16	0: Segment output SEG_{16} to SEG_{19} 1: Output port $P1_0$ to $P1_3$	1	RW
1	Segment output disable bit 17	0: Segment output SEG_{20} to SEG_{23} 1: Output port $P1_4$ to $P1_7$	1	RW
2	Segment output disable bit 18	0: Segment output SEG_{24} to SEG_{27} 1: Output port $P3_0$ to $P3_3$	1	RW
3	Segment output disable bit 19	0: Segment output SEG_{28} to SEG_{31} 1: Output port $P3_4$ to $P3_7$	1	RW
4	If writing to these bits, write “0”. Do not write “1”.		0	RW
5			0	RW
6			0	RW
7			0	RW

Fig.4.55 Structure of Segment output disable register 2

When port Pj (j = 0, 2) direction register is in input mode:
Segment output disable register i (i = 0, 1)



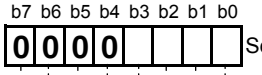
Segment output disable register i (SEGi) (i = 0, 1) [addresses 0FF4h, 0FF5h]

b	Name	Functions	After reset	RW
0	Port Pi_0 pull-up control bit	0: No pull-up 1: Pull-up	1	RW
1	Port Pi_1 pull-up control bit	0: No pull-up 1: Pull-up	1	RW
2	Port Pi_2 pull-up control bit	0: No pull-up 1: Pull-up	1	RW
3	Port Pi_3 pull-up control bit	0: No pull-up 1: Pull-up	1	RW
4	Port Pi_4 pull-up control bit	0: No pull-up 1: Pull-up	1	RW
5	Port Pi_5 pull-up control bit	0: No pull-up 1: Pull-up	1	RW
6	Port Pi_6 pull-up control bit	0: No pull-up 1: Pull-up	1	RW
7	Port Pi_7 pull-up control bit	0: No pull-up 1: Pull-up	1	RW

Note: In port(s) set to output mode, pull-up resistor is not connected.

Fig.4.56 Structure of Segment output disable register i (i = 0, 2)

When port P1, 3 direction registers are in input mode:
Segment output disable register 2



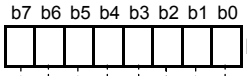
Segment output disable register 2 (SEG2) [address 0FF6h]

b	Name	Functions	After reset	RW
0	Port $P1_0$ to $P1_3$ pull-up control bit	0: No pull-up 1: Pull-up	1	RW
1	Port $P1_4$ to $P1_7$ pull-up control bit	0: No pull-up 1: Pull-up	1	RW
2	Port $P3_0$ to $P3_3$ pull-up control bit	0: No pull-up 1: Pull-up	1	RW
3	Port $P3_4$ to $P3_7$ pull-up control bit	0: No pull-up 1: Pull-up	1	RW
4	If writing to these bits, write “0”. Do not write “1”.		0	RW
5			0	RW
6			0	RW
7			0	RW

Note: In port(s) set to output mode, pull-up resistor is not connected.

Fig.4.57 Structure of Segment output disable register 2

Key input control register

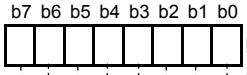


Key input control register (KIC) [address 0FF7h]

b	Name	Functions	After reset	RW
0	$P4_4$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
1	$P4_5$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
2	$P4_6$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
3	$P4_7$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
4	$P2_0$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
5	$P2_1$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
6	$P2_2$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
7	$P2_3$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW

Fig.4.58 Structure of Key input control register

ROM correction address 1 high-order register
ROM correction address 1 low-order register



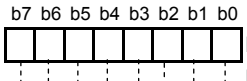
ROM correction address 1 high-order register (RCA1H) [address 0FF8h]
ROM correction address 1 low-order register (RCA1L) [address 0FF9h]

b	Functions	After reset	RW
0	Set the start address of the program to be corrected.	0	RW
1		0	RW
2		0	RW
3		0	RW
4		0	RW
5		0	RW
6		0	RW
7		0	RW

Notes: 1. Specify the start address of each instruction (Op code address) as ROM correction address.
2. Do not set any addresses other than those located in ROM area to ROM correction address registers. Do not set the same addresses to both ROM correction address 1 registers and ROM correction address 2 registers.

Fig.4.59 Structure of ROM correction address 1 high-order register and ROM correction address 1 low-order register

ROM correction address 2 high-order register
ROM correction address 2 low-order register



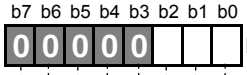
ROM correction address 2 high-order register (RCA2H) [address 0FFAh]
ROM correction address 2 low-order register (RCA2L) [address 0FFBh]

b	Functions	After reset	RW
0	Set the start address of the program to be corrected.	0	RW
1		0	RW
2		0	RW
3		0	RW
4		0	RW
5		0	RW
6		0	RW
7		0	RW

Notes: 1. Specify the start address of each instruction (Op code address) as ROM correction address.
2. Do not set any addresses other than those located in ROM area to ROM correction address registers. Do not set the same addresses to both ROM correction address 1 registers and ROM correction address 2 registers.

Fig.4.60 Structure of ROM correction address 2 high-order register and ROM correction address 2 low-order register

ROM correction enable register



ROM correction enable register (RCR) [address 0FFCh]

b	Name	Functions	After reset	RW
0	ROM correction address 1 enable bit (RC0)	0: Disabled 1: Enabled	0	RW
1	ROM correction address 2 enable bit (RC1)	0: Disabled 1: Enabled	0	RW
2	ROM correction memory selection bit (RC2)	0: Branch to RAM area 1: Branch to ROM area	0	RW
3	The values are “0” at reading. If writing to these bits, write “0”.		0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Note: When using ROM correction function, make sure to enable address enable bits after setting ROM correction address registers.

Fig.4.61 Structure of ROM correction enable register

5. Reference

Datasheet
38D5 Group Datasheet
(Use the most recent version of the document on the Renesas Technology Website.)

Technical News/Technical Update
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Website and Support

Renesas Technology Corporation website
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REVISION HISTORY	38D5 Group List of Registers

Rev.	Date	Description	
		Page	Summary
1.00	Jan 17, 2007	—	First edition issued
2.00	April 20, 2007	4	Figure 4.5 CPU mode register 2: Notes revised
		24	Figure 4.34 Compare register 1, 2, 3(low-order, high-order): Notes revised
		28	Figure 4.39 CPU mode register: Notes revised
		33, 34	Figures 4.46 to 48 Flash memory control registers added.
4.00	Aug 08, 2007	4	Figure 4.5 CPU mode register 2: Note 1revised
		28	Figure 4.39 CPU mode register: Notes 4 and 5 added

Notes regarding these materials

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