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April 1st, 2010
Renesas Electronics Corporation

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38D5 Group

Clock Generating Circuit (Processing During a Power Failure)

1. Abstract

The following article introduces and shows an example of how to use the Clock Generating Circuit (Processing During a Power Failure) in the 38D5 Group.

2. Introduction

The application explained in this document applies to the following MCU and parameters:

- Applicable MCU: 38D5 Group (QzROM version)
- Main clock oscillation frequency ($f(XIN)$): 8 MHz
- Sub clock oscillation frequency ($f(XCIN)$): 32.768 kHz
- OSCSEL pin: "L" input

The flash memory version does not have the OSCSEL pin. The on-chip oscillator does not stop in low-speed mode. When reducing current consumption, stop the on-chip oscillator using the program.

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the user system operating parameters.

3. Contents

3.1 Clock Generation Circuit (Processing During a Power Failure)

Outline: During a power failure, the backup power supply enables the clock count in low-speed and wait modes and allows low power consumption operation.

Specifications:

- High-speed mode operation is selected under normal conditions.
- When a power failure is detected, operation is switched to low-speed mode and the main clock oscillation stops.
- Using wait mode, the timer interrupt routine that occurs every second confirms the conditions for exit from a power failure.
- When an exit from power failure is detected, the main clock oscillation starts. After oscillation is stabilized, the system clock is switched to high-speed mode.

Figure 3.1 shows a Mode Transition Example of System Clock ϕ During a Power Failure, Figure 3.2 shows the Relevant Register Settings, and Figure 3.3 shows the Control Procedure. (0) to (8) in figures show the corresponding parts in each figure.

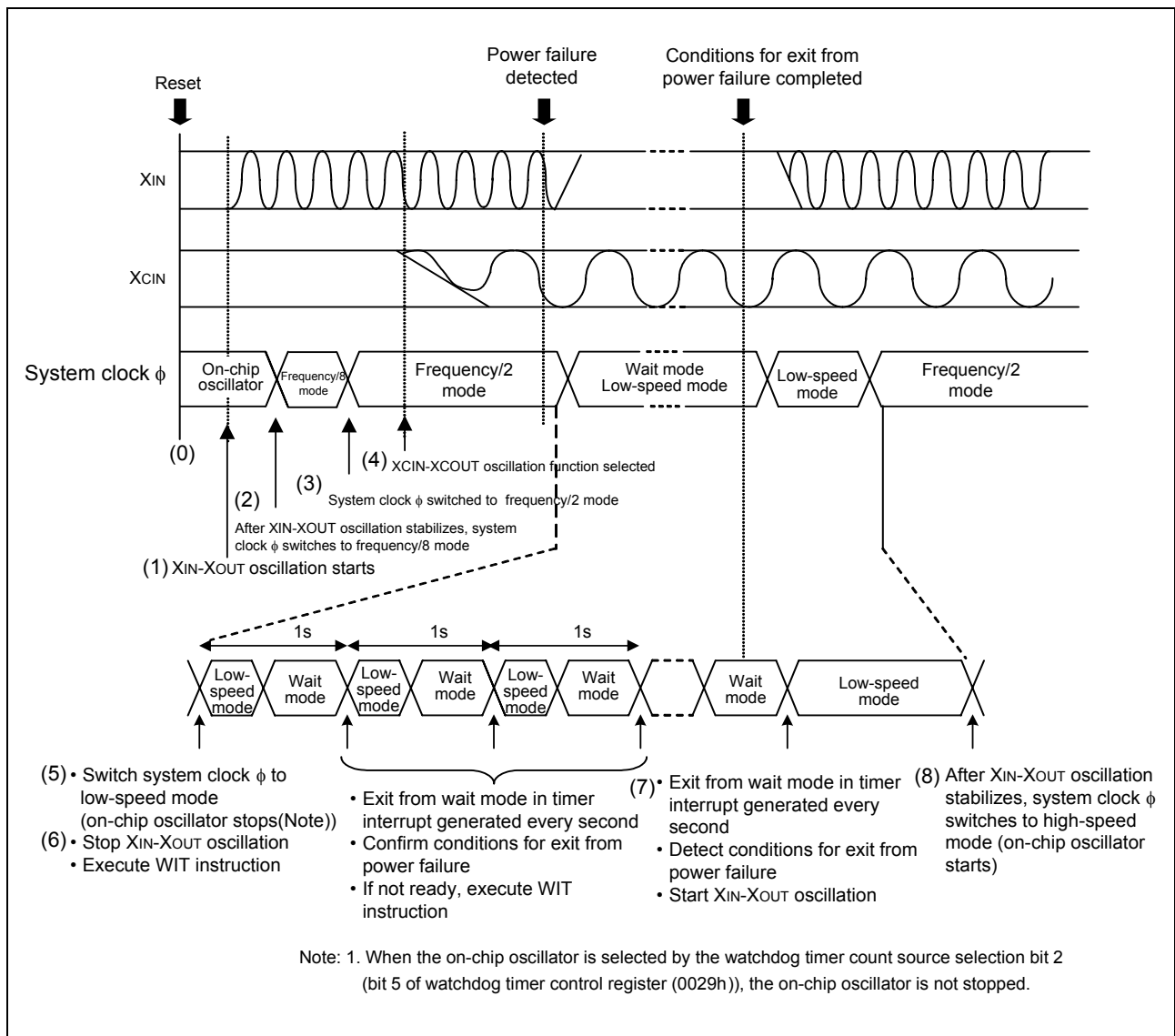


Figure 3.1 Mode Transition Example of System Clock ϕ During a Power Failure (OSCSEL = "L")

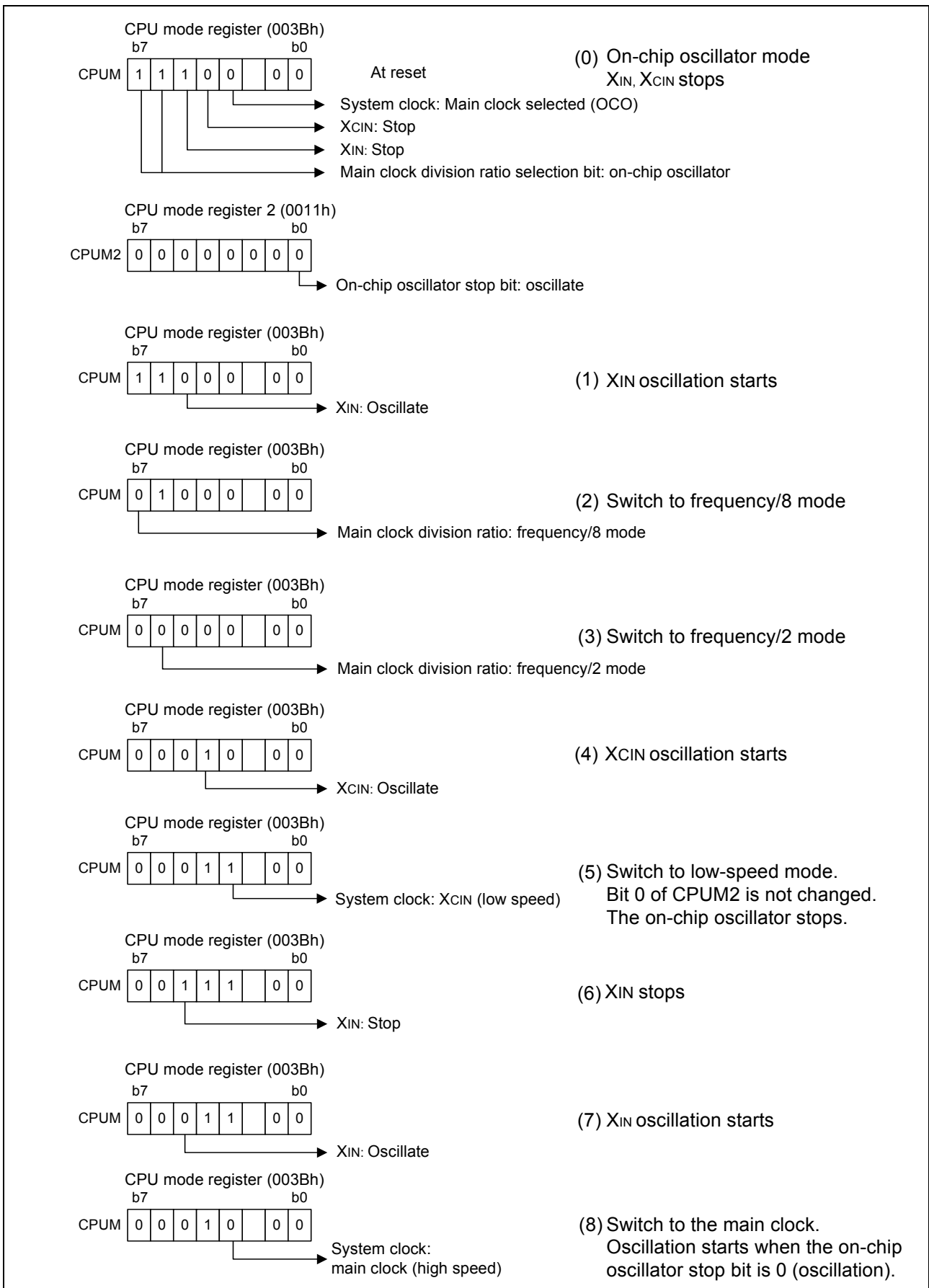


Figure 3.2 Relevant Register Settings

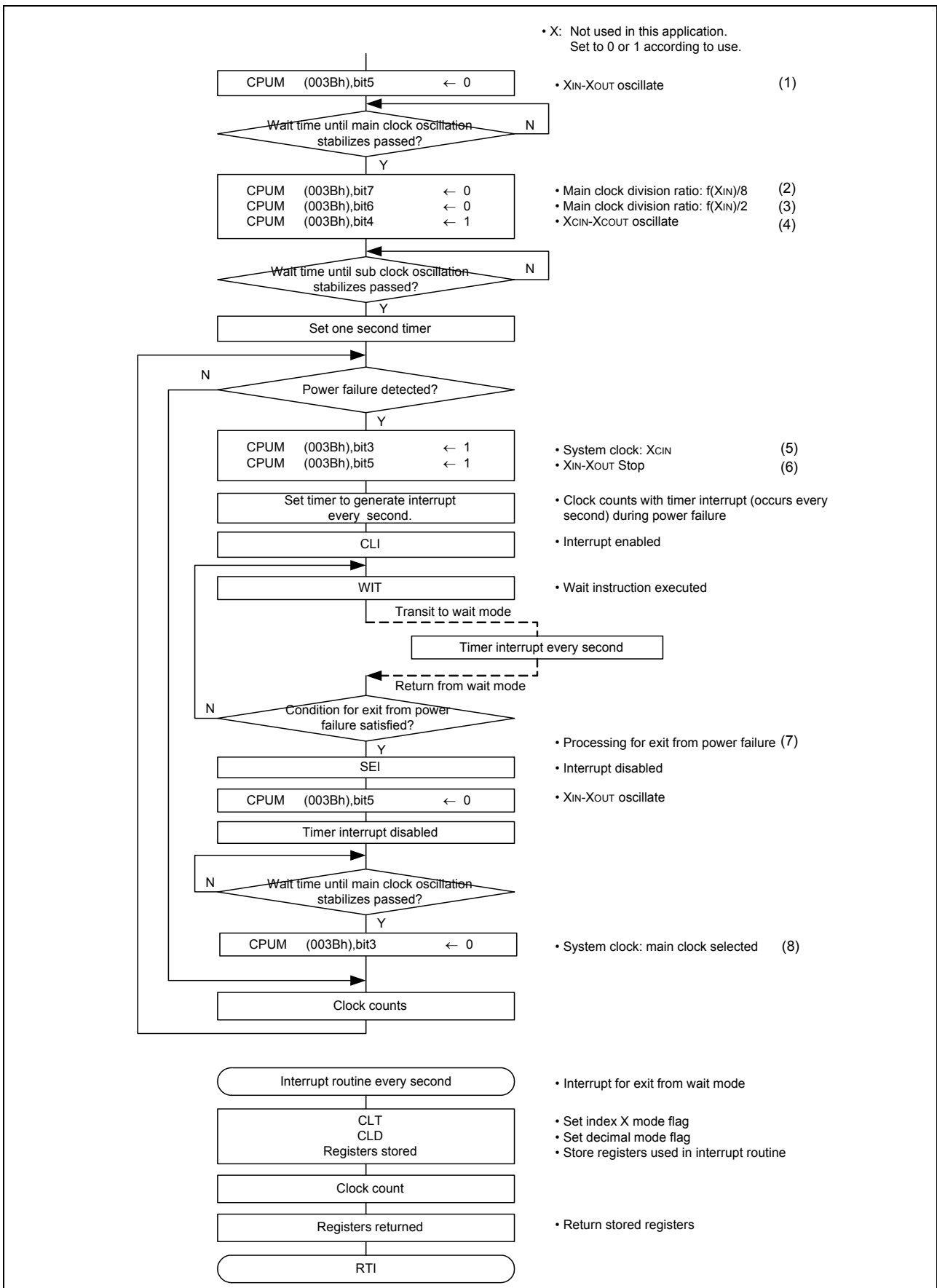


Figure 3.3 Control Procedure

4. Reference Document

Datasheet

38D5 Group Datasheet

(Use the most recent version of the document on the Renesas Technology Web site.)

Technical News/Technical Update

(Use the most recent version of the document on the Renesas Technology Web site.)

5. Sample Programming Code

Please visit the Renesas Technology Web site for a reference program.

Click Application Note in the left menu of the 38D5 Group.

Web site and Support

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<http://www.renesas.com/>

Inquiries
<http://www.renesas.com/inquiry>
csc@renesas.com

REVISION HISTORY	38D5 Group Clock Generating Circuit (Processing During a Power Failure)
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Rev.	Date	Description	
		Page	Summary
1.00	Sep 15, 2006	-	First Edition issued
2.00	May 29, 2007	Full	Full-page revised

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