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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

38D5 Group

A/D Converter

1. Abstract

This document describes the A/D conversion process (8-bit mode) and the A/D conversion operation of the 38D5 Group MCU.

2. Introduction

This document applies to the following MCU:
• Applicable MCU: 38D5 Group

3. Contents

3.1 A/D Conversion Method (8-bit Mode)

In 8-bit mode, eight high-order bits in the 10-bit successive comparison register become the A/D conversion results. When comparing these results with the 8-bit A/D converter results, the comparison voltage varies by VREF/512 (see the underlined formula in the table below). Figure 3.1 shows the Optimal Conversion Characteristics of 8-Bit Mode and 8-Bit A/D Converter.

Table 3.1 Comparison Voltage of 8-Bit Mode and 8-Bit A/D Converter

		8-Bit Mode	8-Bit A/D Converter
Comparison voltage Vref	n = 0	0	0
	n = 1 to 255	$\frac{V_{REF}}{256} \times n$	$\frac{V_{REF}}{256} \times n - \underline{\frac{V_{REF}}{256} \times 0.5}$

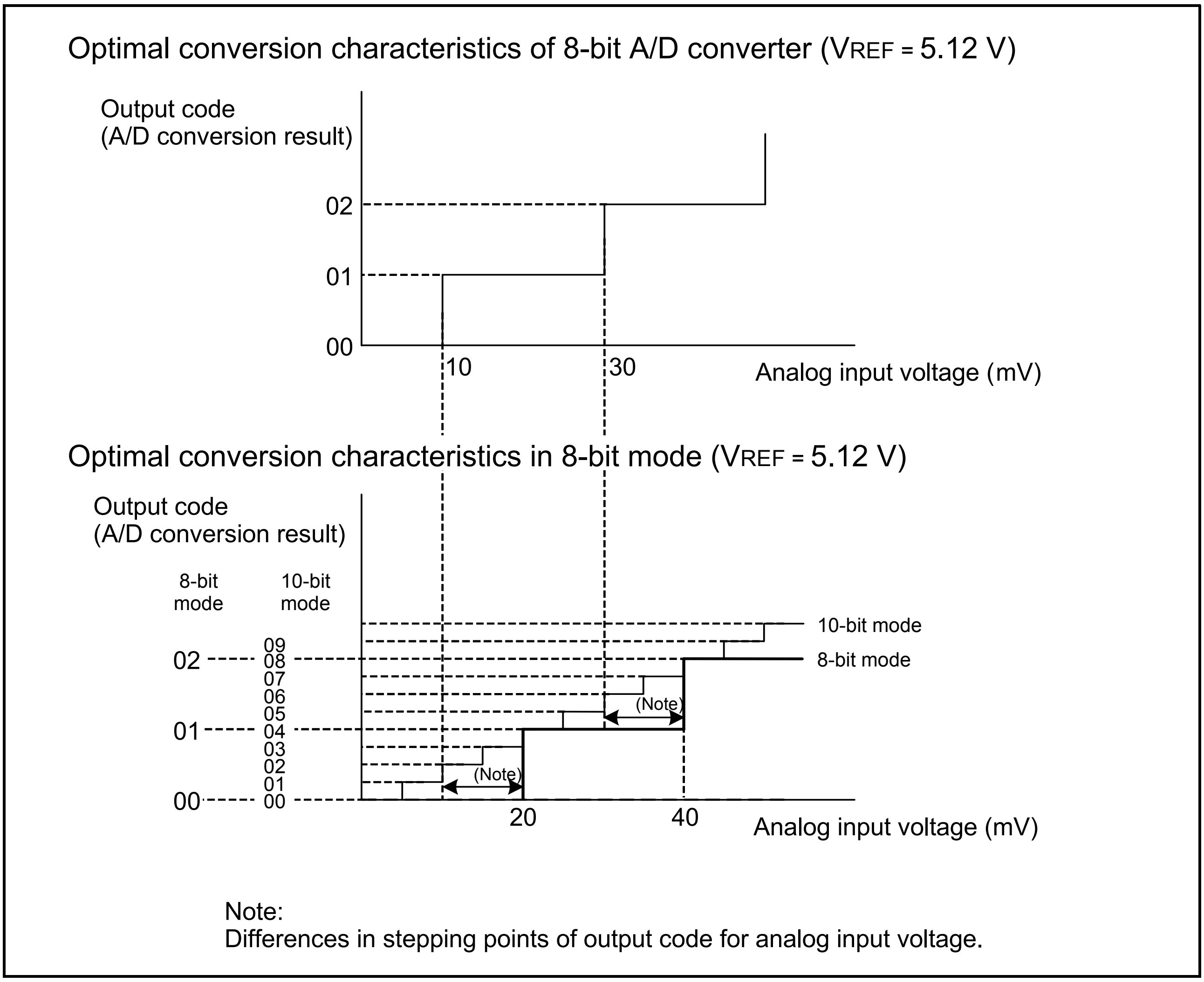

Figure 3.1 Optimal Conversion Characteristics of 8-Bit Mode and 8-Bit A/D Converter

3.2 A/D Conversion Operation

The A/D converter starts by writing “0” to the AD conversion completion bit. Internal operations during A/D conversion are shown below:

1. The value in the A/D conversion buffer register becomes “00h” when A/D conversion starts.
2. The highest-order bit in the A/D conversion buffer register becomes “1” and comparison voltage Vref is input to a comparator. Then, Vref and analog input voltage V_{IN} are compared.
3. If the comparison result is Vref < V_{IN}, the highest-order bit in the A/D conversion buffer register is held as “1”. If Vref > V_{IN}, the highest-order bit becomes “0”.

By performing the above operations to the lowest-order bit in the A/D conversion buffer register, the A/D converter converts an analog value to a digital value. A/D conversion ends in the following time after A/D conversion starts. Then the conversion results are stored in the A/D conversion register (addresses 0016_{16} and 0017_{16}). An A/D conversion interrupt request is generated at the same time as the A/D conversion is completed, and the A/D conversion interrupt request bit becomes “1”

Table 3.2 AD Conversion Time

		Divide-by-2, 4 or 8 mode		Low-speed or on-chip oscillator mode	
		10-bit mode	8-bit mode	10-bit mode	8-bit mode
AD conversion clock selection bit = 0 ΦSOURCE/2	f(ΦAD)	f(XIN)/2		Divide-by-4 of f(OCO)/2	
	tc(ΦAD)	2/f(XIN)		8/f(OCO)	
	AD conversion time (example)	tc(ΦAD) x 62 (15.5 µs)	tc(ΦAD) x 50 (12.5 µs)	tc(ΦAD) x 62 (99.2 µs)	tc(ΦAD) x 50 (80.0 µs)
AD conversion clock selection bit = 1 ΦSOURCE/8	f(ΦAD)	f(XIN)/8		Divide-by-4 of f(OCO)/8	
	tc(ΦAD)	8/f(XIN)		32/f(OCO)	
	AD conversion time (example)	tc(ΦAD) x 62 (62.0 µs)	tc(ΦAD) x 50 (50.0 µs)	tc(ΦAD) x 62 (396.8 µs)	tc(ΦAD) x 50 (320.0 µs)

AD conversion time examples are when f(XIN) = 8 MHz and f(OCO) = 5 MHz.
f(ΦAD) is the AD conversion clock frequency. ΦSOURCE/2 or ΦSOURCE/8 can be selected for the AD conversion clock. tc(ΦAD) is time for one AD conversion clock period.
ΦSOURCE shows the oscillation frequency of XIN input in divide-by-2, 4 or 8 mode and divide-by-4 of the on-chip oscillator in low-speed or on-chip oscillator mode.

Table 3.3 Relational Expression of Vref and A/D Converter Reference Voltage VREF (10-Bit A/D Mode)

When n = 0	Vref = 0
When n = 1 to 1023	Vref = $\frac{V_{REF}}{1024} \times n$

n: Value of A/D conversion register (decimal notation)

Table 3.4 Relational Expression of Vref and A/D Converter Reference Voltage VREF (8-Bit A/D Mode)

When n = 0	Vref = 0
When n = 1 to 255	Vref = $\frac{V_{REF}}{256} \times n$

n: Value of A/D conversion register (decimal notation)

Table 3.5 Changes of A/D Conversion Buffer Register During A/D Conversion

	Changes in the A/D conversion buffer register(1)	Comparison voltage (Vref) value
Conversion starts	0 0 0 0 0 0 0 0 0 0	0
First comparison	1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2}$
Second comparison	*1 1 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4}$
Third comparison	*1 *2 1 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8}$
⋮	⋮	⋮
Tenth comparison completed	A/D conversion result *1 *2 *3 *4 *5 *6 *7 *8 *9 *10	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \cdots \pm \frac{V_{REF}}{1024}$

*1 to *10: Comparison results of 1 to 10

	Changes in the A/D conversion buffer register(1)	Comparison voltage (Vref) value
Conversion starts	0 0 0 0 0 0 0 0	0
First comparison	1 0 0 0 0 0 0 0	$\frac{V_{REF}}{2}$
Second comparison	*1 1 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4}$
Third comparison	*1 *2 1 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8}$
⋮	⋮	⋮
Eighth comparison completed	A/D conversion result *1 *2 *3 *4 *5 *6 *7 *8	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \cdots \pm \frac{V_{REF}}{256}$

*1 to *8: Comparison results of 1 to 8

Note:

1. The A/D conversion buffer register is in the A/D converter. Changes cannot be seen in the middle of comparisons.

Figure 3.2 shows an A/D Converter Equivalent Circuit and Figure 3.3 shows an A/D Conversion Timing Chart.

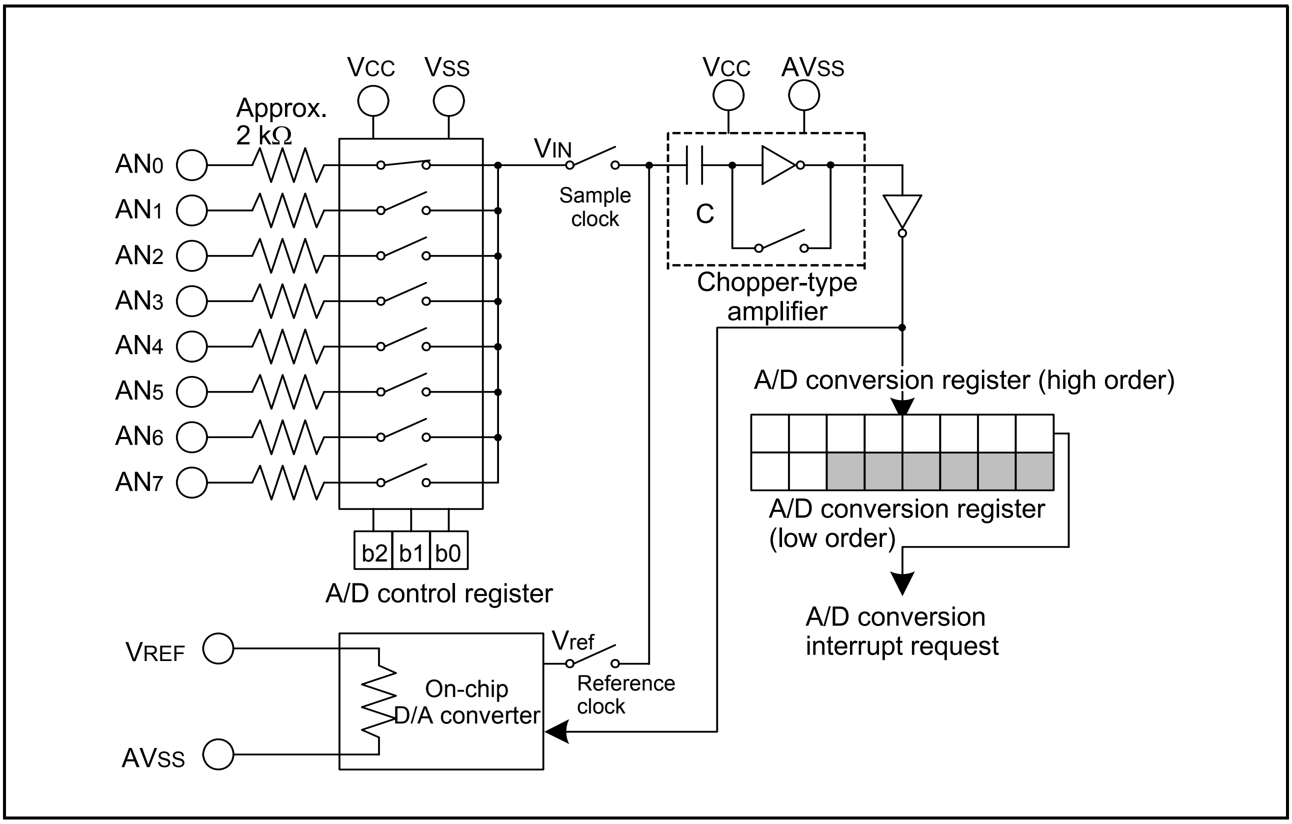

Figure 3.2 A/D Converter Equivalent Circuit

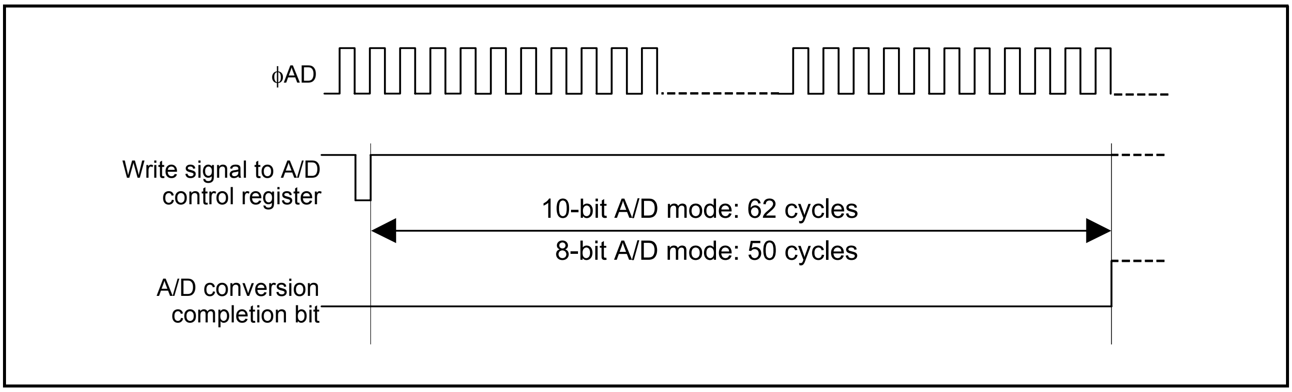

Figure 3.3 A/D Conversion Timing Chart

4. Reference Document

Datasheet
38D5 Group Datasheet
Use the most recent version of the document on the Renesas Technology Web site.

Technical News/Technical Update
Use the most recent version of the document on the Renesas Technology Web site.

Web site and Support

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REVISION HISTORY	38D5 Group A/D Converter

Rev.	Date	Description	
		Page	Summary
1.00	Mar 21, 2008	–	First Edition issued