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April 1st, 2010
Renesas Electronics Corporation

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38D2 Group

LCD Drive Control Circuit (External Dividing Resistor Usage)

1. Abstract

The following article introduces and shows an example of how to use the LCD Drive Control Circuit (External Dividing Resistor Usage) on the 38D2 Group device.

2. Introduction

The application explained in this document applies to the following MCU and parameter(s):

Applicable MCU: 38D2 Group

Frame frequency: 8 MHz

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

3. Contents

3.1 LCD Panel Display (External Dividing Resistor Usage)

Outline: The LCD drive control circuit is used for displaying the LCD panel.

Specifications:

- Segment output SEG0 to SEG19 and common COM0 to COM3 are used.
- Frame frequency = 61 Hz
- Duty ratio = 4, Bias value = 1/3
- Waveform type B
- External dividing resistor is used.
- “M38d2” is displayed.

Figure 3.1 shows a Segment Allocation Example, Figure 3.2 shows the Circuit Example (When Using External Dividing Resistor), Figure 3.3 shows the LCD Display RAM Map, Figure 3.4 shows as LCD Display RAM Setting Example, Figure 3.5 and Figure 3.6 show the Relevant Register Settings, and Figure 3.7 shows the Control Procedure.

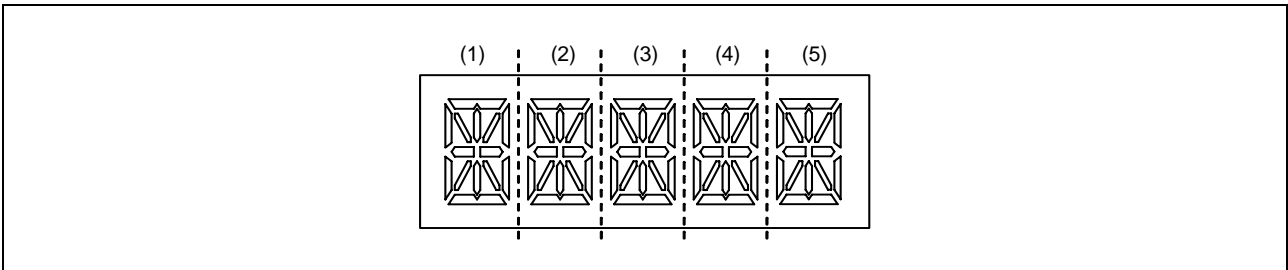


Figure 3.1 Segment Allocation Example

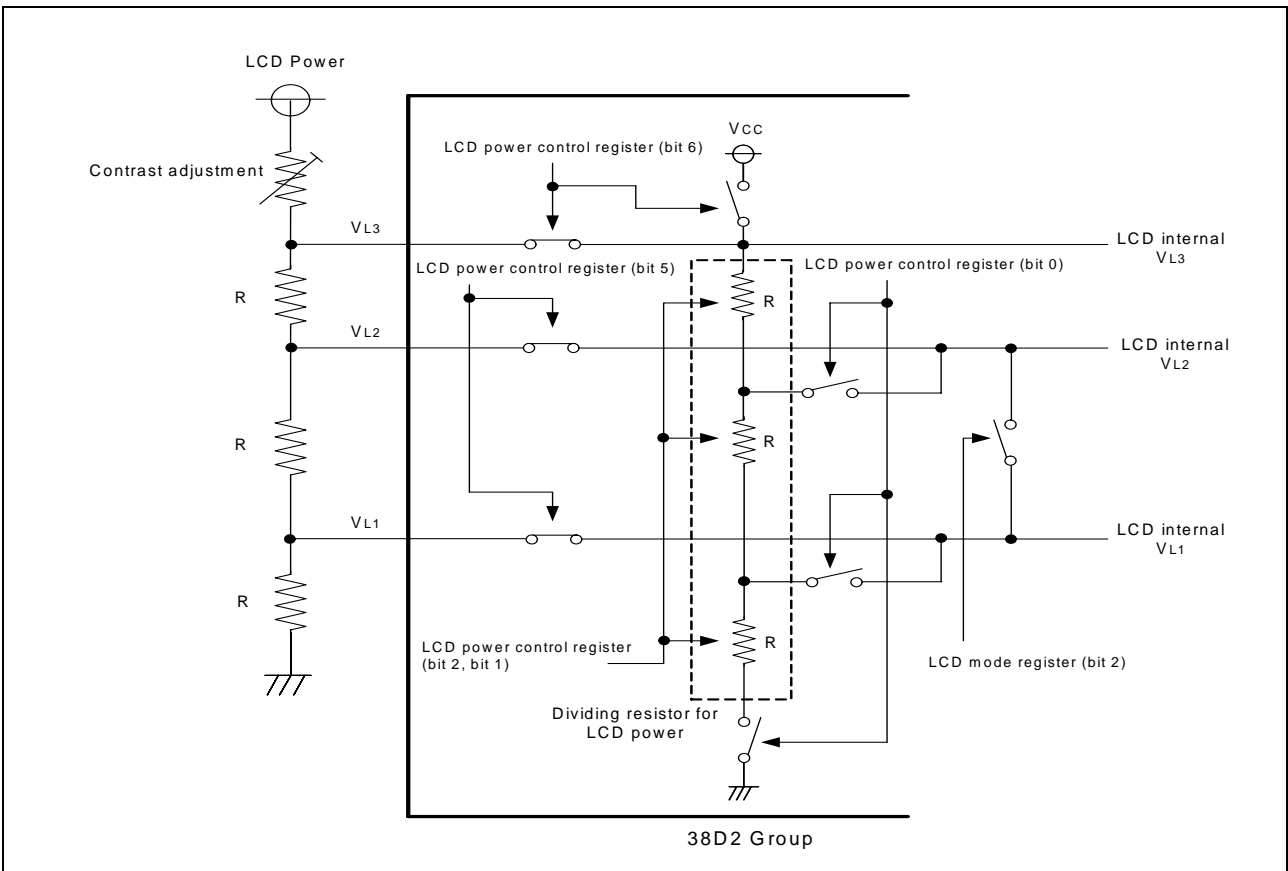


Figure 3.2 Circuit Example (When Using External Dividing Resistor)

address \ bit		7	6	5	4	3	2	1	0
		COM ₃	COM ₂	COM ₁	COM ₀	COM ₃	COM ₂	COM ₁	COM ₀
0040h	LRAM0			SEG ₁				SEG ₀	
0041h	LRAM1			SEG ₃				SEG ₂	
0042h	LRAM2			SEG ₅				SEG ₄	
0043h	LRAM3			SEG ₇				SEG ₆	
0044h	LRAM4			SEG ₉				SEG ₈	
0045h	LRAM5			SEG ₁₁				SEG ₁₀	
0046h	LRAM6			SEG ₁₃				SEG ₁₂	
0047h	LRAM7			SEG ₁₅				SEG ₁₄	
0048h	LRAM8			SEG ₁₇				SEG ₁₆	
0049h	LRAM9			SEG ₁₉				SEG ₁₈	
004Ah	LRAM10			SEG ₂₁				SEG ₂₀	
004Bh	LRAM11			SEG ₂₃				SEG ₂₂	

Figure 3.3 LCD Display RAM Map

address \ bit		7	6	5	4	3	2	1	0
		COM ₃	COM ₂	COM ₁	COM ₀	COM ₃	COM ₂	COM ₁	COM ₀
0040h	LRAM0	h	g	f	e	d	c	b	a
0041h	LRAM1	m	l		n	k	j		i
0042h	LRAM2	h	g	f	e	d	c	b	a
0043h	LRAM3	m	l		n	k	j		i
0044h	LRAM4	h	g	f	e	d	c	b	a
0045h	LRAM5	m	l		n	k	j		i
0046h	LRAM6	h	g	f	e	d	c	b	a
0047h	LRAM7	m	l		n	k	j		i
0048h	LRAM8	h	g	f	e	d	c	b	a
0049h	LRAM9	m	l		n	k	j		i
004Ah	LRAM10								
004Bh	LRAM11								

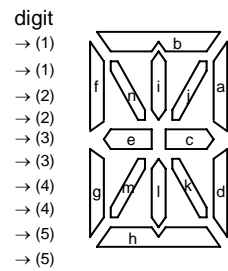


Figure 3.4 LCD Display RAM Setting Example

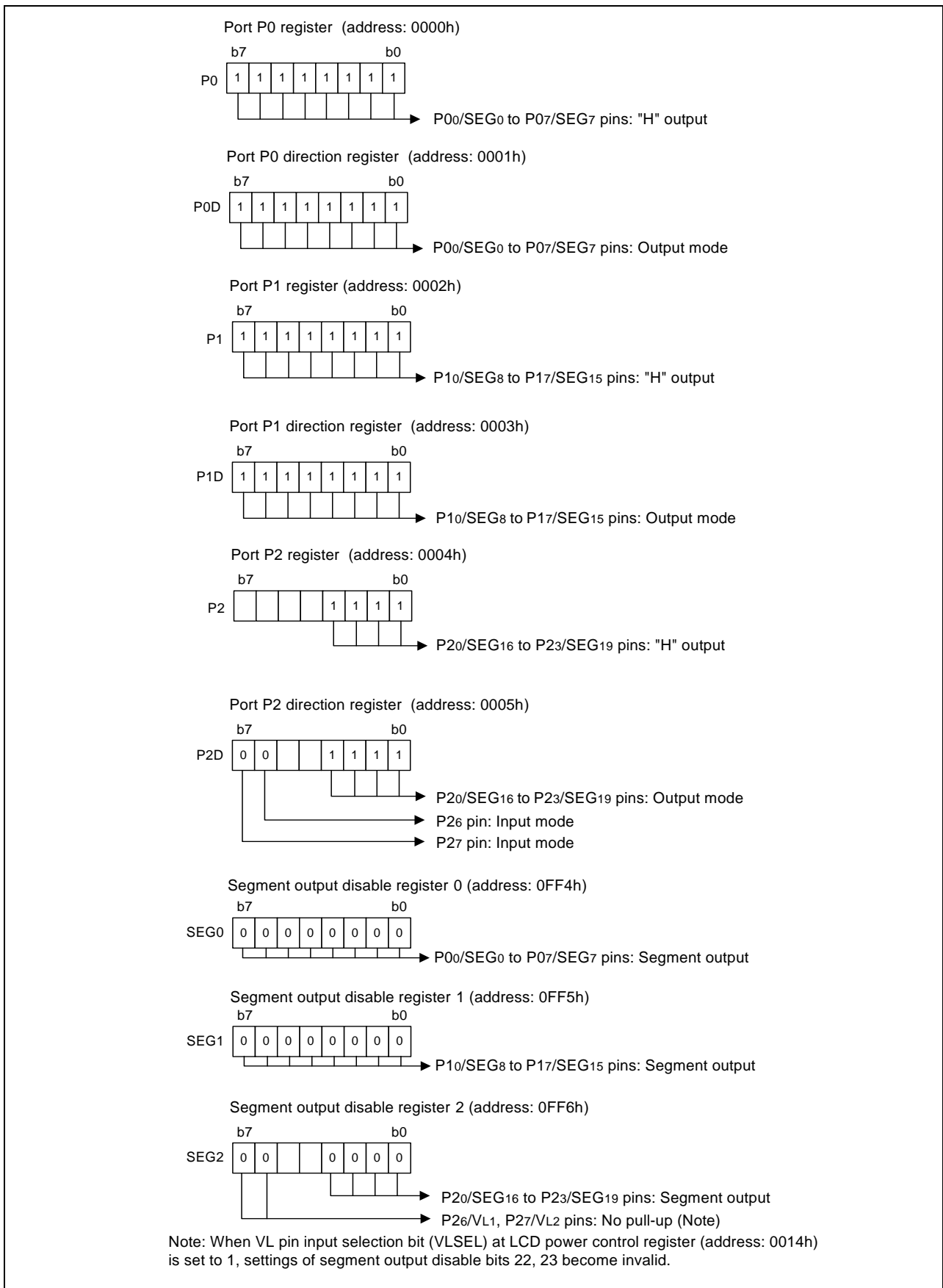


Figure 3.5 Relevant Register Settings (1)

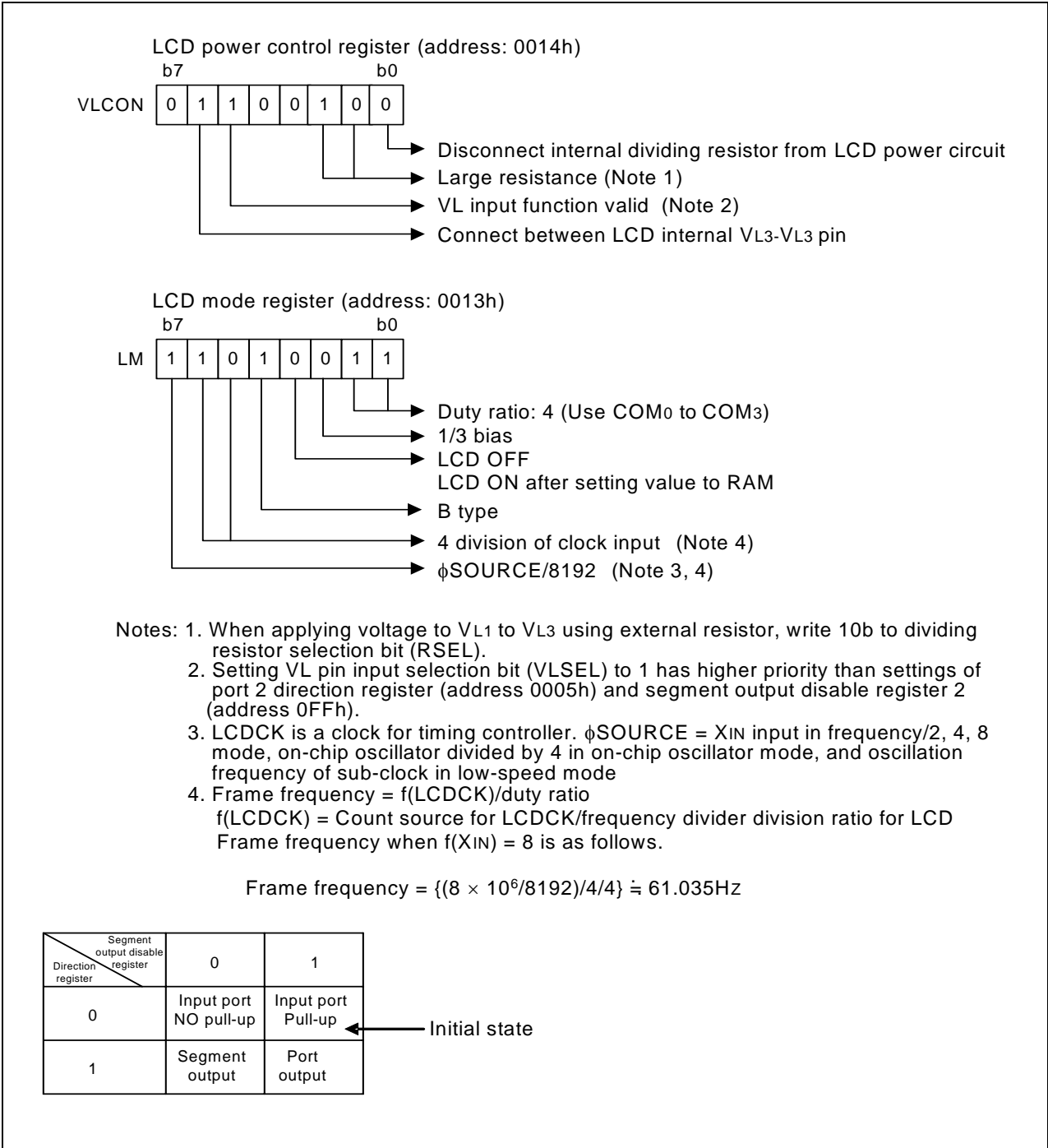


Figure 3.6 Relevant Register Settings (2)

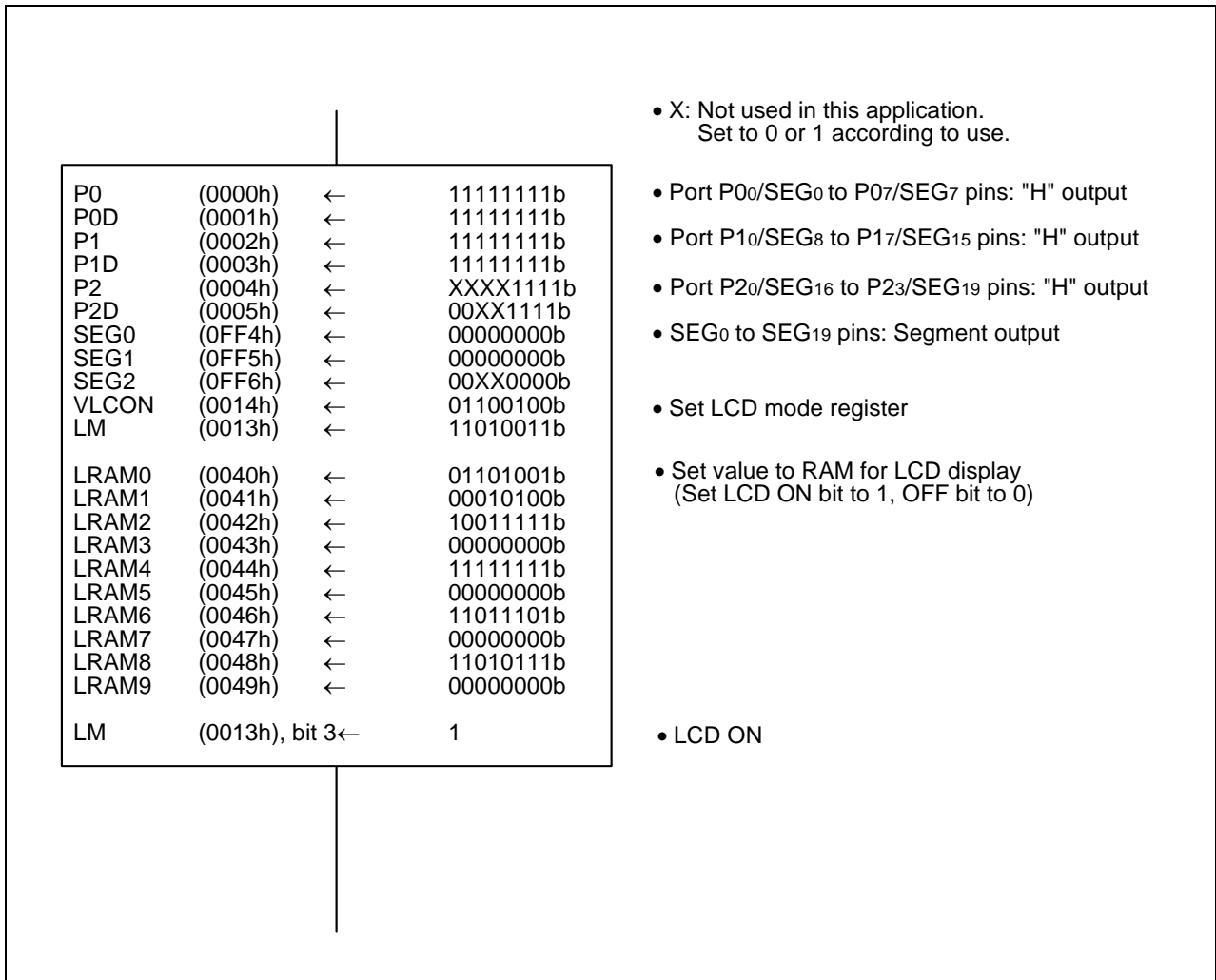


Figure 3.7 Control Procedure

4. Sample Programming Code

Download a sample program from the Renesas Technology website.
To download, click “Application Notes” in the left side menu on the page of the 38D2 Group.

5. Reference Document

Datasheet
38D2 Group Datasheet
Download the latest version from the Renesas Technology website.

Technical News/Technical Update
Download the latest information from the Renesas Technology website.

Website and Support

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REVISION HISTORY	38D2 Group LCD Drive Control Circuit (External Dividing Resistor Usage)
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 9, 2007	-	First Edition issued

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