

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## 38D2 Group

### Reset Circuit

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#### 1. Abstract

The following article introduces and shows reset circuit sequences and connection examples using the reset IC on the 38D2 Group device.

#### 2. Introduction

The application explained in this document applies to the following MCU:  
Applicable MCU: 38D2 Group (QzROM version)

The sequence of the Flash memory version is the same as that of the QzROM version (when OSCSEL = "L").  
Refer to the 38D2 Group datasheet for the reset input waveform.

3. Contents

3.1 Reset Sequence

The MCU enters reset status when the  $\overline{\text{RESET}}$  pin is held at "L" level for 2  $\mu\text{s}$  or more under the circumstance in which the power source voltage is between  $V_{cc}$  (min.) and 5.5 V, and the clock source, such as a quartz-crystal oscillator, is stable. Reset status is released after the  $\overline{\text{RESET}}$  pin is set to "H" and 32768 cycles of OCO (when  $\text{OSCSEL} = \text{"L"}$ ) or 8192 cycles of the XIN input (when  $\text{OSCSEL} = \text{"H"}$ ) has passed and starts sourcing the system clock  $\phi$  to the CPU. Then, the program starts from the address whose high-order address is the content of the address FFFDh and low-order address is the content of the address FFFCh in on-chip oscillator mode (when  $\text{OSCSEL} = \text{"L"}$ ) or frequency divided by 8 mode (when  $\text{OSCSEL} = \text{"H"}$ ). As for the oscillation status of the clock, XIN and XCIN are stopped when  $\text{OSCSEL} = \text{"L"}$  and OCO and XCIN are stopped when  $\text{OSCSEL} = \text{"H"}$ .

Figure 3.1 shows the Reset Sequence When  $\text{OSCSEL} = \text{"L"}$  and Figure 3.2 shows the Reset Sequence When  $\text{OSCSEL} = \text{"H"}$

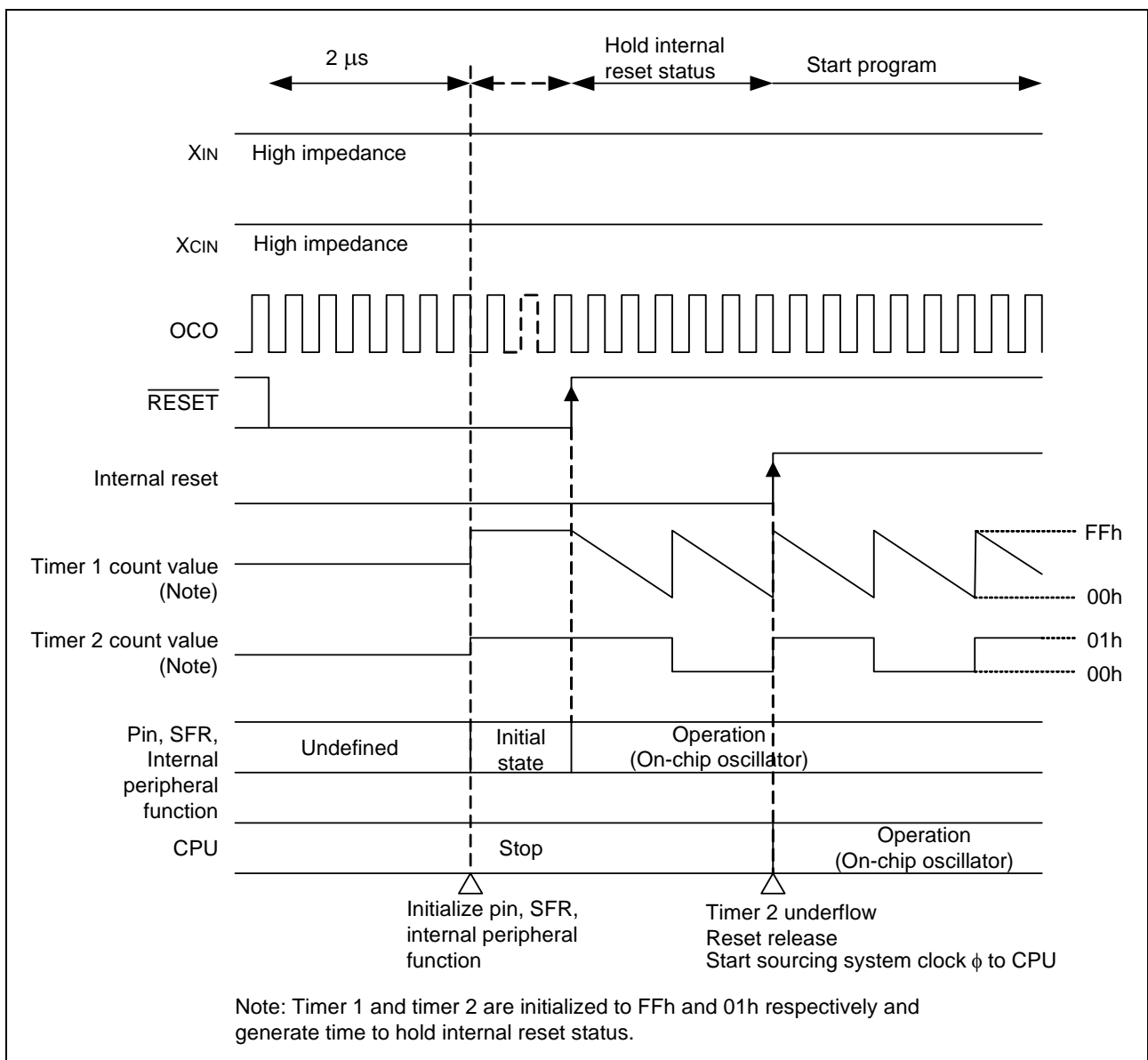


Figure 3.1 Reset Sequence When  $\text{OSCSEL} = \text{"L"}$

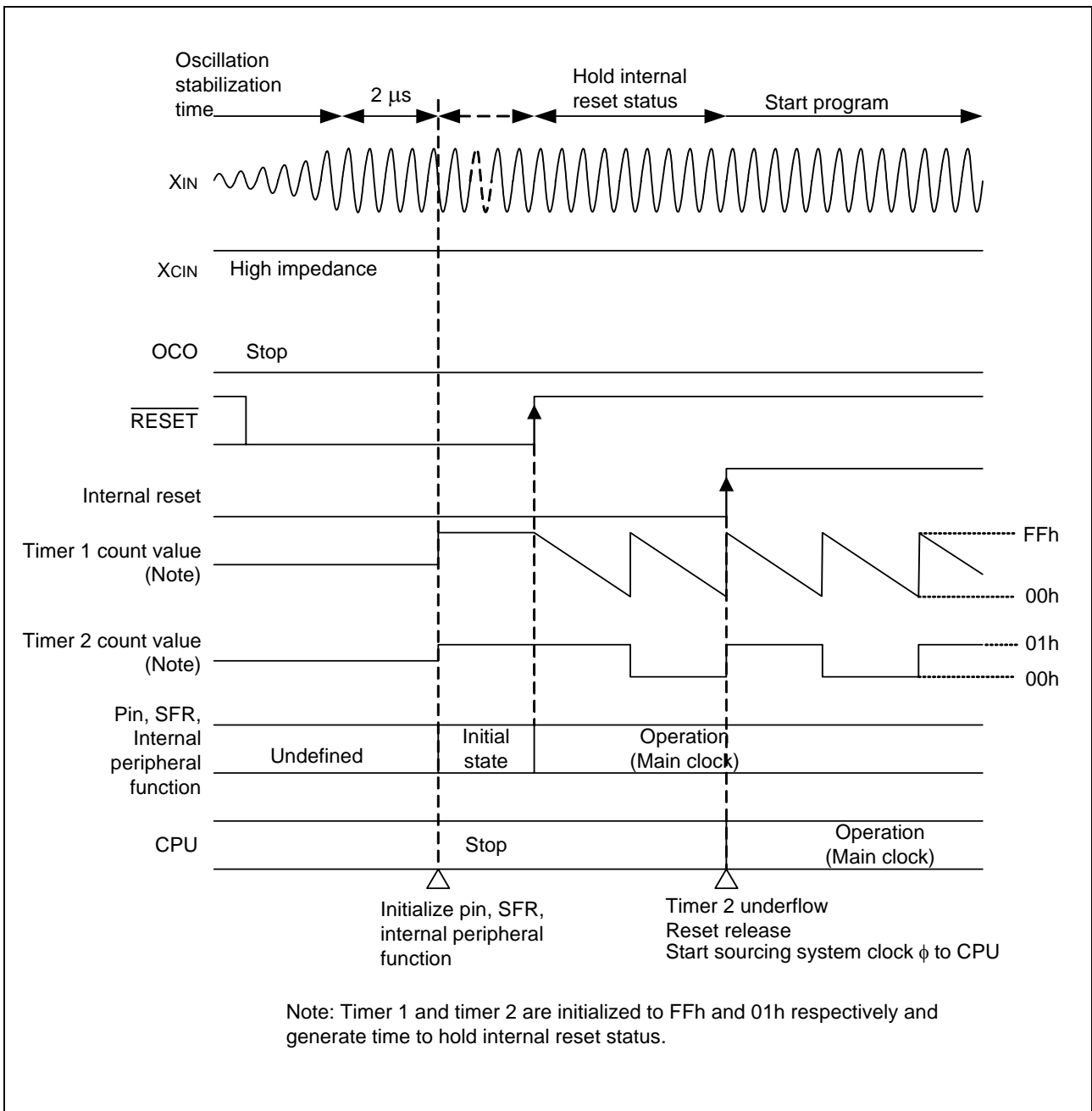


Figure 3.2 Reset Sequence When OSCSEL = "H"

### 3.2 Connection Example Using Reset IC

Figure 3.3 shows the Power-on Reset Circuit Example and Figure 3.4 shows RAM Backup System Example. In this system, the MCU detects system power decrease by INT0 interrupt and is switched to RAM backup mode.

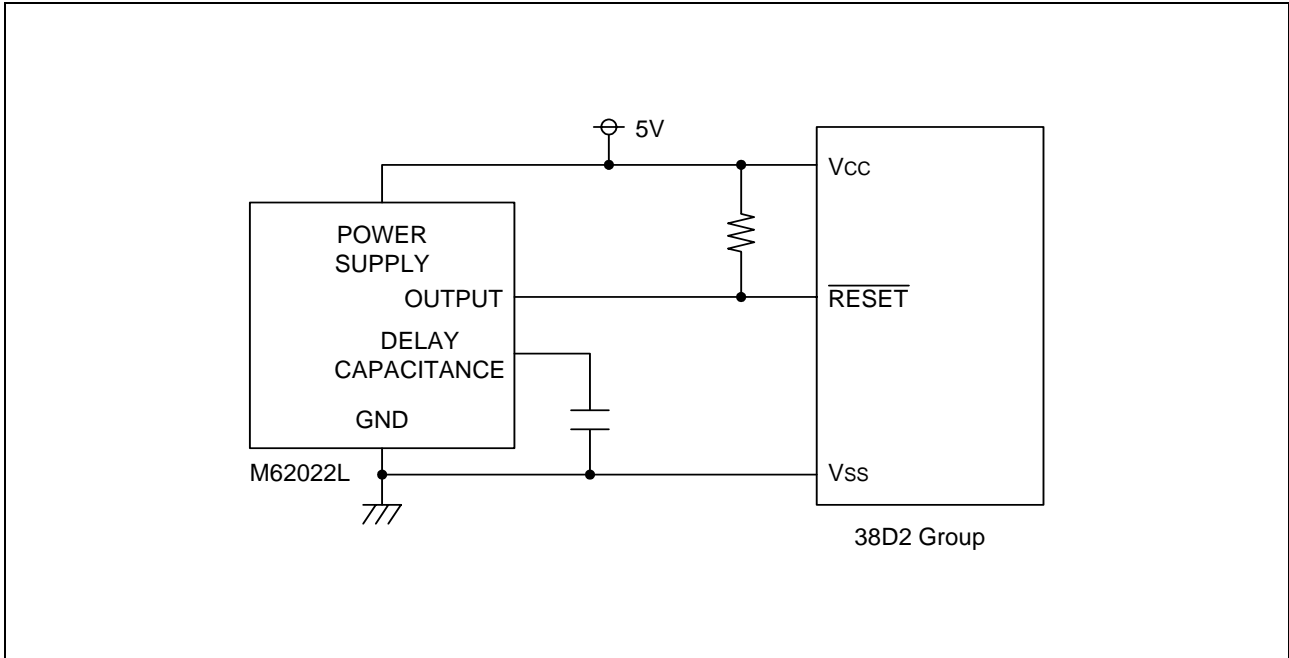


Figure 3.3 Power-on Reset Circuit Example

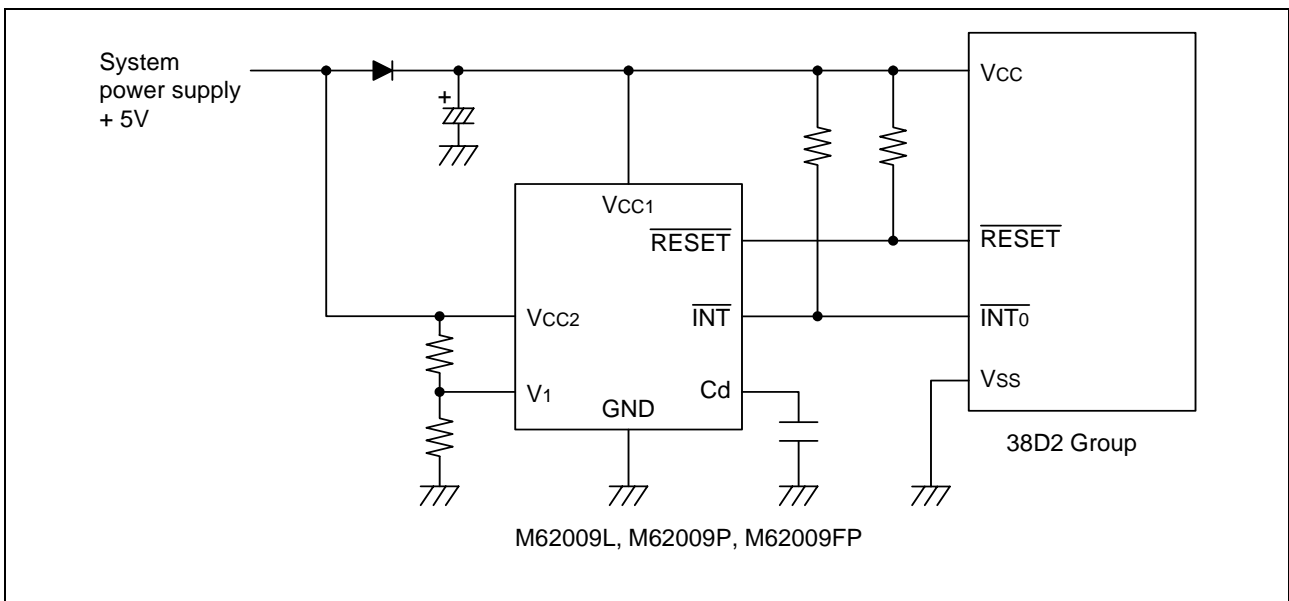


Figure 3.4 RAM Backup System Example

### 3.3 Status of Each Port Immediately After Reset

Table 3.1 lists each pin status when the  $\overline{\text{RESET}}$  pin is held to “L”.

**Table 3.1 Each Pin Status When the  $\overline{\text{RESET}}$  Pin Is Held to “L”**

Pin Name	Pin Status
P0, P1, P2 (SEG0 to SEG23)	Input mode (Pull-up)
P3, P4, P5, P60 to P62	Input mode (High impedance)
COM0 to COM3	Vcc level output

#### **4. Sample Programming Code**

Download a sample program from the Renesas Technology website.  
To download, click “Application Notes” in the left side menu on the page of the 38D2 Group.

#### **5. Reference Document**

Datasheet  
38D2 Group Datasheet  
Download the latest version from the Renesas Technology website.

Technical News/Technical Update  
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REVISION HISTORY	38D2 Group Reset Circuit
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Rev.	Date	Description	
		Page	Summary
1.00	Mar 30, 2007	-	First Edition issued

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