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38D2 Group

Oscillation Control

1. Abstract

This document describes oscillation control of the 38D2 Group MCU.

2. Introduction

The application explained in this document applies to the following MCU:
• Applicable MCU: 38D2 Group

3. Contents

The 38D2 Group MCU can be set to stop the CPU. The CPU can be put on standby using the two power-saving modes listed below:

- Execute the STP instruction to enter stop mode
- Execute the WIT instruction to enter wait mode

3.1 Stop Mode

When the STP instruction is executed, the MCU enters stop mode. In stop mode, the main clock (XIN-XOUT), sub-clock (XCIN-XCOUT), and on-chip oscillator oscillations stop. The system clock ϕ stops "H". The CPU and peripheral functions then stop, and power consumption is reduced.

3.1.1 Status in Stop Mode

Table 3.1 lists the Status in Stop Mode.

Table 3.1 Status in Stop Mode

Item	Function	Pin
Oscillation	Stopped	XIN and XOUT: "H" XCIN and XCOUT: High impedance
On-chip oscillator	Stopped(1)	–
CPU	Stopped	–
System clock ϕ	Stopped "H"	"H" when ϕ output from P36 is selected
I/O ports P0 to P6	Held	The I/O ports are held in their current state when the STP instruction is executed.
Timers	Stopped (timers 1, 2, 3, 4, X and Y) However, timer X and timer Y are only active in event counter mode.	Timers are held in their current state when the STP instruction is executed.
LCD drive control circuit	Stopped(2)	COM and SEG: Vcc when the VL3 connection bit is set to "0" VL3(3) when the VL3 connection bit is set to "1"
Watchdog timer	Stopped(1)	–
Serial I/O1 and serial I/O2	Stopped However, serial I/O1 and serial I/O2 are only active when an external clock is selected.	Serial I/O1 and serial I/O2 are held in their current state when the STP instruction is executed.
A/D converter	Stopped	The A/D converter is held in its current state when the STP instruction is executed.
RAM	Held(4)	–
CPU register and SFR	Held(5)	–

NOTES:
1. When the watchdog timer count source selection bit 2 (bit 5 in the watchdog timer control register (address 002916) is set to "1" (on-chip oscillator divided-by-4), the on-chip oscillator forcibly oscillates and cannot be stopped.
2. The LCD enable bit (bit 3 in the LCD mode register (address 1316)) is forcibly set to "0".
3. VL3 connection bit (bit 6 in the LCD power control register (address 001416))
   0: Connect LCD internal VL3 to VCC
   1: Connect LCD internal VL3 to VL3 pin
4. When voltage supplied to Vcc is more than the RAM hold voltage.
5. When voltage supplied to Vcc is more than the RAM hold voltage. However, the CPU register and SFRs are initialized when the MCU returns by the reset input.

- Example to reduce power consumption
  - Input port: Fix an input port "H" or "L" externally
  - Output port: Fix at the level to which the current does not flow externally
    For example, for a circuit that illuminates an LED when current flows during "L" signal output, an "H" level output is fixed.
  - A/D input pin: Fix the A/D input pin to "H" or "L" externally
  - Complete an A/D conversion
    Confirm that the AD conversion completion bit (bit 3 in the AD control register (address 1516)) is set to "1".
  - VREF input switch bit (bit 0 in the AD conversion register (low-order)(address 1616)): "0"

3.1.2 Exiting Stop Mode

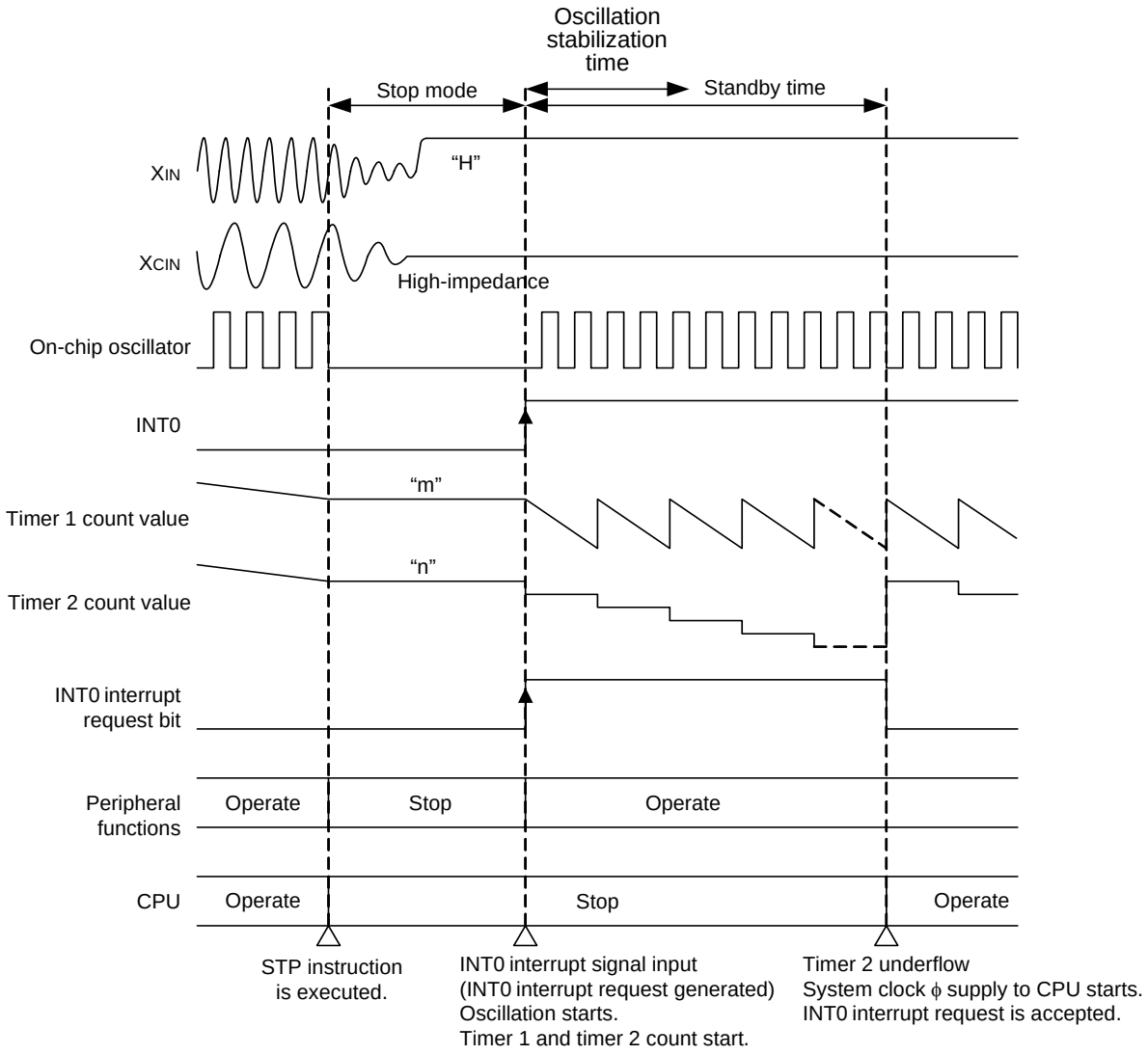
To exit stop mode, generate an enabled interrupt request or input a reset. The MCU's return from stop mode differs between the interrupt request being generated and a reset being input.

- Return by interrupt

If an enabled interrupt request is generated during stop mode(1), stop mode is exited and the on-chip oscillator (when the OSCSEL pin is "L") or the main clock (XIN-XOUT)(when the OSCSEL pin is "H") starts oscillating. On-chip oscillator mode (when the OSCSEL pin is "L") or divide-by-8 mode (when the OSCSEL pin is "H") is selected as the system clock. As oscillation is unstable when it starts, a certain amount of time is necessary for oscillation to stabilize (oscillation stabilization time). When the MCU returns from stop mode from an interrupt, timer 1 and timer 2 generate the stand-by time for the system clock ϕ supply to the CPU(2). When the MCU is returning from stop mode, the on-chip oscillator (when the OSCSEL is "L") becomes the count source, and this standby time is allocated for the system clock's oscillation stabilization time(3). The standby time is completed when timer 2 underflows and system clock ϕ supply to the CPU starts. The generated interrupt request is accepted and the interrupt routine is executed. The watchdog timer does not operate in stop mode, but operates during the standby time. Write to the watchdog timer control register (address 2916) before the STP instruction is executed to prevent underflow during this time(4). After the MCU returns from stop mode, when switching the on-chip oscillator to the main clock or sub-clock, start each oscillation, generate oscillation stabilization standby time with the user program, and switch when oscillation is sufficiently stable. Figures 3.1 and 3.2 show Operation Examples When Returning from Stop Mode Using a Generated INT0 Interrupt Request.

NOTES:

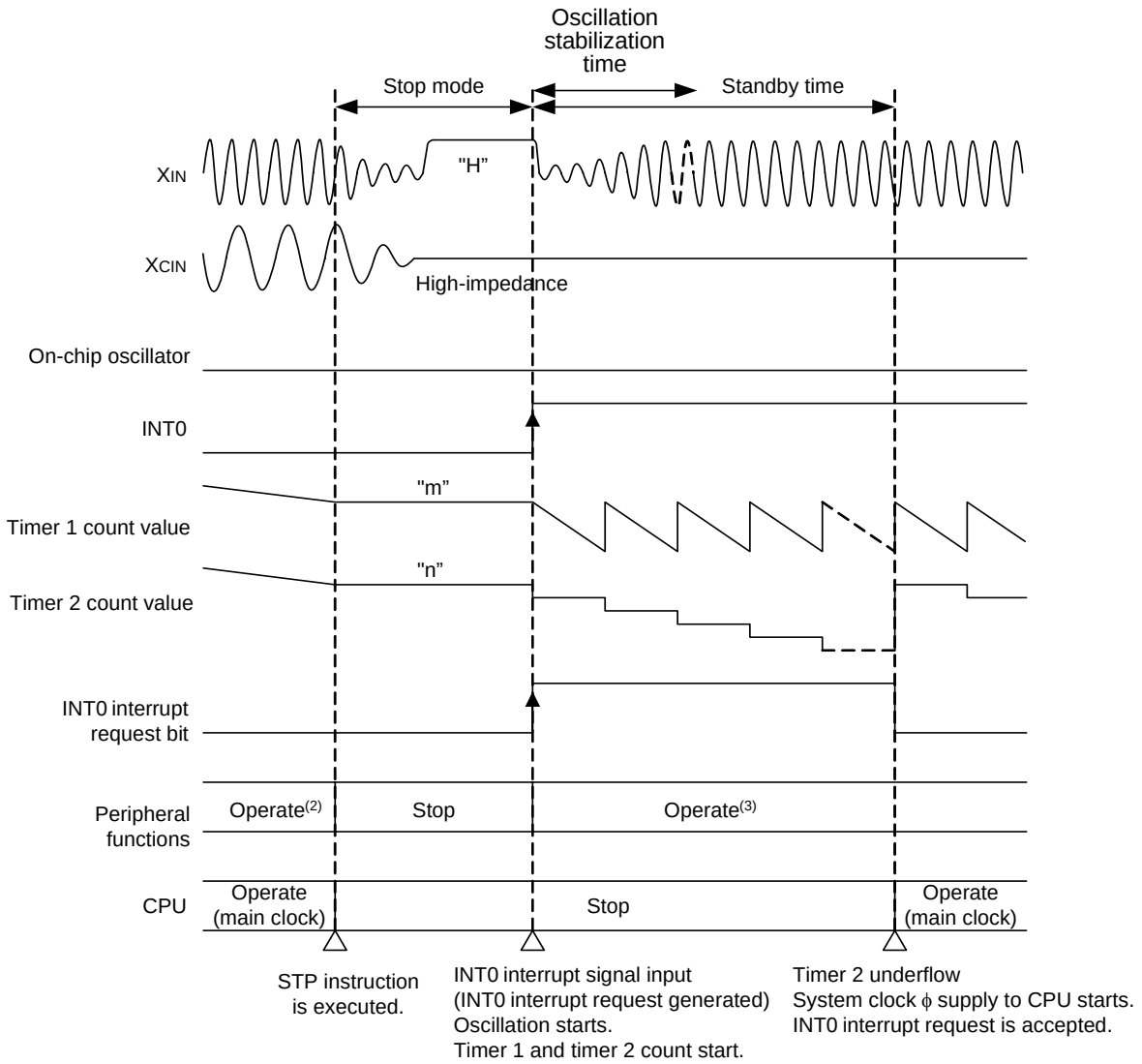
1. The following show the interrupt sources which can be used for returning from stop mode. Enable the interrupt to be used and execute the STP instruction.
   - INT0 to INT2
   - CNTR0 and CNTR1
   - Serial I/O1 and serial I/O2 when an external clock is selected
   - Timer X and timer Y in event counter mode
   - Key input (key-on wake up)
   - A/D conversion (ADKEY function)
2. When using timer 1 and timer 2, first set the following and then execute the STP instruction.
   - Timer 1 register (address 0020_{16}) and timer 2 register (address 0021_{16}): standby time
     Set the standby time to be within the following range.
     Oscillation stabilization time < standby time < time until the watchdog timer underflows
   - Timer 1 interrupt enable bit, timer 2 interrupt enable bit: "0" (interrupts disabled)
3. Only the T2OUT output edge switch bit (bit 7) and timer 2 output selection bit (bit 6) in the timer 12 mode register (address 0025_{16}) are retained -all other bits are set to "0". The timer 1 count source is the timer 1 frequency divider and the timer 2 count source is a timer 1 underflow signal. Since the value in the timer 1234 frequency division selection register (address 0028_{16}) remains unchanged, it is necessary to set the timer 1 division selection in advance.
4. When "1" (on-chip oscillator divided-by-4) is set by the watchdog timer count source selection bit 2, the on-chip oscillator forcibly oscillates and cannot be stopped. At this time, set the STP instruction function selection bit (bit 6 in the watchdog timer control register (address 0029_{16})) to "1" (internal reset occurs when the STP instruction is executed).



NOTES:
1. The timer 1 count source is the frequency divider output for timer 1.
   The timer 2 count source is an underflow signal for timer 1.
   m: Timer 1 setting value, n: timer 2 setting value
2. The peripheral functions operate based on the clocks set by the user.
3. Peripheral functions operate by the on-chip oscillator.
   However, when XCIN is selected for the count source by peripheral functions other than timer 1 and timer 2, XCIN must be reoscillated.

This example shows that the sub-clock oscillates by selecting ϕSOURCE for the watchdog timer count source and the main clock for system clock ϕ.
XIN, XCIN and OCO oscillation depends on the CPU mode register setting.
The CPU operates in on-chip oscillator mode after returning from stop mode, and XIN and XCIN are in oscillation stop state. The rising edge active is set for the INT0 interrupt.

Figure 3.1 Operation Example When Returning from Stop Mode Using a Generated INT0 Interrupt Request (in the Flash Memory Version, or When OSCEL is "L" in the QzROM Version)



NOTES:
1. The timer 1 count source is the frequency divider output for timer 1.
   The timer 2 count source is an underflow signal for timer 1.
   m: Timer 1 setting value, n: timer 2 setting value
2. The peripheral functions operate based on the clocks set by the user.
3. Peripheral functions operate by XIN.
   However, when XCIN is selected for the count source by peripheral functions other than timer 1 and timer 2, Xcin must be reoscillated.

This example shows that the sub-clock oscillates by selecting ϕSOURCE for the watchdog timer count source and the main clock for system clock ϕ.
XIN, XCIN and OCO oscillation depends on the CPU mode register setting.
The CPU operates in the main clock after returning from stop mode, and XIN and OCO are in oscillation stop state. The rising edge active is set for the INT0 interrupt.

Figure 3.2 Operation Example When Returning from Stop Mode Using a Generated INT0 Interrupt Request (OSCSEL = "H" in QzROM version)

- Return by reset input

To exit stop mode, the input level to the $\overline{\text{RESET}}$ pin must be “L”. All I/O ports are changed to in input mode, and on-chip oscillator (when the OSCSEL pin is “L”) oscillation or main clock (XIN-XOUT)(when the OSCSEL pin is “H”) oscillation starts. On-chip oscillator mode (when the OSCSEL pin is “L”) or divide-by-8 mode (when the OSCSEL pin is “H”) is selected for the system clock. Oscillation is unstable when it starts, and a certain amount of time is necessary for oscillation to stabilize (oscillation stabilization time). Hold the $\overline{\text{RESET}}$ pin input level “L” until oscillation is stable. An internal reset occurs when the $\overline{\text{RESET}}$ pin is held “L” for 2 μs or more and the MCU operates according to the reset sequence. Refer to the 38D2 application note Reset Circuit for the reset sequence.

3.1.3 Notes on Stop Mode

1. Return by interrupt
   - Only bits 7 and 6 in the timer 12 mode register are retained - all other bits are set to “0”.
   - The main clock and sub-clock oscillation stabilization time differs. When the MCU is returned from stop mode, if a clock that is not selected for the system clock ϕ is used as a clock for peripheral functions, make sure there is sufficient standby time.

2. When displaying the LCD
   When the STP instruction is executed, the LCD enable bit is set to “0” and the LCD panel is deluminated. To illuminate the LCD panel after returning from stop mode, set the LCD enable bit to “1”.

3. When “1” (on-chip oscillator divide-by-4) is set by the watchdog timer count source selection bit 2, the on-chip oscillator forcibly oscillates and cannot be stopped. At this time, set the STP instruction function selection bit (bit 6 in the watchdog timer control register (address 0029_{16})) to “1” (an internal reset occurs when the STP instruction is executed).

3.2 Wait Mode

The MCU enters wait mode when the WIT instruction is executed. In wait mode, oscillation continues but the system clock ϕ stops "H". The CPU stops, but the peripheral functions are active.

3.2.1 Status in Wait Mode

Table 3.2 lists the Status in Wait Mode.

Table 3.2 Status in Wait Mode

Item	State in Wait Mode
Oscillation	Active (oscillation continues)
On-chip oscillator	Active (oscillation continues) Stopped when the WIT instruction is executed in low-speed mode.(1)
CPU	Stopped
System clock ϕ	Stopped "H"
I/O ports P0 to P6	Hold the input state or output level when the WIT instruction is executed.
Timers	Active
LCD drive control circuit	Active
Watchdog timer	Active
Serial I/O1 and serial I/O2	Active
A/D converter	Active
RAM	Held
CPU register and SFR	Held(2)

NOTES:
1. For the QzROM version of this MCU, the on-chip oscillator stops in low-speed mode. For the flash memory version of this MCU, set the on-chip oscillator to stop in low-speed mode. When using the watchdog timer, set the watchdog timer count source selection bit 2 to "0" (ϕSOURCE).
2. Some SFRs may be changed depending on peripheral function operations (AD conversion completion bit, receive buffer full flag, etc.). The SFRs are initialized when the MCU returns by the reset input.

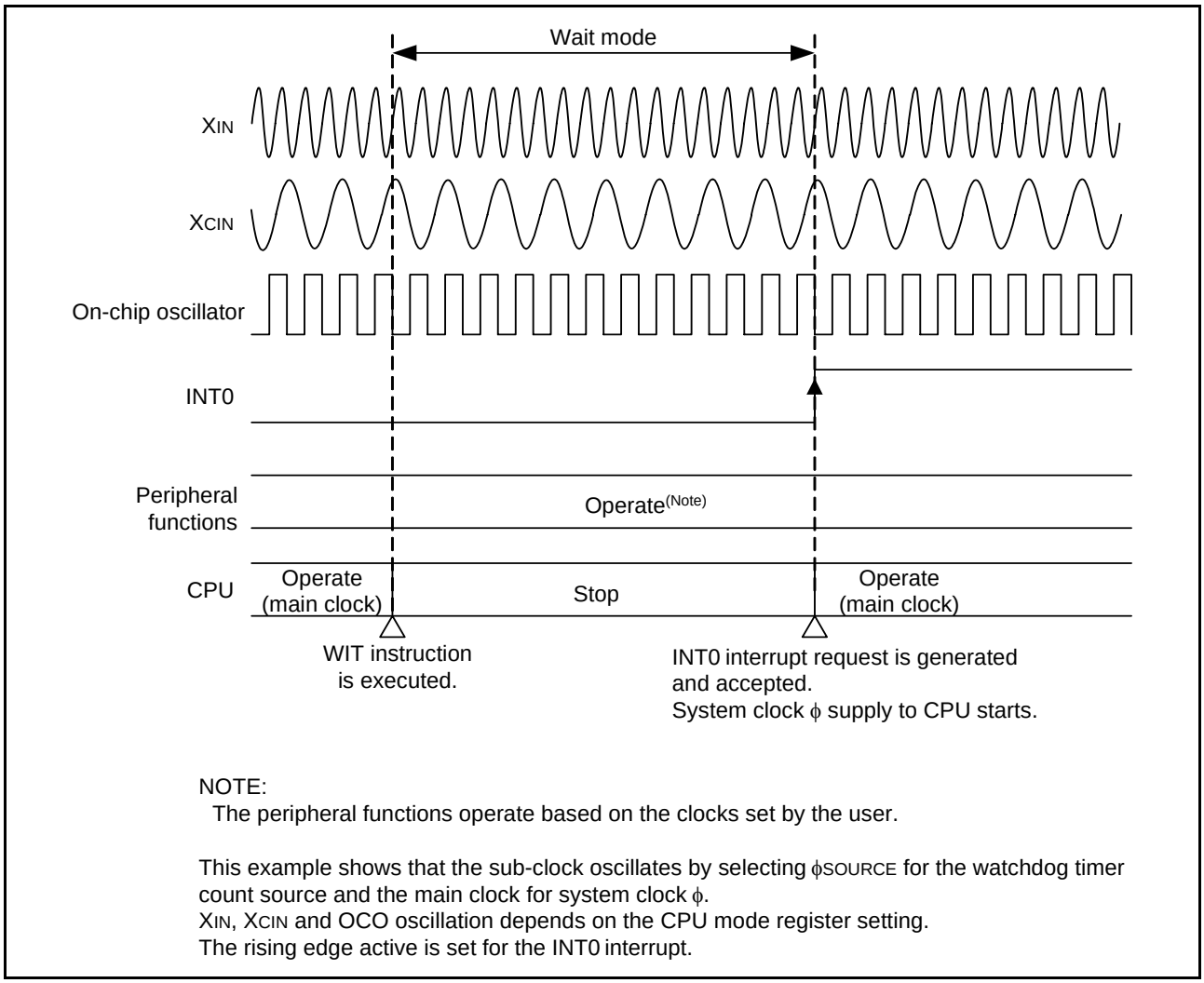
3.2.2 Exiting Wait Mode

To exit wait mode, generate an enabled interrupt request or input a reset. The MCU's return from wait mode differs between the interrupt request being generated and a reset being input.

- Return by interrupt

If an enabled interrupt request is generated during wait mode(1), wait mode is exited and the system clock ϕ supply to the CPU starts. The generated interrupt request is accepted and its interrupt routine is executed. The watchdog timer is active in wait mode. Write to the watchdog timer control register to prevent underflow. Figure 3.3 shows an Operation When Returning from Wait Mode Using a Generated INT0 Interrupt Request.

NOTE:
All interrupt sources can be used for returning from wait mode. Enable an interrupt and execute the WIT instruction.



NOTE:
The peripheral functions operate based on the clocks set by the user.

This example shows that the sub-clock oscillates by selecting ϕSOURCE for the watchdog timer count source and the main clock for system clock ϕ.
XIN, XCIN and OCO oscillation depends on the CPU mode register setting.
The rising edge active is set for the INT0 interrupt.

Figure 3.3 Operation When Returning from Wait Mode Using a Generated INT0 Interrupt Request

- Return by reset input
  To exit wait mode, the input level to the $\overline{\text{RESET}}$ pin must be “L”. All I/O ports are changed to in input mode, and sub-clock oscillation stops and on-chip oscillator (when the OSCSEL pin is “L”) oscillation or the main clock (XIN-XOUT)(when the OSCSEL pin is “H”) oscillation starts. On-chip oscillator mode (when the OSCSEL pin is “L”) or divide-by-8 mode (when the OSCSEL pin is “H”) is selected for the system clock. If the main clock oscillates when the WIT instruction is executed, oscillation continues. An internal reset occurs when the $\overline{\text{RESET}}$ pin is held “L” for 2 μs or more and the MCU operates according to the reset sequence. If the main clock stops when the WIT instruction is executed, time for oscillation to stabilize when oscillation starts is necessary. Hold the $\overline{\text{RESET}}$ pin input level “L” until oscillation is stable. And an internal reset occurs when the $\overline{\text{RESET}}$ pin is held “L” for 2 μs or more and the MCU operates according to the reset sequence. Refer to the 38D2 application note Reset Circuit for the reset sequence.

3.2.3 Notes on Wait Mode

- Return by reset input
  When the WIT instruction is executed, the sub-clock is selected for the system clock and the main clock stops, sub-clock oscillation stops and on-chip oscillator (when the OSCSEL pin is “L”) oscillation or main clock (XIN-XOUT)(when the OSCSEL pin is “H”) oscillation starts by applying “L” input level for the $\overline{\text{RESET}}$ pin. Oscillation is unstable when it starts, and a certain amount of time is necessary for oscillation to stabilize. Hold the $\overline{\text{RESET}}$ pin input level “L” until oscillation is stable. An internal reset occurs when oscillation is stable and the $\overline{\text{RESET}}$ pin is held at an “L” level for 2 μs or more.

- In low-speed mode, the on-chip oscillator stops in the QzROM version. In low-speed mode, stop the on-chip oscillator by a program for the flash memory version. When using the watchdog timer, set the watchdog timer count source selection bit 2 to “0” (φSOURCE).

4. Reference Document

Datasheet
38D2 Group Datasheet
Use the most recent version of the document on the Renesas Technology Web site.

Technical News/Technical Update
Use the most recent version of the document on the Renesas Technology Web site.

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