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38C2 Group

Timer X Operation (IGBT Output Mode:Output of IGBT Control Signal)

1. Abstract

The following document describes examples how to set the timer X and application examples in the 38C2 Group.

2. Introduction

The application examples described in this document are applied to the following MCU and conditions:

- Applicable MCU: 38C2 Group A Version
- Oscillation frequency: 8 MHz

In this sample program, the bit of the function which is not used may be operated according to the bit assignment of SFR. Please set these values according to the use status of a user system.

3. Description of IGBT Control Signal Output

3.1 Outline of IGBT Output Mode

The 38C2 Group has the IGBT output mode as a function of timer X (16-bit timer).
In IGBT output mode, IGBT control signal is output from the T_{XOUT} pin by the count value of timer X. Period and duty ratio of IGBT control signal are fixed by timer X and the compare register when a trigger is not input from the INT_0 pin. Period is determinate.
Period and duty ratio of IGBT control signal are fixed by timer X, the compare register, and trigger input from the INT_0 pin when the trigger is input from the INT_0 pin. Period is variable.

Operation when setting the timer X output polarity switch bit (bit 5 in the timer X control register ($0FF4_{16}$)) to "0" and "Start from "L" output" is selected is described. When a trigger is input from the INT_0 pin or timer X underflows after the timer X count starts, the T_{XOUT} pin outputs "H"(1) ("L"(1) is output for the first period until the trigger is input from the INT_0 pin, or timer X underflows.) When the count value of timer X matches with the value of the compare register, the T_{XOUT} pin outputs "L"(1). Trigger input from the INT_0 pin is valid while the T_{XOUT} pin outputs "L"(1). The following selections are available regarding the trigger input:

- Falling edge active or rising edge active
- Sampling clock of noise filter (determined as valid signal if signal levels are the same four times continuously with the sampling clock.)
- Four types of delay time

To set the timer X output control bit 1 or 2 (bit 3 or 4 in the timer X control register) to "1", the timer X count stop bit (bit 6 in the timer X mode register ($002F_{16}$)) is set to "1" by input of the INT_1 or INT_2. Then the timer X count stops and output from the T_{XOUT} pin can be held "L"(1). The falling edge active or rising edge active can be selected for input of the INT_1 or INT_2 pin.

The previous setting value is valid for the value of the compare register until trigger input from the INT_0 pin or underflow of timer X after the timer X count starts. However, "L"(1) is output for the first period regardless of the setting value of the compare register after the timer X count starts.

To use the IGBT output mode, note the following:
(Refer to 4. Notes on Timer X (IGBT Output Mode).)

- Set the port direction register shared with the INT_0 pin to input mode and the port direction register shared with the T_{XOUT} pin to output mode.
- To use the T_{XOUT} pin by switching it with the port output, the port latch value may be changed by the read-modify-write instruction.
- Since the port ($P3_5$) shared with the T_{XOUT} pin functions as input at reset, stabilize the level by the external pull-down resistor or pull-up resistor.
- Set the timer X register (extension) to "00_{16}"

NOTE:
1. When the timer X output polarity switch bit is set to "1", the level is inverted.

3.2 Output IGBT Control Signal

Outline:

- IGBT control signal of 20μs period with 5μs for "H" duration is output (IGBT active level is "H") and start from "L" output.
- When trigger signal ("H" to "L") is input to the INT_0 pin during "L" output, the output level is "H" and timer X restarts from the setting value of the timer X latch.

Specifications:

- Select f(X_{IN}) = 8 MHz (1 count 125 ns) for the timer X count source.
- The timer X initial value is set to 159 and the timer X underflow period is set to 20 μs.
- The setting value of the compare register is set to 120. When trigger signal from the INT_0 pin is not input, "L" duration is set to 15 μs. Therefore, "H" duration is set to 5 μs.
- Select f(X_{IN})/2 for the noise filter sampling clock. Select "not delayed" for external trigger delay time.
- Select falling edge active for INT_0 input signal.

Figure 3.1 shows the Timer Connection and Setting of Division Ratio; Figure 3.2 shows the TXOUT Output Waveform; Figure 3.3 shows the Setting of Related Registers (1); Figure 3.4 shows the Setting of Related Registers (2) and Figure 3.5 shows the Control Procedure.

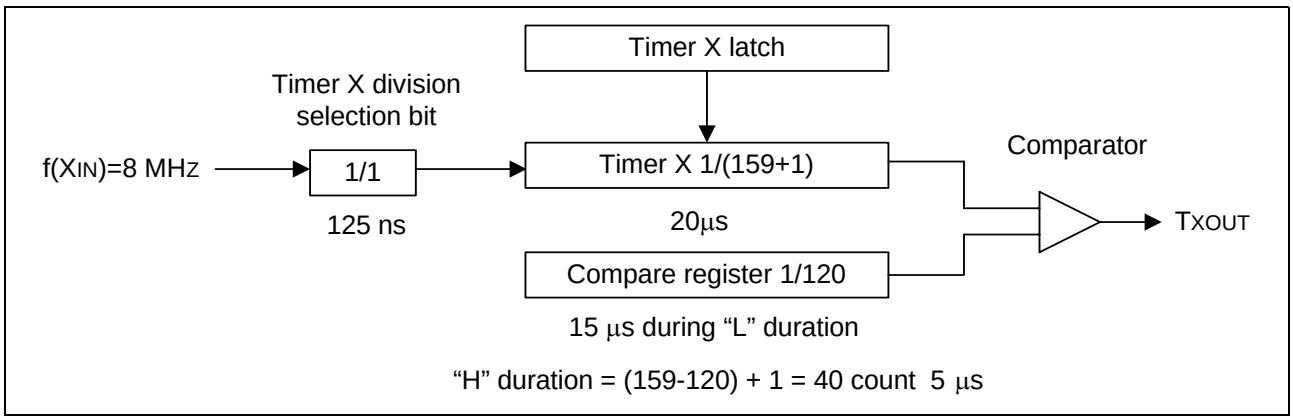


Figure 3.1 Timer Connection and Setting of Division Ratio

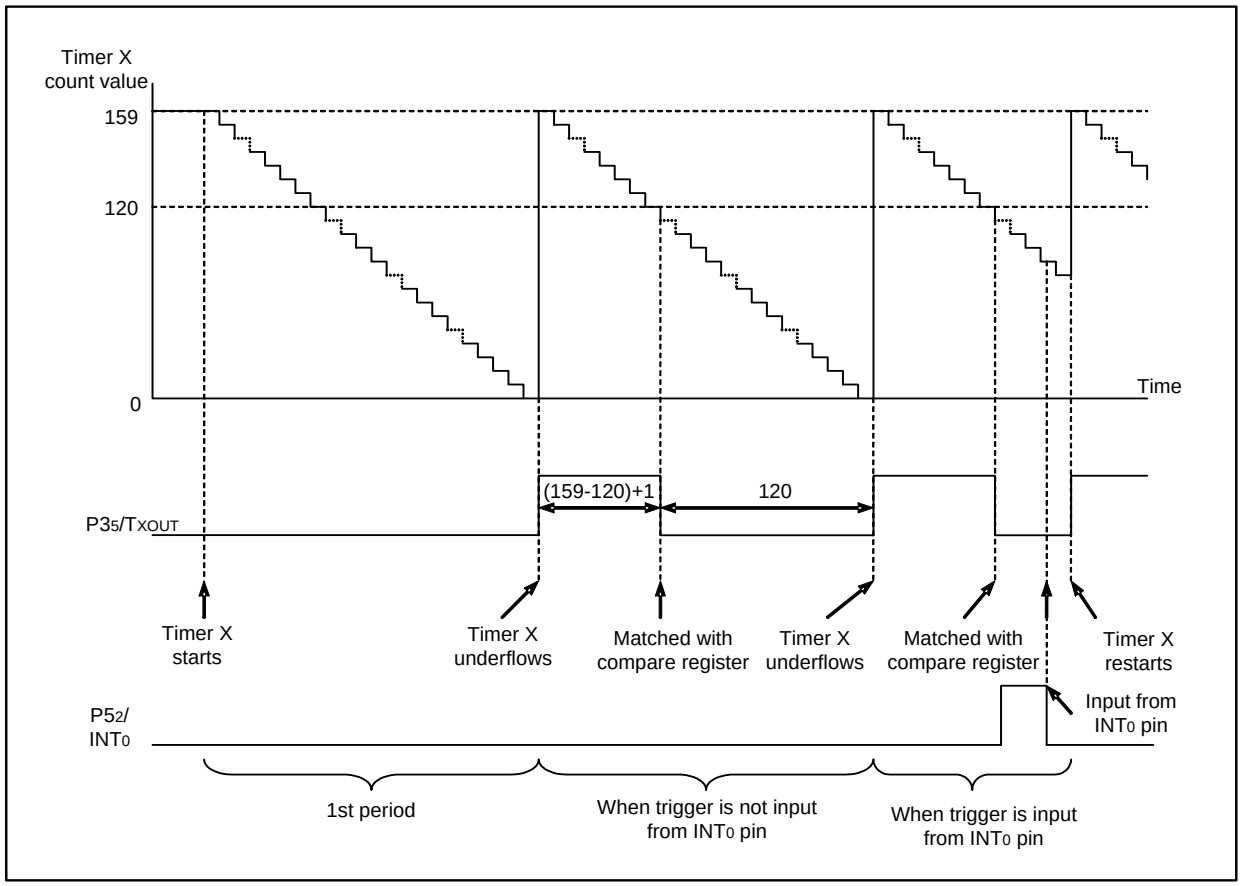
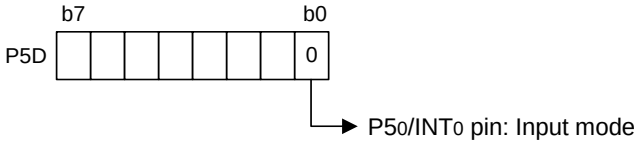
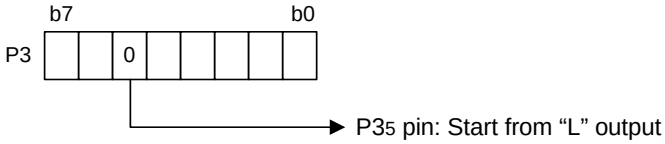


Figure 3.2 TXOUT Output Waveform

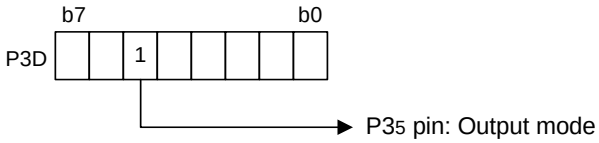
Port P5 Direction Register (000B16)



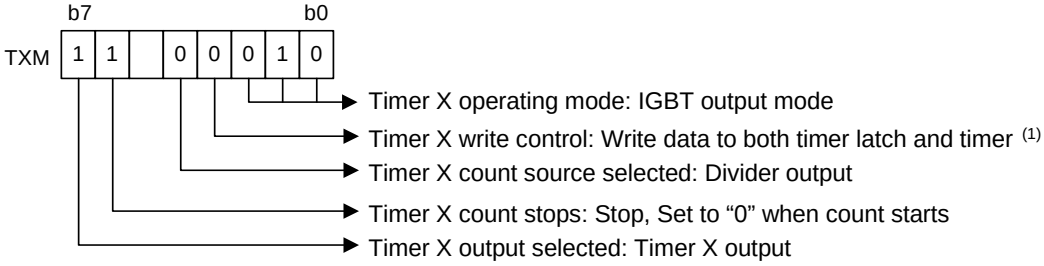
Port P3 Register (000616)



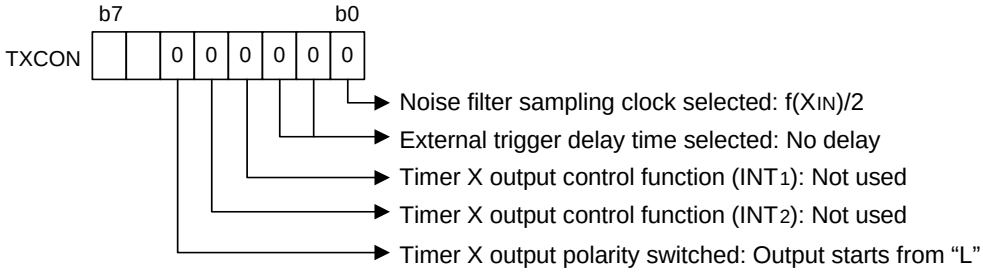
Port P3 Direction Register (000716)



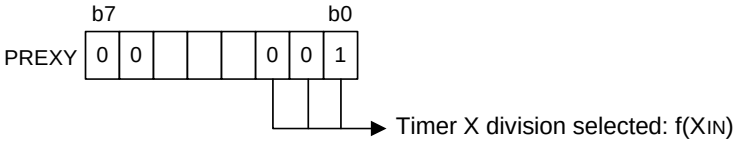
Timer X Mode Register (002F16)



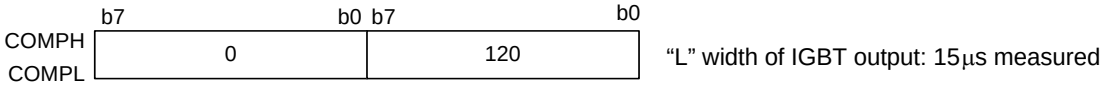
Timer X Control Register (0FF416)



Timer XY Division Selection Register (0FF716)



Compare Register (high-order) (002916)
Compare Register (low-order) (002816)



NOTE:
1. Write data to timer latch only after setting the value to the compare register and timer X.

Figure 3.3 Setting of Related Registers (1)

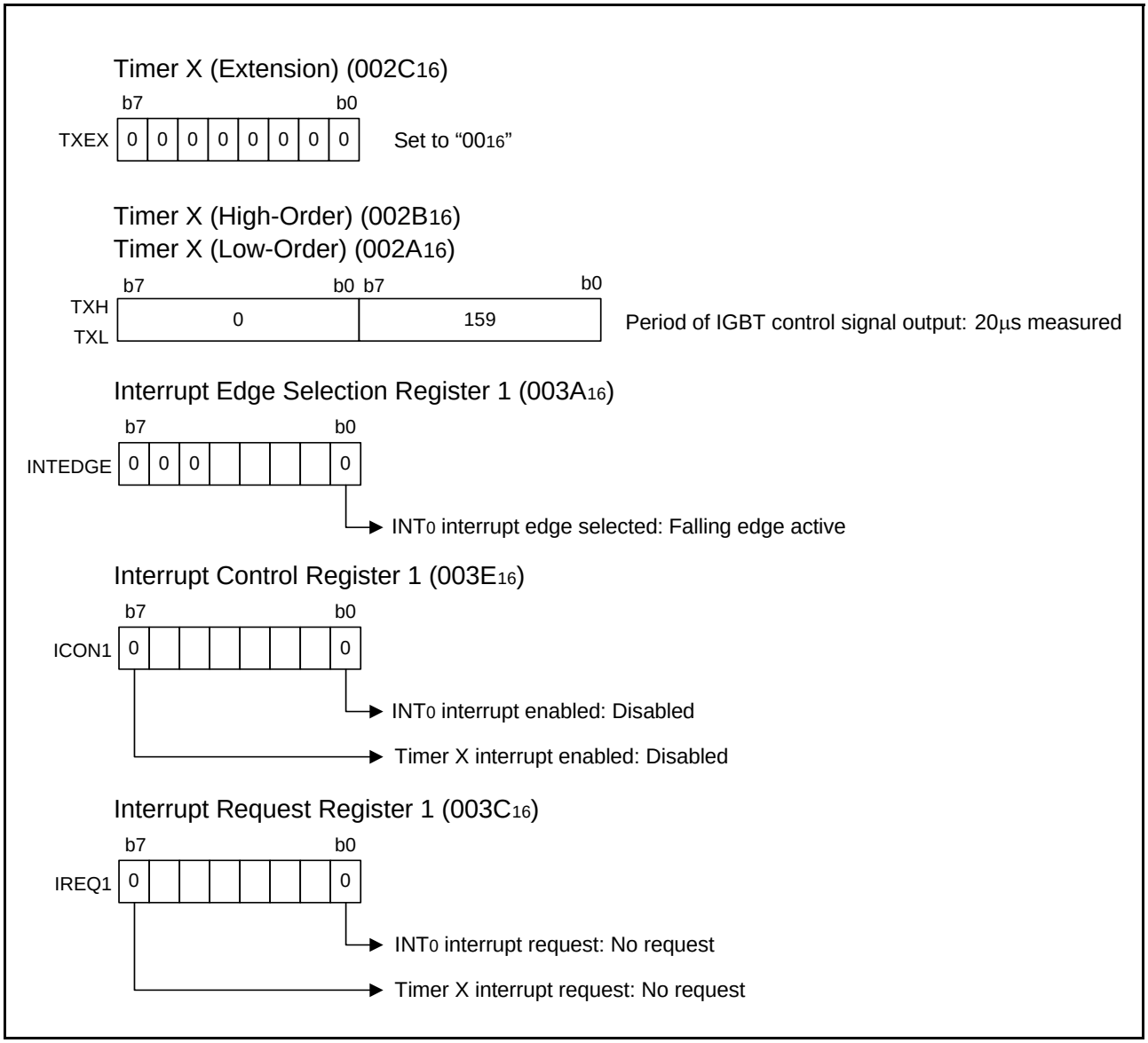


Figure 3.4 Setting of Related Registers (2)

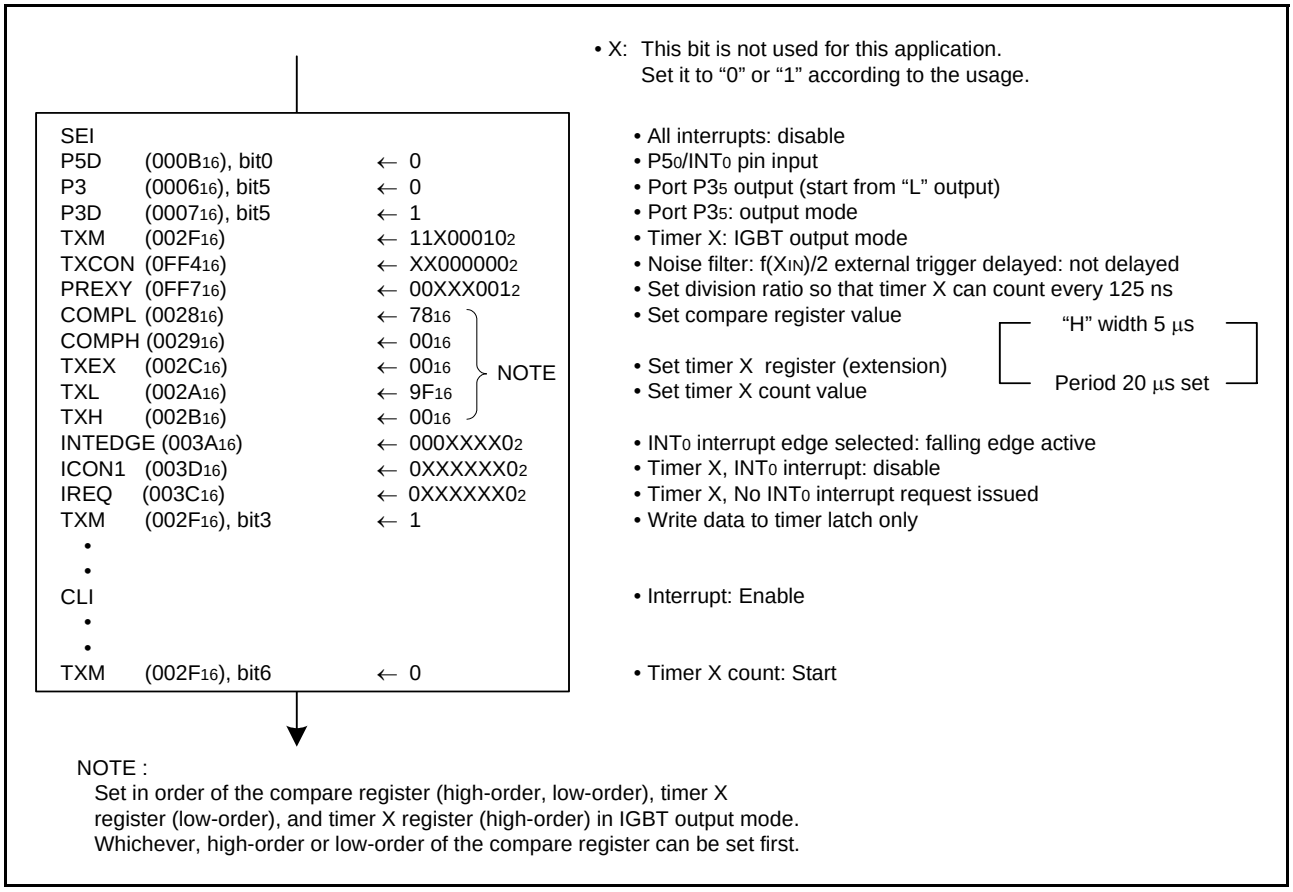


Figure 3.5 Control Procedure

4. Notes on Timer X (IGBT Output Mode)

(1) Write order to timer X

- In IGBT output mode, do not write "1" to the timer X register (extension). When "1" is already written to the timer X register (extension), ensure to write "0" to the register before using. Write in order of the compare register (high order, low order), timer X register (extension), timer X register (low order), and timer X register (high order). Whichever, high order or low order of the compare register can be set first . Write data to both the high order and low order for the compare register and timer X register.

(2) Read order to timer X

- In all modes, read in order of the timer X register (extension), timer X register (high-order), and timer X register (low-order). When reading the timer X register (extension) is not required, read in order of the timer X register (high-order) first and the timer X register (low-order). Read order to the compare register is not specified.
- Write and read operations of the timer X register should be performed in 16-bit units. If write or read operation is stopped, normal operation will not be performed.

(3) Write to timer X

- Which write control can be selected by the timer X write control bit (b3) of the timer X mode register (address $002F_{16}$), writing data to both the latch and the timer at the same time or wiritng data only to the latch. When writing a value to the timer X address to write to the latch only, the value is set into the timer latch and the timer is updated at the next underflow. Because writing to the timer and timer latch at the same time is set after reset, a value is set to the timer and timer latch at the same time when the value is written to the timer X address. When writing to the latch only, if the write timing to the high-order timer latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting may be stopped during write operation to the high-order timer latch (refer to 5.Notes on Timer Count Stop of Writing Data to Timer Latch Only).
- Do not switch the timer count source during timer count operation. Stop the timer count before switching it.

(4) Set of timer X mode register

- Set the write control bit of the timer X mode register to "1" (write to the latch only) in IGBT output mode.

(5) Timer X output control function

- When using the timer X output control function (INT_1 or INT_2) in IGBT output mode, set the INT_1 or INT_2 level to "H" in the falling edge active or to "L" in the rising edge active before switching to IGBT output mode.

(6) Port $P3_5$ latch

- When the waveform from the T_{XOUT} pin is output and the port P3 is read in IGBT output mode, the pin state (level) is read. At this time, when the read-modify-write instructions are executed, the pin state (level) is reflected to the port latch and the value of bit 5 may be changed. Then when the P35/TXOUT pin is switched to the I/O port (output mode) from the timer X output, the unexpected level may be output by the changed value. Switch the I/O port after setting a given value to the port latch.

  Read-modify-write instruction: Read one-byte of data from memory (read), modify the data (modify), write the data back to original memory (write).
  CLB, SEB, ASL, LSR, ROL, ROR, RRF, DEC, INC, COM

(7) When 0000_{16} is set to the compare register (previous value: other than 0000_{16})

"H" signal is output for one period at the next period after writing to timer X or the compare register. And "L" signal is output while timer X counts $3FFFF_{16}$. After that, this operation will be repeated. (The timer X output polarity switch bit is set to "0": start from "L" output and INT0 trigger is not input.)

Figure 4.1 shows an Example of IGBT Control Signal when 0000_{16} is Set to Compare Register (Previous Value: Other than 0000_{16}).

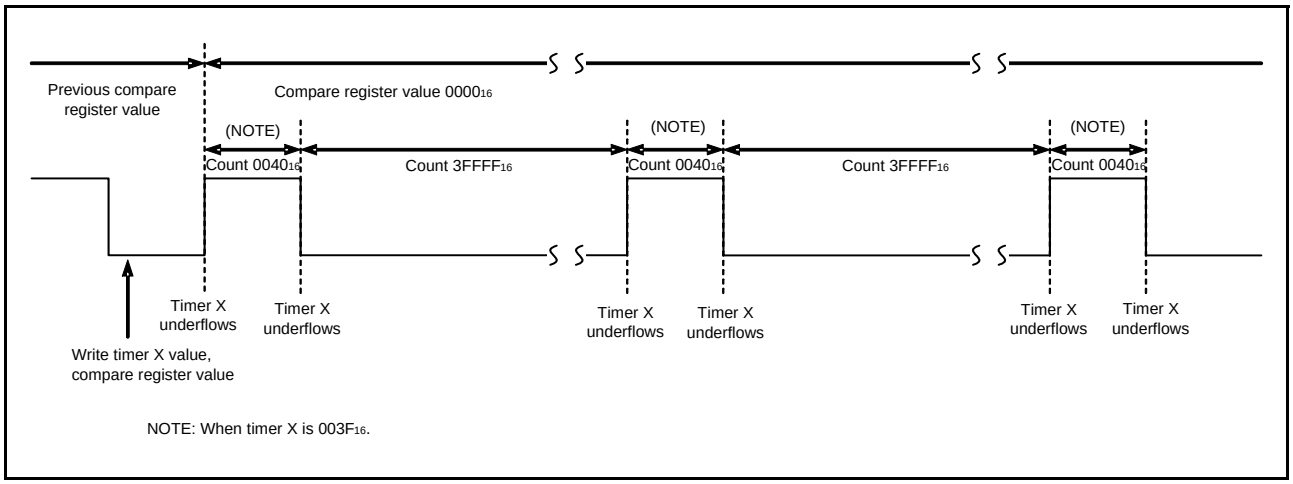


Figure 4.1 Example of IGBT Control Signal Output when 0000_{16} is Set to Compare Register (Previous Value: Other than 0000_{16})

(8) When same value is set to timer X and compare register

TXOUT output is held "H" at the timing of underflow immediately after writing to timer X and the compare register. Then TXOUT output is held "L" when the timer X value is reloaded and matches with the compare register value. The width of "H" output is assumed as 1 count of the timer X count source (the timer X output polarity switch bit is set to "0": start from "L" output and INT0 trigger is not input).

Figure 4.2 shows an Example of IGBT Control Signal Output when Same Value is Set to Timer X and Compare Register.

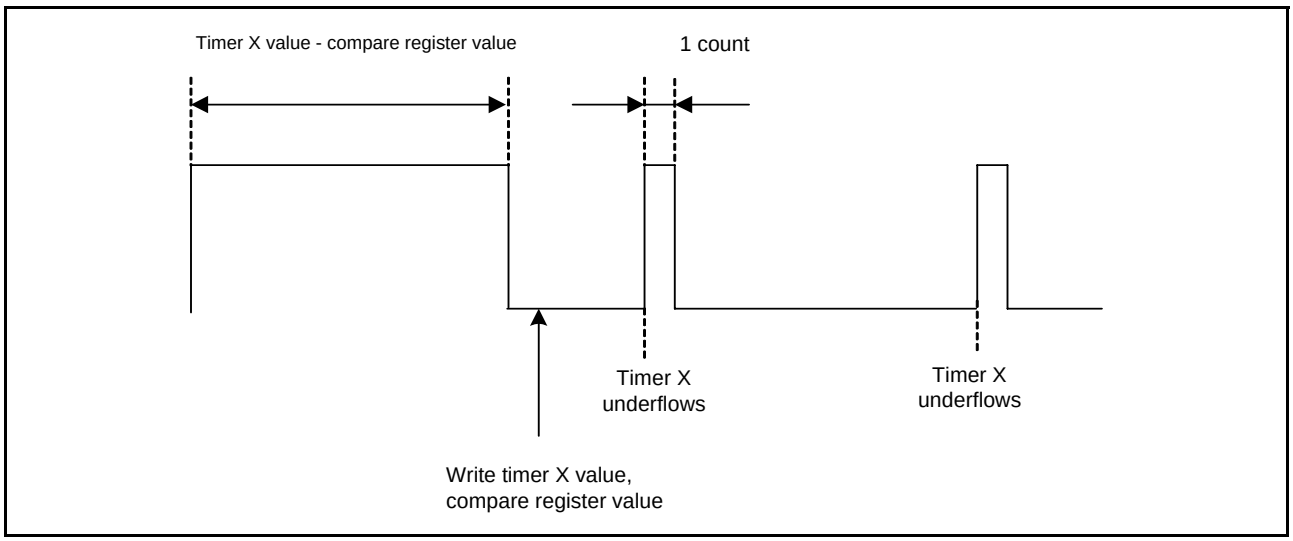


Figure 4.2 Example of IGBT Control Signal Output when Same Value is Set to Timer X and Compare Register

(9) Time between trigger input to INT0 pin and invert of TXOUT output waveform polarity

In IGBT output mode, a trigger input from the INT0 pin is valid only while the opposite polarity level from the active level is output (if the IGBT active level is "H", the trigger input is valid only while the TXOUT output level is held "L"). The TXOUT output level is switched to the active level by the valid trigger input of the INT0 pin (if the IGBT active level is "H", the TXOUT output level is switched to "H"). Time difference is generated by level determined time with a noise filter (determined as four times matches continuously) and delay time with the delay circuit between the input valid edge of the INT0 signal and the polarity invert to the active level. The noise filter sampling clock can be selected by the noise filter sampling clock selection bit (bit 0 of the timer X control register). Delay time with the delay circuit can be set by the external trigger delay time selection bits (bit 2, 1 of the timer X control register).

Figure 4.3 shows an example of IGBT control signal output when INTO input is falling edge active and IGBT active level is "H".

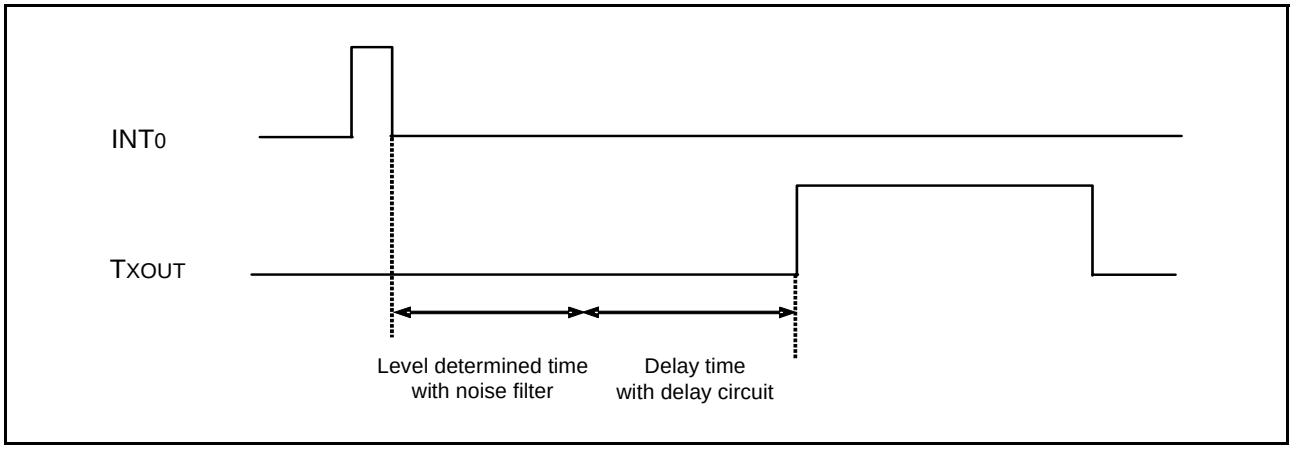


Figure 4.3 Example of IGBT Control Signal Output of TXOUT Pin by Trigger Input to INT0 Pin

5. Notes on Timer Count Stop of Writing Data to Timer Latch Only

When writing to the latch only, if the write timing to the timer latch and the underflow timing are the same time, the timer count operates as follows:

- Timer count source ≤ internal system clock ϕ
  Timer count operation does not stop and starts counting with new timer value.

- Timer count source > internal system clock ϕ
  Timer count operation stops for up to one cycle of the system clock. When write operation (internal system clock ϕ) is completed, count starts with the new timer value.

  NOTE:
  Timer latch for timer 2, 3, or 4. High-order timer latch for timer X or Y.

6. Reference Program

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7. Reference Document

Datasheet
38C2 Group (A version) Datasheet
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Technical News/Technical Update
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REVISION HISTORY	38C2 Group Timer X Operation (IGBT Output Mode:Output of IGBT Control Signal)

Rev.	Date	Description	
		Page	Summary
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