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38C2 Group

Serial I/O 1, 2 (Clock Synchronous Serial I/O Mode: Example-2)

1. Abstract

The following article introduces and shows an example of how to use the Serial I/O1 (Clock Synchronous Serial I/O Mode: Example-2) on the 38C2 group device.
In serial I/O2, it can be used similarly.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: 38C2 Group
Oscillation frequency: 4MHz

Set transfer speed within the timing requirements and switching characteristics of data sheet.

In this sample program, the bit of the function which is not used may be operated on account of bit arrangement of SFR. Please set these setting values according to the use situation of a user system.

3. Contents

3.1 Cyclic Transmission or Reception of Block Data (Data of Specified Number of Bytes) Between Two Microcomputers

Outline: When the clock synchronous serial I/O is used for communication, synchronization of the clock and the data between the transmitting and receiving sides may be lost because of noise included in the synchronous clock. It is necessary to correct that constantly, using “heading adjustment”.
This “heading adjustment” is carried out by using the interval between blocks in this example.

Specifications:

- Serial I/O1 is used (clock synchronous serial I/O is selected.)
- Synchronous clock frequency: 125kHz ($f(X_{IN})$=4MHz divided by 32)
- Byte cycle: 500μs
- Number of bytes for transmission or reception: 8 bytes/block
- Block transfer cycle: 16ms
- Block transfer term: 4ms
- Interval between blocks: 12ms
- Heading adjustment time: 8ms

Master side control

- Data is transmitted and received by interrupt routine executed every byte cycle (500μs).

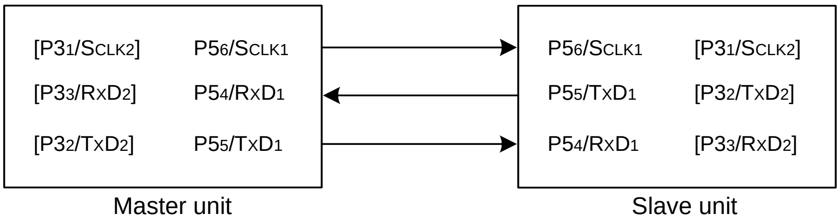
Slave side control

- Data is transmitted and received by serial I/O1 receive interrupt routine.
- The heading adjustment is carried out by interrupt routine executed every 1ms.

Limitation of specification:

- Reading of the reception data and writing of the next transmission data must be completed within the time obtained from “byte cycle - time for transferring 1-byte data” (in this example, the time taken from generating of the serial I/O1 receive interrupt request to input of the next synchronous clock is 436μs).
- “Heading adjustment time < interval between blocks” must be satisfied.

Figure 3.1 shows the Connection Diagram.



Note: In the serial I/O2, the pin in [ ] corresponds.

Figure 3.1 Connection Diagram

Figure 3.2 shows the Timing Chart. In the slave unit, when a synchronous clock is not input within a certain time (heading adjustment time), the next clock input is processed as the beginning (heading) of a block. When a clock is input again after one block (8 bytes) is received, the clock is ignored.
Figure 3.3 shows the Relevant Registers Setting.

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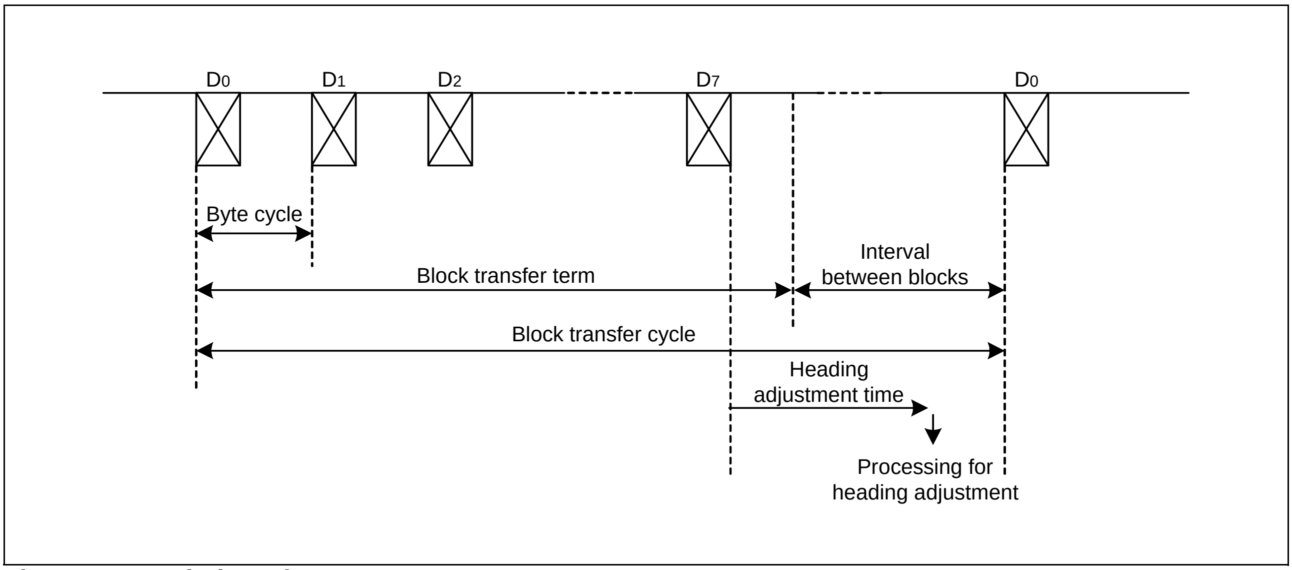

Figure 3.2 Timing Chart

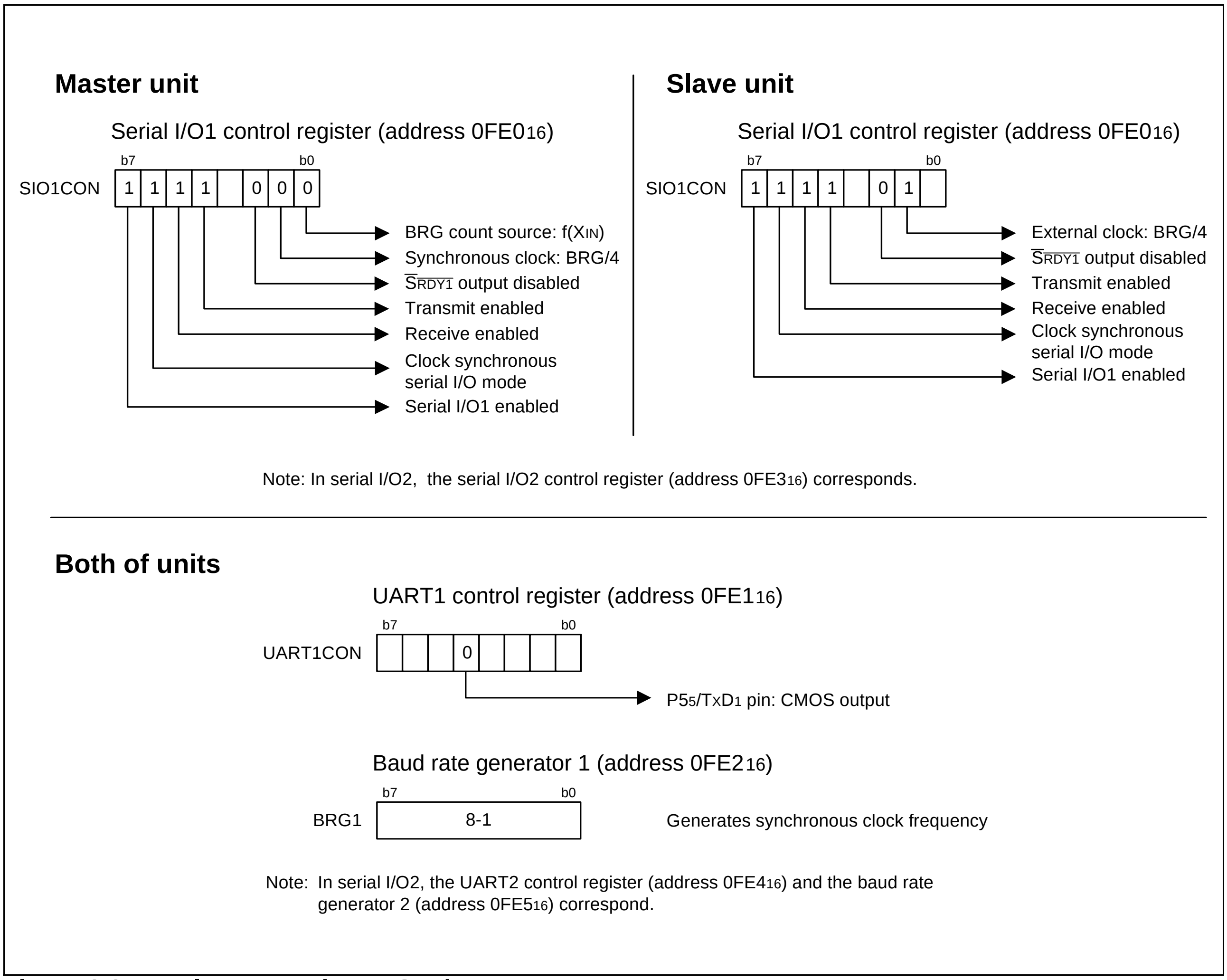

Figure 3.3 Relevant Registers Setting

Control by software:

• Control in the master unit

The master unit starts transmission or reception by writing transmission data to the transmit buffer register in the interrupt routine executed every 500µs. In this interrupt routine, read the reception data before the next transmission data is written to the transmit buffer register. Additionally, transmission and reception of one block (8 bytes) is controlled and the block interval is generated.

Figure 3.4 shows the Control Procedure of Master Unit.

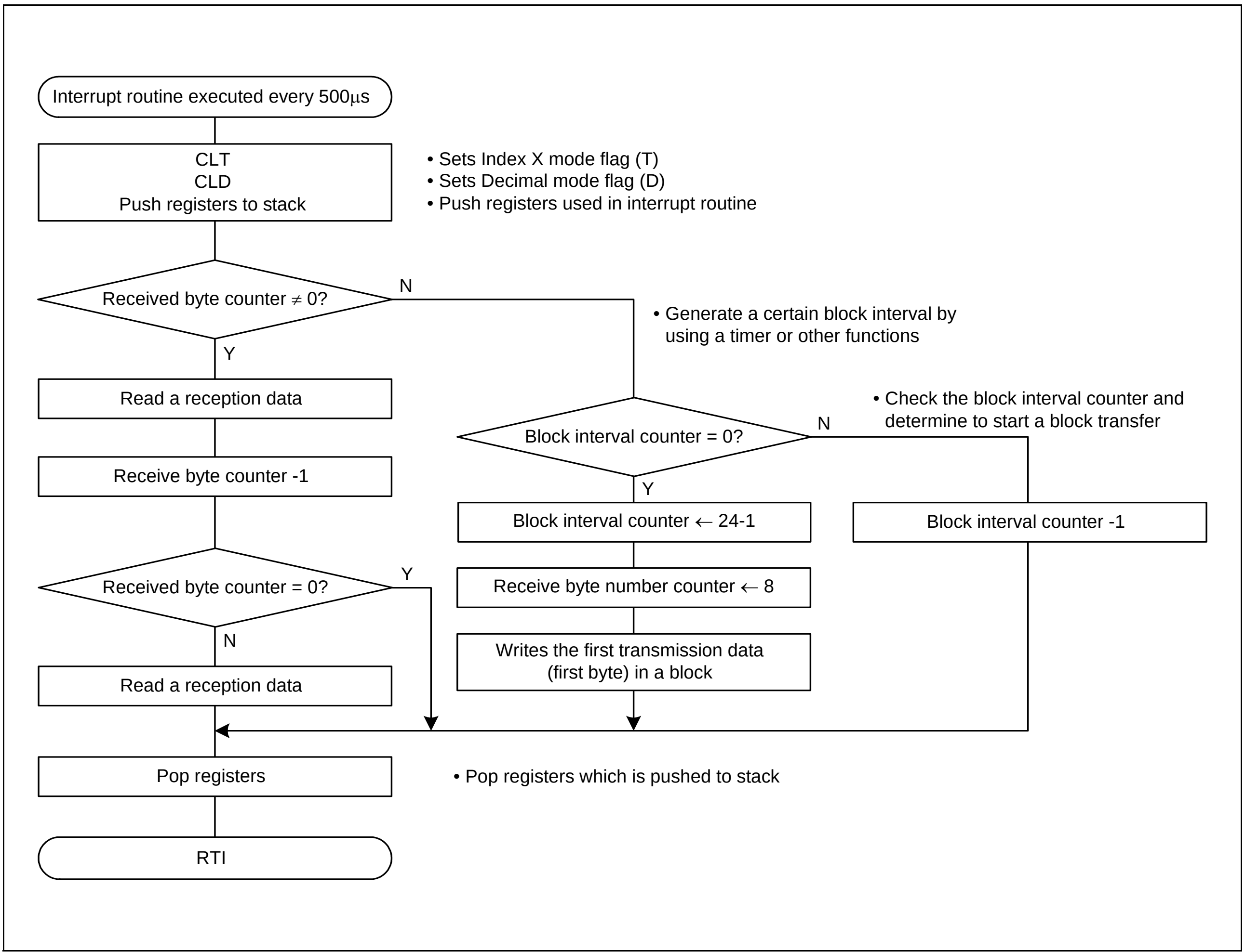

Figure 3.4 Control Procedure of Master Unit

Control by software:

- Control in the slave unit

After setting the relevant registers as shown in figure 3.3, the slave unit becomes the state where a synchronous clock can be received at any time, and the serial I/O1 receive interrupt request occurs each time an 8-bit data is received. In the serial I/O1 receive interrupt routine, the data to be transmitted next is written to the transmit buffer register after the received data is read out.

However, if no serial I/O1 receive interrupt occurs for a certain time (heading adjustment time or more), the following processing will be performed in the interrupt routine executed every 1ms.

1. Serial I/O1 is initialized.
2. The first 1-byte data of the transmission data in the block is written into the transmit buffer register.
3. Since the data to be received next is processed as the first 1 byte of the received data in the block, the receive byte counter is initialized.

Figure 3.5 shows the Control Procedure of Slave Unit.

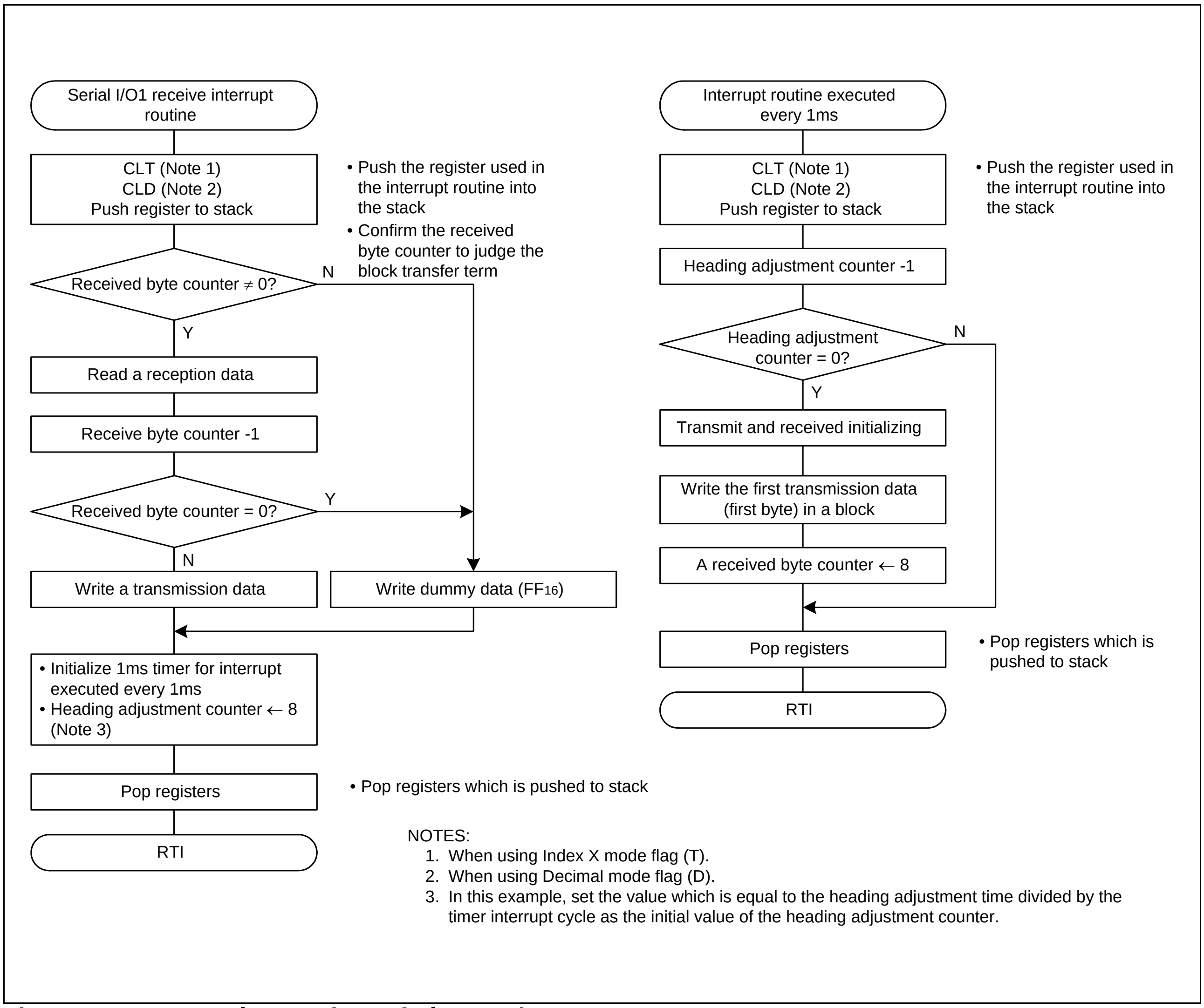

Figure 3.5 Control Procedure of Slave Unit

4. Sample Programming Code

```
Master unit
[Setting of control register]
    LDA UART1CON              ;Set TXD CMOS-OUT
    AND #%11101111
    STA UART1CON
    LDM #%01100000,P5         ;Set Port P5 register
    LDM #%01100000,P5D        ;Set Port P5 direction register
;
    LDA #%00000000            ;Set Serial I/O1 control register
    STA SIO1CON
    LDA #8-1                  ;Set Baud rate generator1
    STA BRG1
    LDA #%11110000            ;Set Serial I/O1 control register
    STA SIO1CON
;
    LDM #%00000000,T12M       ;Set Timer 12 mode register
    LDA #%00000000            ;Set Timer 12 frequency division selection
    STA PRE12
    LDA #%00000000            ;Set Timer 1234 mode register
    STA T1234M
    LDM #125-1,T1             ;Set Timer 1
;       ;
    CLB 0,IREQ2               ;Timer1 interrupt request clear
    SEB 0,ICON2               ;Timer1 interrupt enable
;
    CLI                       ;Interrupt enable
;
```

```
Master unit
[Timer 1 interrupt routine processing]
__TIMER1:
    CLT
    CLD
    PHA
    TXA
    PHA
;
    LDA RECV_BYTE
    CMP #$0                 ;Receive byte zero ?
    BEQ __TIMER1_10         ;-> no
;
    LDX RECV_BYTE
    LDA RB1
    STA RECV_DATA-1,X       ;Receive data read
;
    DEC RECV_BYTE           ;Receive byte dec
    LDA RECV_BYTE
    CMP #$0                 ;Receive byte zero ?
    BEQ __TIMER1_00         ;-> yes
    LDX RECV_BYTE
    LDA SEND_DATA_TBL-1,X
    STA TB1                 ;Send data write
    BRA __TIMER1_00
;
__TIMER1_10:
    LDA BLOCK_SPACE
    CMP #$0                 ;Block space zero ?
    BNE __TIMER1_11         ;-> no
    LDM #24-1,BLOCK_SPACE   ;Block space counter set
    LDM #8,RECV_BYTE        ;Receive byte counter set
    LDX RECV_BYTE
    LDA SEND_DATA_TBL-1,X
    STA TB1                 ;Send data write
    BRA __TIMER1_00
;
__TIMER1_11:
    DEC BLOCK_SPACE         ;Block space dec
;
__TIMER1_00:
    PLA
    TAX
    PLA
    RTI
;
```

```
Slave unit
[Setting of control register]
    LDA UART1CON                ;Set TXD CMOS-OUT
    AND #%11101111
    STA UART1CON
    LDM #%10000000,P5           ;Set Port P5 register
    LDM #%10000000,P5D          ;Set Port P5 direction register
;
    LDA #%00000000              ;Set Serial I/O1 control register
    STA SIO1CON
    LDA #%11110010              ;Set Serial I/O1 control register
    STA SIO1CON
;
    LDM #%00000000,T12M         ;Set Timer 12 mode register
    LDA #%00000000
    STA PRE12                   ;Set Timer 12 frequency division selection
    LDA #%00000000
    STA T1234M                  ;Set Timer 1234 mode register
    LDM #250-1,T1               ;Set Timer 1

    CLB 0,IREQ2                 ;Timer1 interrupt request clear
    SEB 0,ICON2                 ;Timer1 interrupt enable
    CLB 3,IREQ1                 ;SIO1 interrupt request clear
    SEB 3,ICON1                 ;SIO1 interrupt enable
;
    CLI                         ;Interrupt enable
;

[Timer 1 interrupt routine processing]
__TIMER1:
    CLT
    CLD
    PHA
    TXA
    PHA
;
    DEC SERIAL_HEAD
    LDA SERIAL_HEAD
    CMP #$0
    BNE __TIMER1_00
;
    LDM #%00000000,SIO1CON      ;Set Serial I/O1 control register
    LDM #%11110010,SIO1CON      ;Set Serial I/O1 control register
    LDX #8
    LDA SEND_DATA_TBL-1,X
    STA TB1                     ;Send data write
    LDM #8,RECV_BYTE            ;Receive byte counter set
;
__TIMER1_00:
    PLA
    TAX
    PLA
    RTI
;
```

```
Slave unit
[Serial I/O receive interrupt routine processing]
__SIO1:
    CLT
    CLD
    PHA
    TXA
    PHA
;
    LDA RECV_BYTE
    CMP #$0                 ;Receive byte zero ?
    BEQ __SIO1_00           ;-> no
;
    LDX RECV_BYTE
    LDA RB1                 ;Receive data read
    STA RECV_DATA-1,X
;
    DEC RECV_BYTE           ;Receive byte dec
    LDA RECV_BYTE
    CMP #$0                 ;Receive byte zero ?
    BEQ __SIO1_00           ;-> yes
    LDX RECV_BYTE
    LDA SEND_DATA_TBL-1,X
    STA TB1                 ;Send data write
    BRA __SIO1_01
;
__SIO1_00:
    LDA #$0FF
    STA TB1                 ;Send dummy data write
;
__SIO1_01:
    LDM #250-1,T1           ;Set Timer 1
    CLB 2,IREQ2             ;Timer1 interrupt request clear
    LDM #8,SERIAL_HEAD      ;Header counter set
;
    PLA
    TAX
    PLA
    RTI
;
```

5. Reference

Renesas Technology Corporation Semiconductor Home Page
http://www.renesas.com

E-mail Support
E-mail: support_apl@renesas.com

Data Sheet
38C2 Group (A version) Data sheet
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