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Renesas Electronics Corporation

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38C2 Group

Serial I/O 1, 2 (Clock Synchronous Serial I/O Mode: Example-1)

1. Abstract

The following article introduces and shows an example of how to use the Serial I/O1 (Clock Synchronous Serial I/O Mode: Example-1) on the 38C2 group device.

In serial I/O2, it can be used similarly.

2. Introduction

The explanation of this issue is applied to the following condition:

Applicable MCU: 38C2 Group

Oscillation frequency: 4MHz

Set transfer speed within the timing requirements and switching characteristics of data sheet.

In this sample program, the bit of the function which is not used may be operated on account of bit arrangement of SFR. Please set these setting values according to the use situation of a user system.

3. Contents

3.1 Communication Using Clock Synchronous Serial I/O (Transmit/Receive)

Outline: 2-byte data is transmitted and received, using the clock synchronous serial I/O.
The $\overline{SRDY1}$ signal is used for communication control.

Specifications:

- Serial I/O1 is used (clock synchronous serial I/O is selected.)
- Synchronous clock frequency: 125kHz ($f(XIN)=4MHz$ is divided by 32)
- $\overline{SRDY1}$ (receivable signal) is used.
- The receiving side outputs $\overline{SRDY1}$ signal at intervals of 2ms (generated by timer), and 2-byte data is received.
- The transmitting side confirms $\overline{SRDY1}$ signal by INT1 interrupt request and transmits 2-byte data.

Figure 3.1 shows the Connection Diagram; Figure 3.2 shows the Timing Chart; Figures 3.3 and 3.4 show the registers setting relevant to the transmitting side; Figure 3.5 shows the Registers Setting Relevant to the Receiving Side; Figure 3.6 shows the Control Procedure of Transmitting Side; Figure 3.7 shows the Control Procedure of Receiving Side.

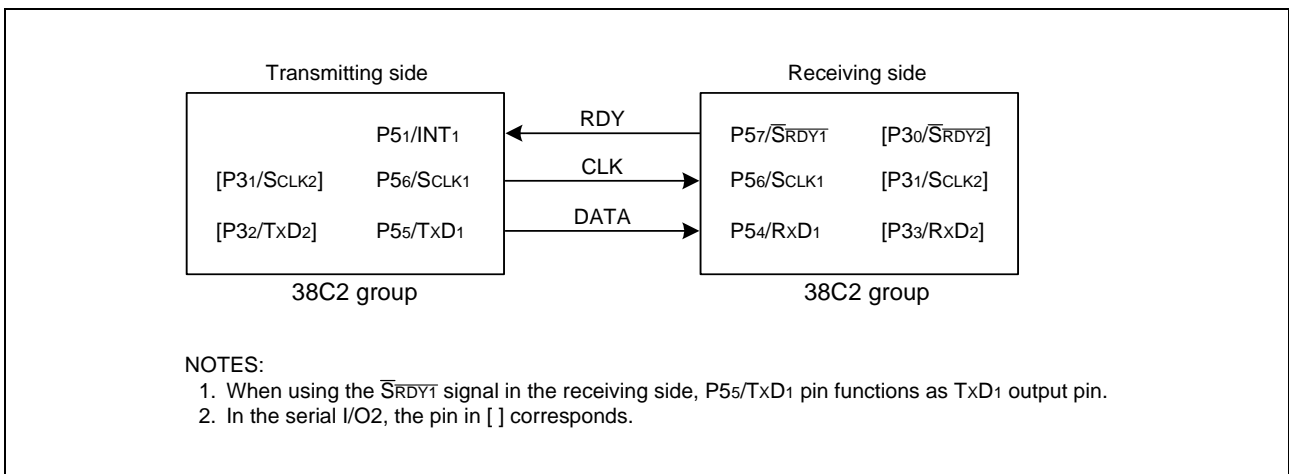


Figure 3.1 Connection Diagram

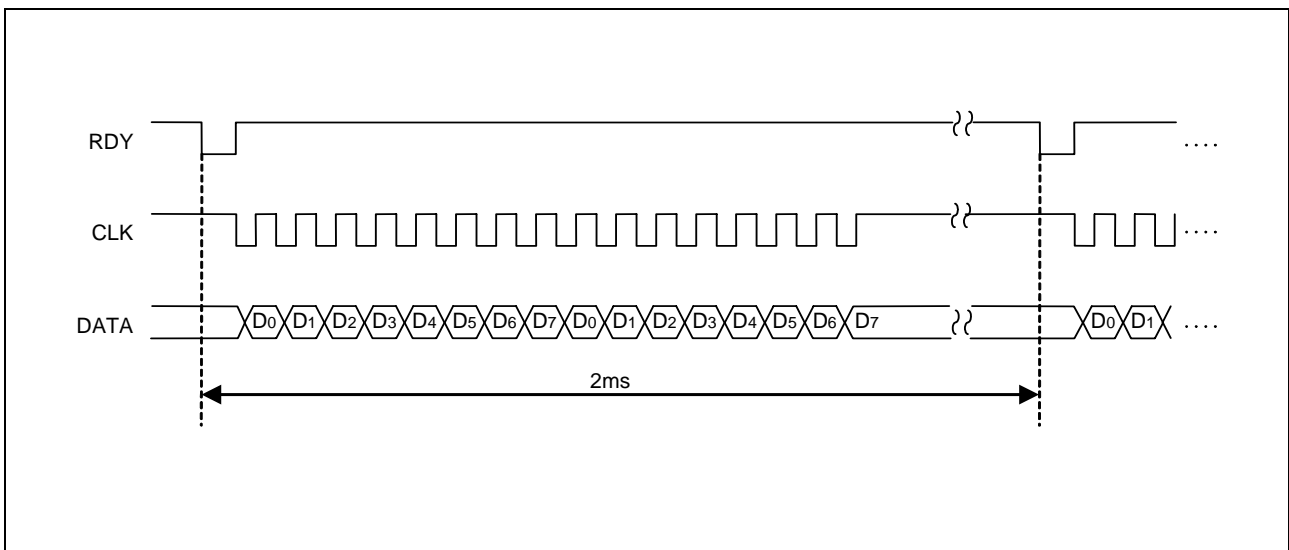


Figure 3.2 Timing Chart

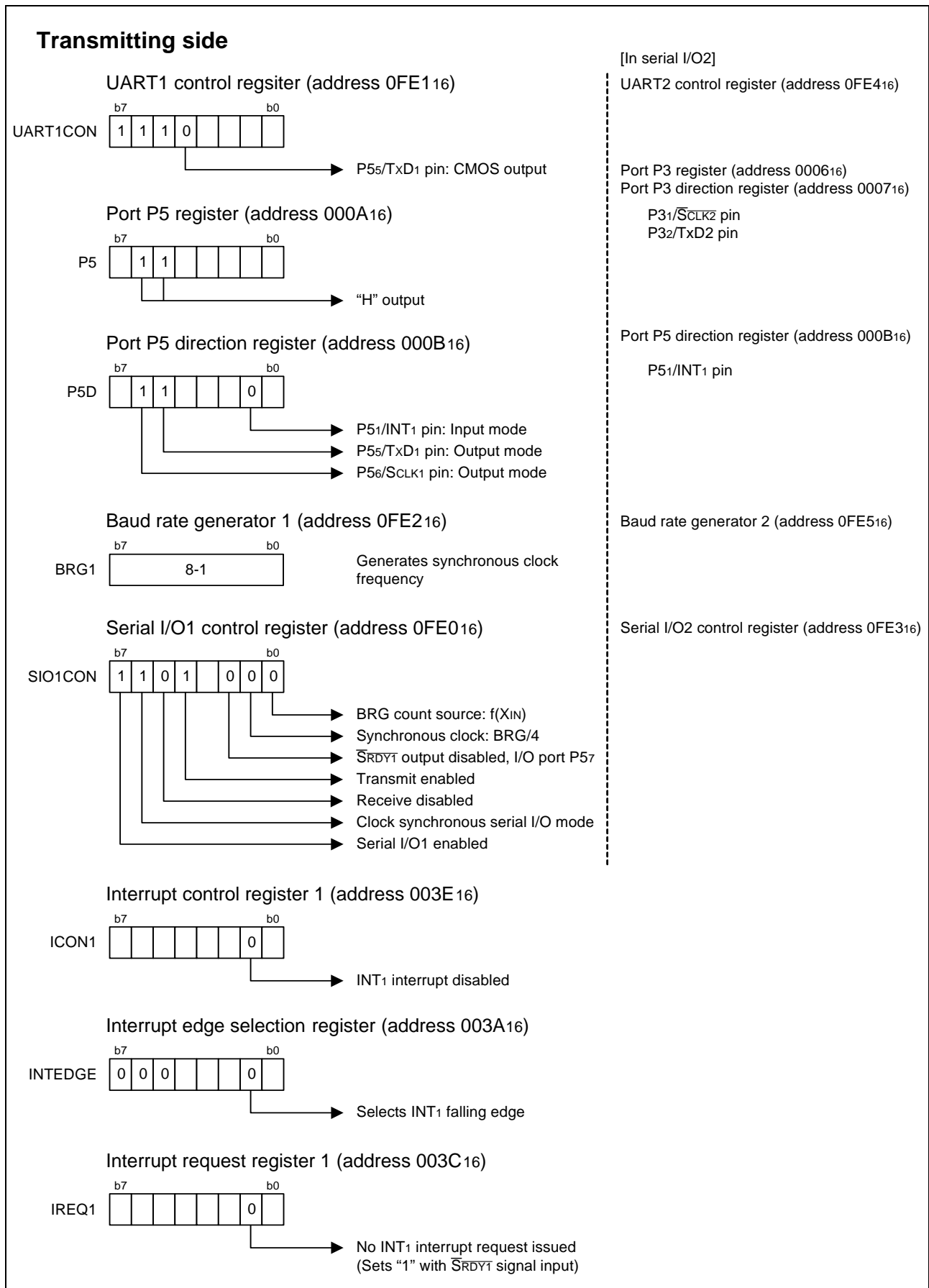


Figure 3.3 Registers Setting Relevant to the Transmitting Side (1)

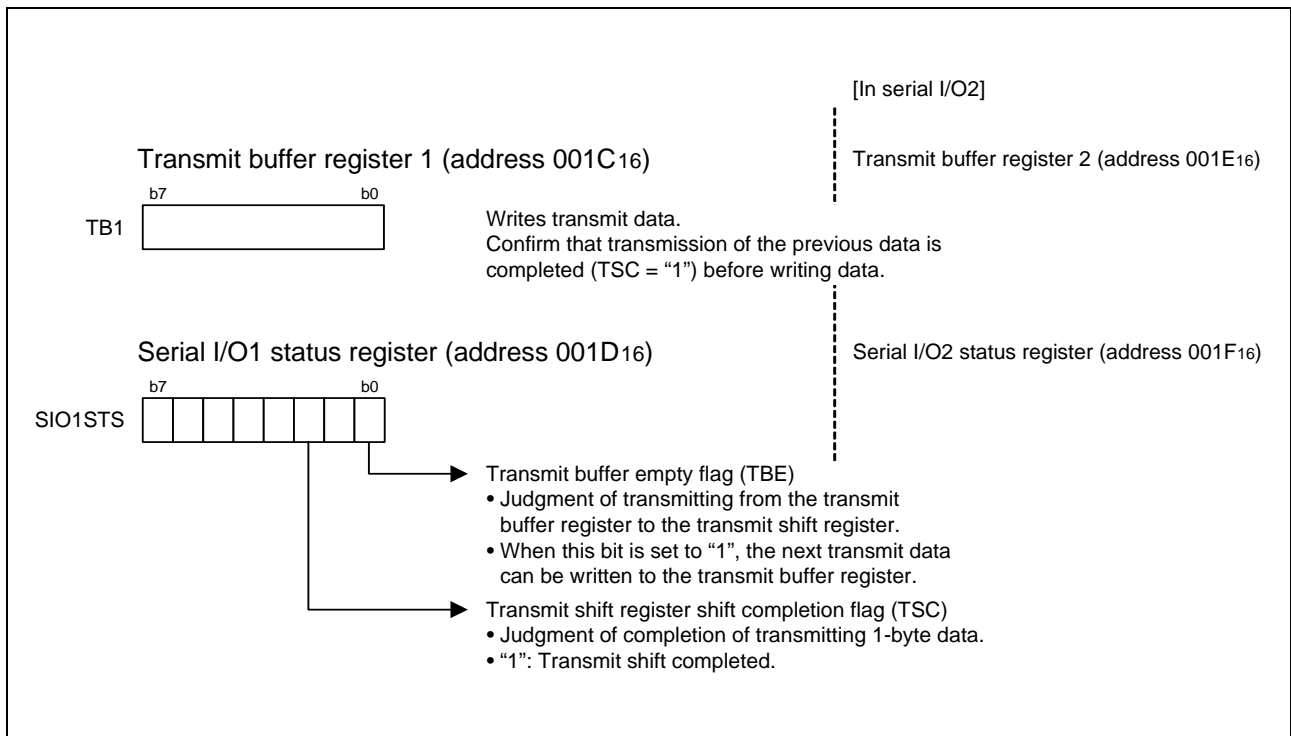


Figure 3.4 Registers Setting Relevant to the Transmitting Side (2)

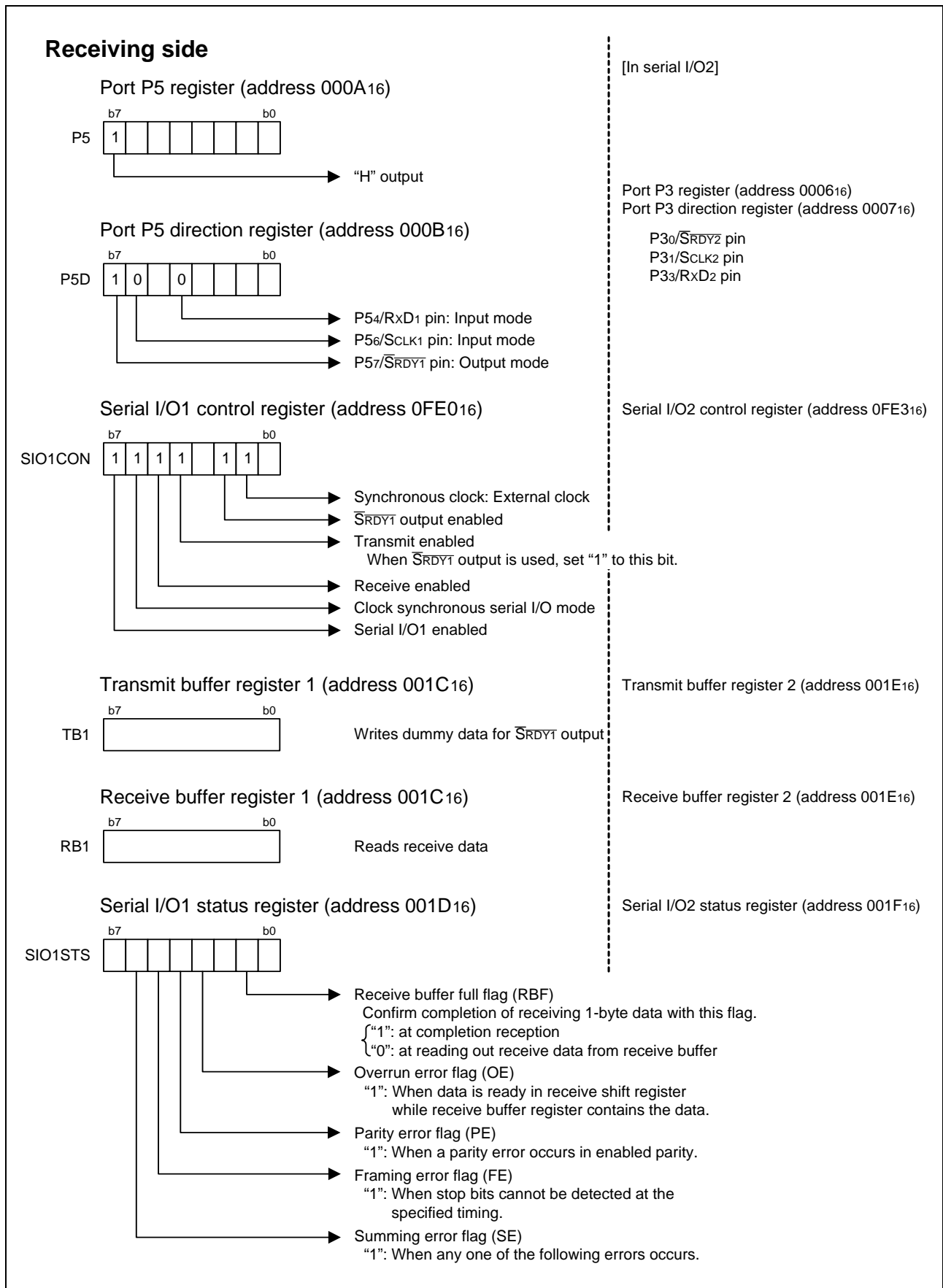
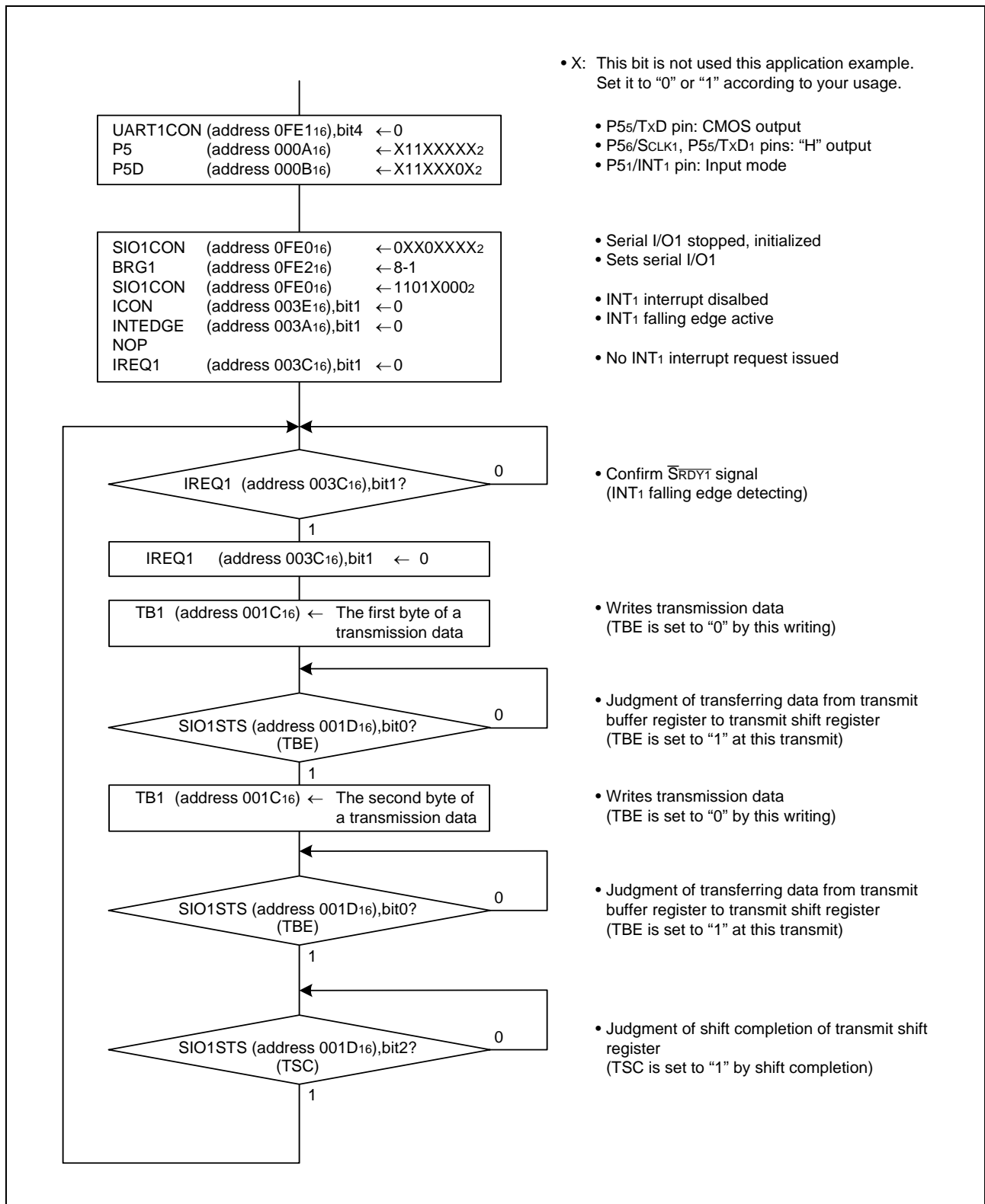
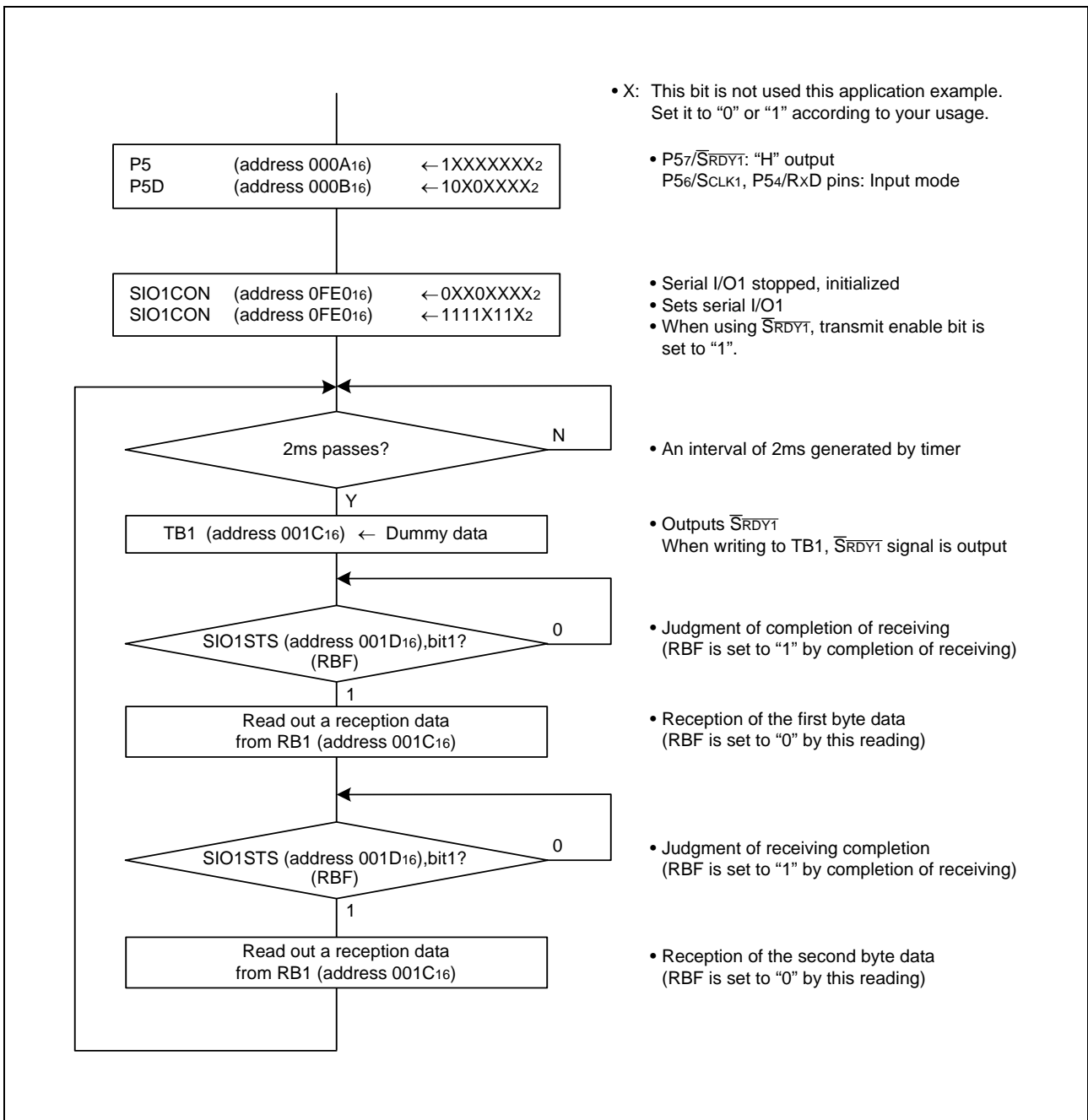


Figure 3.5 Registers Setting Relevant to the Receiving Side



- X: This bit is not used this application example. Set it to "0" or "1" according to your usage.
- P5₅/Tx_D pin: CMOS output
- P5₆/SCL_{K1}, P5₅/Tx_{D1} pins: "H" output
- P5₁/INT₁ pin: Input mode
- Serial I/O1 stopped, initialized
- Sets serial I/O1
- INT₁ interrupt disabled
- INT₁ falling edge active
- No INT₁ interrupt request issued
- Confirm $\overline{SRDY1}$ signal (INT₁ falling edge detecting)
- Writes transmission data (TBE is set to "0" by this writing)
- Judgment of transferring data from transmit buffer register to transmit shift register (TBE is set to "1" at this transmit)
- Writes transmission data (TBE is set to "0" by this writing)
- Judgment of transferring data from transmit buffer register to transmit shift register (TBE is set to "1" at this transmit)
- Judgment of shift completion of transmit shift register (TSC is set to "1" by shift completion)

Figure 3.6 Control Procedure of Transmitting Side



• X: This bit is not used this application example. Set it to "0" or "1" according to your usage.

• P57/ $\overline{SRDY1}$: "H" output
P56/SCLK1, P54/RxD pins: Input mode

• Serial I/O1 stopped, initialized
• Sets serial I/O1
• When using $\overline{SRDY1}$, transmit enable bit is set to "1".

• An interval of 2ms generated by timer

• Outputs $\overline{SRDY1}$
When writing to TB1, $\overline{SRDY1}$ signal is output

• Judgment of completion of receiving (RBF is set to "1" by completion of receiving)

• Reception of the first byte data (RBF is set to "0" by this reading)

• Judgment of receiving completion (RBF is set to "1" by completion of receiving)

• Reception of the second byte data (RBF is set to "0" by this reading)

Figure 3.7 Control Procedure of Receiving Side

4. Sample Programming Code

```

Transmitting side
[Setting of control register]
    LDA UART1CON          ;Set TXD CMOS-OUT
    AND #%11101111
    STA UART1CON
    LDM #%01100000,P5     ;Set Port P5 register
    LDM #%01100000,P5D   ;Set Port P5 direction register
;
    LDA #%00000000       ;Set Serial I/O1 control register
    STA SIO1CON
    LDA #8-1             ;Set SIO/UART bit rate generator1
    STA BRG1
    LDA #%11010000       ;Set Serial I/O1 control register
    STA SIO1CON
    CLB 1,ICON1          ;INT1 interrupt enable
    CLB 1,INTEDGE        ;INT1 down-edge set
    NOP
    CLB 1,IREQ1          ;INT1 interrupt request clear
;

[Main routine processing]
__MAIN:
    BBC 1,IREQ1,__MAIN   ;INT1 check
    CLB 1,IREQ1
;
    LDM #$055,TB1        ;Send data set
;
__MAIN00:
    BBC 0,SIO1STS,__MAIN00 ;Send check
;
    LDM #$0AA,TB1        ;Send data set
;
__MAIN01:
    BBC 0,SIO1STS,__MAIN01 ;Send check
;
__MAIN02:
    BBC 2,SIO1STS,__MAIN02 ;Shift end check
    BRA __MAIN
;
    
```

```

Receiving side
[Setting of control register]
    LDM #10000000,P5          ;Set Port P5 register
    LDM #10000000,P5D        ;Set Port P5 direction register
;
    LDA #00000000            ;Set Serial I/O1 control register
    STA SIO1CON
    LDA #11110110            ;Set Serial I/O1 control register
    STA SIO1CON
;

[Main routine processing]
__MAIN:
    BBC 6,IREQ1,__MAIN        ;2ms check
    CLB 6,IREQ1
;
    LDM #055,TB1              ;Dummy data set
;
__MAIN00:
    BBC 1,SIO1STS,__MAIN00    ;Receive check
;
    LDA RB1
    STA RECV_DATA              ;Receive data read
;
__MAIN01:
    BBC 1,SIO1STS,__MAIN01    ;Receive check
;
    LDA RB1
    STA RECV_DATA+1            ;Receive data read
    BRA __MAIN
;
    
```

5. Reference

Renesas Technology Corporation Semiconductor Home Page
<http://www.renesas.com>

E-mail Support
E-mail: support_apl@renesas.com

Data Sheet
38C2 Group (A version) Data sheet
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REVISION HISTORY	38C2 Group Serial I/O 1, 2 (Clock Synchronous Serial I/O Mode: Example-1)
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Rev.	Date	Description	
		Page	Summary
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