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38C2 Group
List of Registers

1. Abstract

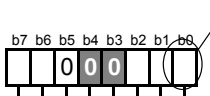
The following article describes the control registers of the 38C2 Group.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: 38C2 Group

3. Structure of Register

.....register



..... register (....) [Address : ....16]

b	Name	Functions	At reset (*2)	RW (*3)
0	.....bits	0 0 : ..... 0 1 : ..... 1 0 : ..... 1 1 : Do not select.	0	RW
1			0	RW
2	.....bit	0 : ..... 1 :	0	RW
3	The contents are “0” at reading. If writing to these bits, write“0”.		0	RO
4	The contents are undefined at reading. If writing to this bit, write“0”.		Undefined	-
5	If writing to this bit, write “0”.		0	RW
6	.....flag	0 : ..... 1 :	0	RO
7	.....bit	0 : ..... 1 :	0	RO

*1
Blank : Set “1” or “0” to this bit as usage.
0 : If writing to this bit, write “0”.
1 : If writing to this bit, write “1”.
× : This bit is not used in the specific mode or state.
■ : Nothing is arranged for this bit.

*2
0 : “0” at reset release
1 : “1” at reset release
Undefined : Undefined at reset release

*3
RW : Read enabled. Write enabled.
RO : Read enabled. This value depends on each bit at writing.
WO : Write enabled. Undefined at reading.
- : Undefined at reading. This value depends on each bit at writing.

4. List of Registers

Port Pi register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi register (Pi) (i = 0 to 5)

[Addresses 0000_{16}, 0002_{16}, 0004_{16}, 0006_{16}, 0008_{16}, $000A_{16}$]

b	Name	Functions	At reset	RW
0	Port Pi_0	•In output mode Write •••••••• Port latch Read •••••••• Port latch •In input mode Write •••••••• Port latch Read •••••••• Value of pin	0	RW
1	Port Pi_1		0	RW
2	Port Pi_2		0	RW
3	Port Pi_3		0	RW
4	Port Pi_4		0	RW
5	Port Pi_5		0	RW
6	Port Pi_6		0	RW
7	Port Pi_7		0	RW

Fig. 4.1 Structure of Port Pi register (i = 0 to 5)

Port P6 register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0

Port P6 register (P6)

[Address $000C_{16}$]

b	Name	Functions	At reset	RW
0	Port $P6_0$	•In output mode Write •••••••• Port latch Read •••••••• Port latch •In input mode Write •••••••• Port latch Read •••••••• Value of pin	0	RW
1	Port $P6_1$		0	RW
2	Port $P6_2$		0	RW
3	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.2 Structure of Port P6 register

Port Pi direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (PiD) (i =0 to 5)

[Addresses 0001_{16}, 0003_{16}, 0005_{16}, 0007_{16}, 0009_{16}, $000B_{16}$]

b	Name	Functions	At reset	RW
0	Port Pi_0 direction register	0 : Input mode 1 : Output mode	0	WO
1	Port Pi_1 direction register	0 : Input mode 1 : Output mode	0	WO
2	Port Pi_2 direction register	0 : Input mode 1 : Output mode	0	WO
3	Port Pi_3 direction register	0 : Input mode 1 : Output mode	0	WO
4	Port Pi_4 direction register	0 : Input mode 1 : Output mode	0	WO
5	Port Pi_5 direction register	0 : Input mode 1 : Output mode	0	WO
6	Port Pi_6 direction register	0 : Input mode 1 : Output mode	0	WO
7	Port Pi_7 direction register	0 : Input mode 1 : Output mode	0	WO

Note: When ports P0-P2 are set as input mode, control of pull-up resistor can be performed by the segment output disable registers 0-2 (addresses $0FF8_{16}$-$0FFA_{16}$) (refer to Fig.4.51). Pull-up resistor is not connected to the port set as output mode. Ports P3-P5 can control the pull-up resistor by the PULL register (address $0FF1_{16}$). In the port set as output mode, a pull-up control bit becomes invalid, and the pull-up resistor is not connected.

Fig. 4.3 Structure of Port Pi direction register (i = 0 to 5)

Port P6 direction register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0

Port P6 direction register (P6D)

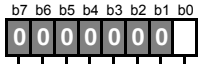
[Address $000D_{16}$]

b	Name	Functions	At reset	RW
0	Ports $P6_0$ direction register	0 : Input mode 1 : Output mode	0	WO
1	Ports $P6_1$ direction register	0 : Input mode 1 : Output mode	0	WO
2	Ports $P6_2$ direction register	0 : Input mode 1 : Output mode	0	WO
3	The contents are undefined at reading. If writing to this bit, write“0”.		Undefined	-
4			Undefined	-
5			Undefined	-
6			Undefined	-
7			Undefined	-

Note: Port P6 can control the pull-up resistor by the PULL register (address $0FF1_{16}$). In the port set as output mode, a pull-up control bit becomes invalid, and the pull-up resistor is not connected.

Fig. 4.4 Structure of Port P6 direction register

Clock output control register



Clock output control register (CKOUT)

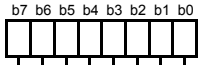
[Address 0018$_{16}$]

b	Name	Functions	At reset	RW
0	P3$_6$ clock output control bit	0 : Timer 2 output 1 : System clock φ output	0	RW
1	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO
2			0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Note: Do not write “1” to these bits.

Fig. 4.5 Structure of Clock output control register

A-D control register



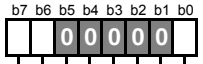
A-D control register (ADCON)

[Address 0019$_{16}$]

b	Name	Functions	At reset	RW
0	Analog input pin selection bits	b2 b1 b0 0 0 0 : P4$_0$/OUT$_{0}$/AN$_0$ 0 0 1 : P4$_1$/OUT$_{1}$/AN$_1$ 0 1 0 : P4$_2$/AN$_2$ 0 1 1 : P4$_3$/AN$_3$ 1 0 0 : P4$_4$/AN$_4$ 1 0 1 : P4$_5$/AN$_5$ 1 1 0 : P4$_6$/RTP$_0$/AN$_6$ 1 1 1 : P4$_7$/RTP$_1$/AN$_7$	0	RW
1			0	RW
2			0	RW
3	AD conversion completion bit	0 : Conversion in progress 1 : Conversion completed	1	RW
4	AD conversion clock selection bits	b5 b4 0 0 : X$_{IN}$/2 0 1 : X$_{IN}$/4 1 0 : X$_{IN}$/8 1 1 : X$_{IN}$/16	0	RW
5			0	RW
6	10-bit or 8-bit conversion switch bit	0 : 10-bitAD 1 : 8-bitAD	0	RW
7	Booster selection bit	0 : Booster not used 1 : Booster used	0	RW

Fig. 4.6 Structure of A-D control register

A-D conversion low-order register



A-D conversion low-order register (ADL)

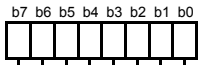
[Address 001A16]

b	Functions	At reset	RW
0	Vref input switch bit 0 : Auto 1 : ON	0	WO
1	The contents are “0” at reading. If writing to these bits, write “0”.	0	RO
2		0	RO
3		0	RO
4		0	RO
5		0	RO
6	In the 10-bit A-D mode, A-D conversion result can be read. In the 8-bit A-D mode, the contents are undefined at writing. If writing to these bits,write “0”.	Undefined	RO
7	At 10-bit A-D mode b7 b0 b1 b0 0	Undefined	RO

Note: During A-D conversion, do not read these registers.

Fig. 4.7 Structure of A-D conversion low-order register

A-D conversion high-order register



A-D conversion high-order register (ADH)

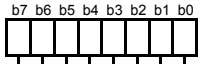
[Address 001B16]

b	Functions	At reset	RW
0	A-D conversion result can be read. Write “0016” to these bits at writing. At 10-bit A-D mode b7 b0 b9 b8 b7 b6 b5 b4 b3 b2 At 8-bit A-D mode b7 b0 b9 b8 b7 b6 b5 b4 b3 b2	Undefined	RO
1		Undefined	RO
2		Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

Note: During A-D conversion, do not read these registers.

Fig. 4.8 Structure of A-D conversion high-order register

Transmit buffer register 1,2



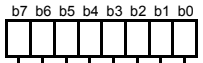
Transmit buffer register1 (TB1) [Address 001C16]
Transmit buffer register2 (TB2) [Address 001E16]

b	Functions	At reset	RW
0	The transmission data is written to this buffer register.	Undefined	RW
1	Write transmission data to this register.	Undefined	RW
2		Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Note: This register is assigned to the same address as the receive buffer register. This register cannot be read.

Fig. 4.9 Structure of Transmit buffer register/Receive buffer register 1

Receive buffer register 1,2



Receive buffer register (RB1) [Address 001C16]
Receive buffer register (RB2) [Address 001E16]

b	Functions	At reset	RW
0	The receive data is read from this buffer register.	Undefined	RW
1	Read receive data from this register.	Undefined	RW
2		Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Note: This register is assigned to the same address as the transmit buffer register. This register cannot be written to.

Fig. 4.10 Structure of Transmit buffer register/Receive buffer register 2

Serial I/O1 status register and Serial I/O2 status register

b7 b6 b5 b4 b3 b2 b1 b0
1

Serial I/O1 status register (SIO1STS) [Address 001D16]
Serial I/O2 status register (SIO2STS) [Address 001F16]

b	Name	Functions	At reset	RW
0	Transmit buffer empty flag (TBE)	0: Buffer register full 1: Buffer register empty	0	RO
1	Receive buffer full flag (RBF)	0: Buffer register empty 1: Buffer register full	0	RO
2	Transmit shift register shift completion flag(TSC)	0: Transmit shift in progress 1: Transmit shift completed	0	RO
3	Overrun error flag (OE)	0: No error 1: Overrun error	0	RO
4	Parity error flag (PE)	0: No error 1: Parity error	0	RO
5	Framing error flag (FE)	0: No error 1: Framing error	0	RO
6	Summing error flag (SE)	0: (OE) U (PE) U (FE) = 0 1: (OE) U (PE) U (FE) = 1	0	RO
7	The contents are “1” at reading. If writing to this bit, write “1”.		1	RO

Note: Writing to this register sets all the error flags OE, PE, FE and SE to “1”.

Fig. 4.11 Structure of Serial I/O1 status register and Serial I/O2 status register

Timer 1 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 1 register (T1)
[Address 002016]

b	Functions	At reset	RW
0	Set the count initial value. This register counts (n+1) times, where the set value is n. [At write] Writes data to both timer 1 latch and timer 1 simultaneously. [At read] The timer 1 count value is read by reading this register.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.12 Structure of Timer 1 register

Timer 2 register

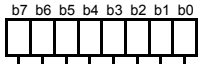
b7 b6 b5 b4 b3 b2 b1 b0

Timer 2 register (T2)
[Address 002116]

b	Functions	At reset	RW
0	Set the count initial value. This register counts (n+1) times, where the set value is n.	1	RW
1	[At write] These registers operate according to the value of Timer 2 write control bit. •When Timer 2 write control bit = “0”	0	RW
2	Writes data to both timer 2 latch and timer 2 simultaneously •When Timer 2 write control bit = “1”	0	RW
3	Writes data only to timer 2 latch [At read] The timer 2 count value is read by reading this register.	0	RW
4		0	RW
5		0	RW
6		0	RW
7		0	RW

Fig. 4.13 Structure of Timer 2 register

Timer 3 register



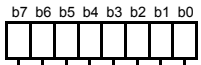
Timer 3 register (T3)

[Address 0022_{16}]

b	Functions	At reset	RW
0	Set the count initial value. This register counts (n+1) times, where the set value is n. [At write] These registers operate according to the value of Timer 3 write control bit. •When Timer 3 write control bit = "0" Writes data to both timer 3 latch and timer 3 simultaneously •When Timer 3 write control bit = "1" Writes data only to timer 3 latch [At read] The timer 3 count value is read by reading this register.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.14 Structure of Timer 3 register

Timer 4 register



Timer 4 register (T4)

[Address 0023_{16}]

b	Functions	At reset	RW
0	Set the count initial value. This register counts (n+1) times, where the set value is n. [At write] These registers operate according to the value of Timer 4 write control bit. •When Timer 4 write control bit = "0" Writes data to both timer 4 latch and timer 4 simultaneously •When Timer 4 write control bit = "1" Writes data only to timer 4 latch [At read] The timer 4 count value is read by reading this register.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.15 Structure of Timer 4 register

PWM01 register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

PWM01 register (PWM01)

[Address 0024$_{16}$]

b	Name	Functions	At reset	RW
0	PWM0 set bits	b1 b0 0 0 : No extended 0 1 : Extended once in four periods 1 0 : Extended twice in four periods 1 1 : Extended three times in four periods	0	RW
1			0	RW
2	PWM1 set bits	b3 b2 0 0 : No extended 0 1 : Extended once in four periods 1 0 : Extended twice in four periods 1 1 : Extended three times in four periods	0	RW
3			0	RW
4	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.16 Structure of PWM01 register

Timer 12 mode register

b7	b6	b5	b4	b3	b2	b1	b0

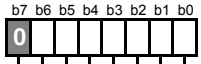
Timer 12 mode register (T12M)

[Address 0025$_{16}$]

b	Name	Functions	At reset	RW
0	Timer 1 count stop bit	0 : Count operation 1 : Count stop	0	RW
1	Timer 2 count stop bit	0 : Count operation 1 : Count stop	0	RW
2	Timer 1 count source selection bits	b3 b2 0 0 : Frequency divider for Timer 1 0 1 : f(XCIN) 1 0 : Underflow of Timer Y 1 1 : Not available	0	RW
3			0	RW
4	Timer 2 count source selection bits	b5 b4 0 0 : Underflow of Timer 1 0 1 : f(XCIN) 1 0 : Frequency divider for Timer 2 1 1 : Not available	0	RW
5			0	RW
6	Timer 2 output selection bit (P36)	0 : I/O port 1 : Timer 2 output	0	RW
7	T2OUT output edge switch bit	0 : Start at “L” output 1 : Start at “H” output	0	RW

Fig. 4.17 Structure of Timer 12 mode register

Timer 34 mode register



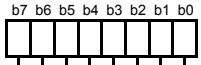
Timer 34 mode register (T34M)

[Address 0026_{16}]

b	Name	Functions	At reset	RW
0	Timer 3 count stop bit	0 : Count operation 1 : Count stop	0	RW
1	Timer 4 count stop bit	0 : Count operation 1 : Count stop	0	RW
2	Timer 3 count source selection bit	0 : Frequency divider for Timer 3 1 : Underflow of Timer 2	0	RW
3	Timer 4 count source selection bits	b4 b3 0 0 : Frequency divider for Timer 4 0 1 : Underflow of Timer 3 1 0 : Underflow of Timer 2 1 1 : Not available	0	RW
4			0	RW
5	Timer 3 operating mode selection bit	0 : Timer mode 1 : PWM mode	0	RW
6	Timer 4 operating mode selection bit	0 : Timer mode 1 : PWM mode	0	RW
7	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO

Fig. 4.18 Structure of Timer 34 mode register

Compare register (low-order, high-order)



Compare register (low-order, high-order) (COMPL, COMPH)

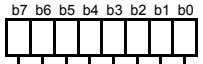
[Address 0028_{16}, 0029_{16}]

b	Functions	At reset	RW
0	Set a value of the compare register.	0	RW
1		0	RW
2		0	RW
3		0	RW
4		0	RW
5		0	RW
6		0	RW
7		0	RW

Note: When writing to this register in the PWM mode or the IGBT output mode, write to the following registers in the order as shown below; the compare register (high- and low-order), the timer X register (low-order), the timer X register (high-order).
It is possible to use whichever order to write to the compare register (high- and low-order).

Fig. 4.19 Structure of Compare register (low-order, high-order)

Timer X low-order register , Timer X high-order register



Timer X low-order register (TXL) [Addresses 002A16]

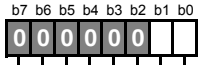
Timer X high-order register (TXH) [Addresses 002B16]

b	Functions	At reset	RW
0	Set the count initial value. These registers count (n+1) times, where the set value is n. [At write] Depending on the timer X write control bit , these registers operate as follows. •When Timer X write control bit = "0" Writes data to both timer X latch and timer X simultaneously •When Timer X write control bit = "1" Writes data only to timer X latch Write both registers from TXL to TXH in consecutive order. This operation is not affected by the timer X stop control bit. [At read] The timer X count value is read by reading these registers. Read both registers from TXH to TXL in consecutive order.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Note: When writing to this register in the PWM mode or the IGBT mode, write to the following registers in the order as shown below; the compare register (high- and low-order), the timer X register (low-order), the timer X register (high-order).

Fig. 4.20 Structure of Timer X low-order register , Timer X high-order register

Timer X register (Extend)



Timer X register (Extend) (TXEX)

[Addresses 002C16]

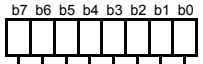
b	Functions	At reset	RW
0	Set the count initial value. These registers count (n+1) times, where the set value is n. [At write] Depending on the timer X write control bit , these registers operate as follows. •When Timer X write control bit = "0" Writes data to both extend latch and extend counter simultaneously •When Timer X write control bit = "1" Writes data only to extend latch [At read] The count value of extend counter is read by reading these registers.	0	RW
1		0	RW
2	The contents are "0" at reading. If writing to these bits, write "0".	0	RO
3		0	RO
4		0	RO
5		0	RO
6		0	RO
7		0	RO

Notes:

1. When a value is set to this register after reset, timer X operates as the 18-bit counter.
2. When writing to this register in the timer mode, the pulse output mode, the event counter mode, and the pulse width measurement mode, write to the following registers in the order as shown below; the timer X register (extension), the timer X register (low-order), the timer X register (high-order).
   When reading value from this register in all modes, read the following registers in the order as shown below, the timer X register (extension), timer X register (high-order), timer X register (low-order).
3. In the IGBT and PWM output modes, do not write "1" to this register. Also, when "1" is already written to this register, be sure to write "0" to this register before using.

Fig. 4.21 Structure of Timer X register (Extend)

Timer Y low-order register, Timer Y high-order register



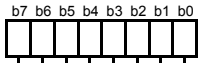
Timer Y low-order register (TYL) [Addresses 002D16]

Timer Y high-order register (TYH) [Addresses 002E16]

b	Functions	At reset	RW
0	Set the count initial value. These registers count (n+1) times, where the set value is n. [At write] Depending on the timer Y write control bit , these registers operate as follows. •When Timer Y write control bit = "0" Writes data to both timer Y latch and timer Y simultaneously •When Timer Y write control bit = "1" Writes data only to timer Y latch Write both registers from TYL to TYH in consecutive order. This operation is not affected by the timer Y stop control bit. [At read] The timer Y count value is read by reading these registers. Read both registers from TYH to TYL in consecutive order.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.22 Structure of Timer Y low-order register, Timer Y high-order register

Timer X mode register



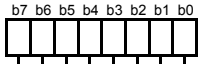
Timer X mode register (TXM)

[Address 002F16]

b	Name	Functions	At reset	RW
0	Timer X operating mode bits	b2 b1 b0 0 0 0 : Timer mode 0 0 1 : Pulse output mode 0 1 0 : IGBT output mode 0 1 1 : PWM mode 1 0 0 : Event counter mode 1 0 1 : Pulse width measurement mode	0	RW
1			0	RW
2			0	RW
3	Timer X write control bit	0 : Write data to both timer latch and timer 1 : Write data to timer latch only	0	RW
4	Timer X count source selection bit	0 : Frequency divider output 1 : f(XCIN)	0	RW
5	Data for control of event counter window	0 : Event count enabled 1 : Event count disabled	0	RW
6	Timer X count stop bit	0 : Count operation 1 : Count stop	0	RW
7	Timer X output selection bit (P35)	0 : I/O port 1 : Timer X output	0	RW

Fig. 4.23 Structure of Timer X mode register

Timer Y mode register



Timer Y mode register (TYM)

[Address 0030$_{16}$]

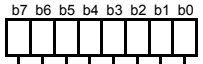
b	Name	Functions	At reset	RW
0	Real time port control bit	0 : Real time port function invalid 1 : Real time port function valid	0	RW
1	$P4_6$ data for real time port	0 : "L" output 1 : "H" output	0	RW
2	$P4_7$ data for real time port	0 : "L" output 1 : "H" output	0	RW
3	Timer Y count source selection bit	0 : Frequency divider output 1 : f(X_{CIN})	0	RW
4	Timer Y operating mode bits	b5 b4 0 0 : Timer mode 0 1 : Period measurement mode 1 0 : Event counter mode 1 1 : Pulse width HL continuous measurement mode	0	RW
5			0	RW
6	$CNTR_1$ active edge switch bit	This function changes according to timer Y operation mode. (Refer to Table 4.1.)	0	RW
7	Timer Y count stop bit	0 : Count operation 1 : Count stop	0	RW

Fig. 4.24 Structure of Timer Y mode register

Table 4.1 $CNTR_1$ active edge switch bit function

Timer Y operation mode	Set value	Timer function selection	CNTR1 interrupt request occurrence source
Timer mode	"0"	-	$CNTR_1$ input signal falling edge (No influence to timer count)
	"1"	-	$CNTR_1$ input signal rising edge (No influence to timer count)
Period measurement mode	"0"	Measures the falling edge to falling edge	Input signal falling edge
	"1"	Measures the rising edge to rising edge	Input signal rising edge
Event counter mode	"0"	Count at rising edge	Input signal falling edge
	"1"	Count at falling edge	Input signal rising edge
Pulse width HL continuously measurement mode	"0"	Measures "H" and "L" pulse widths	Input signal falling and rising edges
	"1"		

Watchdog timer control register



Watchdog timer control register (WDTCON)

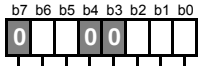
[Address 0037_{16}]

b	Name	Functions	At reset	RW
0	Watchdog timer H		1	RO
1			1	RO
2			1	RO
3			1	RO
4			1	RO
5			1	RO
6	STP instruction disable bit	0: STP instruction enabled 1: STP instruction disabled	0	RW
7	Watchdog timer H count source selection bit	0: 1/1024 of system clock 1: 1/4 of system clock	0	RW

Note: The watchdog timer is set to "FF_{16}" by writing to this register.

Fig. 4.25 Structure of Watchdog timer control register

LCD power control register



LCD power control register (VLCON)

[Address 0038_{16}]

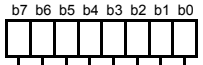
b	Name	Functions	At reset	RW
0	Dividing resistor for LCD power control bit	0 : Internal dividing resistor disconnected from LCD power circuit 1 : Internal dividing resistor connected to LCD power circuit	0	RW
1	Dividing resistor for LCD power selection bits	b3 b2 1 0 : Larger resistor 0 1 : 0 0 : 1 1 : Smaller resistor	0	RW
2			0	RW
3	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO
4			0	RO
5	VL pin input selection bit	0 : Input invalid 1 : VL input function valid	0	RW
6	V_{L3} connection bit	0 : Connect LCD internal V_{L3} to V_{CC} 1 : Connect LCD internal V_{L3} to V_{L3} pin	0	RW
7	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO

Notes:

1. When voltage is applied to V_{L1} to V_{L3} by using the external resistor , write “10_2” to dividing resistor for LCD power selection bits.
2. Setting to the VL pin input selection bit (VLSEL) = “1”has the most priority than setting to the port P2 direction register (address 0005_{16}) and segment output disable register 2 (address $0FFA_{16}$).
3. When the LCD drive control circuit is use dat V_{L3} = V_{CC} , apply V_{CC} to V_{L3} pin and write “1” to V_{L3} connection bit.

Fig. 4.26 Structure of LCD power control register

LCD mode register



LCD mode register (LM)

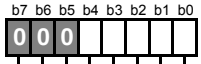
[Address 39_{16}]

b	Name	Functions	At reset	RW
0	Duty ratio selection bits	b1 b0 0 0: Do not select 0 1: 2 duty (use COM_0, COM_1) 1 0: 3 duty (use COM_0–COM_2) 1 1: 4 duty (use COM_0–COM_3)	0	RW
1			0	RW
2	Bias control bit	0: 1/3 bias 1: 1/2 bias	0	RW
3	LCD enable bit	0: LCD OFF 1: LCD ON	0	RW
4	LCD drive timing selection bit	0: Type A 1: Type B	0	RW
5	LCD circuit divider division ratio selection bits	b1 b0 0 0: Clock input 0 1: 2 division of clock input 1 0: 4 division of clock input 1 1: 8 division of clock input	0	RW
6			0	RW
7	LCDCK count source selection bit (Note)	0: f(X_{CIN})/32 1: f(X_{IN})/8192 (f(X_{CIN})/8192 in low speed mode)	0	RW

Note: LCDCK is a clock for an LCD timing controller.

Fig. 4.27 Structure of LCD mode register

Interrupt edge selection register



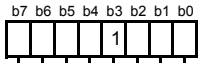
Interrupt edge selection register (INTEDGE)

[Address 003A16]

b	Name	Functions	At reset	RW
0	INT0 active edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
1	INT1 active edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
2	INT2 active edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
3	INT2/Key input interrupt switch bit	0 : INT2 interrupt 1 : Key input interrupt	0	RW
4	Timer Y/CNTR1 interrupt switch bit	0 : Timer Y interrupt 1 : CNTR1 interrupt	0	RW
5	When these bits are read out, the contents are “0”. If writing to these bits, write “0”.		0	RO
6			0	RO
7			0	RO

Fig. 4.28 Structure of Interrupt edge selection register

CPU mode register



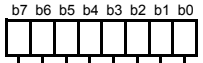
CPU mode register (CPUM)

[Address 3B16]

b	Name	Functions	At reset	RW
0	Processor mode bits	b1 b0 00 : Single-chip mode 01 : Do not select 10 : Do not select 11 : Do not select	0	RW
1			0	RW
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	RW
3	Write “1” to this bit at writing.		1	RW
4	Main clock (XIN-XOUT) division ratio selection bit	b5 b4 0 0 : XIN/8 (frequency/8 mode) 0 1 : XIN/4 (frequency/4 mode) 1 0 : XIN/2 (frequency/2 mode) 1 1 : Not available	0	RW
5			0	RW
6	System clock selection bit	b7 b6 0 0 : XIN stop, XCIN oscillating, system clock = XCIN 0 1 : XIN oscillating, XCIN stop, system clock = XIN 1 0 : XIN oscillating, XCIN oscillating, system clock = XCIN 1 1 : XIN oscillating, XCIN oscillating, system clock = XIN	1	RW
7			0	RW

Fig. 4.29 Structure of CPU mode register

Interrupt request register 1



Interrupt request register 1 (IREQ1)

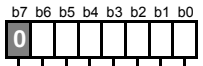
[Address 003C16]

b	Name	Functions	At reset	RW
0	INT0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
1	INT1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
2	INT2/key input interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
3	Serial I/O1 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
4	Serial I/O1 transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
5	Serial I/O2 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
6	Serial I/O2 transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
7	Timer X interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)

Note: This bit can be set to “0” but not to “1” by program.

Fig. 4.30 Structure of Interrupt request register 1

Interrupt request register 2



Interrupt request register 2 (IREQ2)

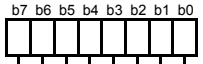
[Address 003D16]

b	Name	Functions	At reset	RW
0	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
1	Timer 2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
2	Timer 3 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
3	Timer 4 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
4	CNTR0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
5	Timer Y/CNTR1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
6	AD converter interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
7	The contents are “0” at reading. If writing to this bit, write “0”.		0	RO

Note: This bit can be set to “0” but not to “1” by program.

Fig. 4.31 Structure of Interrupt request register 2

Interrupt control register 1



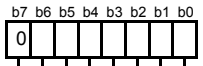
Interrupt control register 1 (ICON1)

[Address 003E16]

b	Name	Functions	At reset	RW
0	INT0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
1	INT1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
2	INT2/key input interrupt request bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
3	Serial I/O1 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
4	Serial I/O1 transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
5	Serial I/O2 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
6	Serial I/O2 transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
7	Timer X interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW

Fig. 4.32 Structure of Interrupt control register 1

Interrupt control register 2



Interrupt control register 2 (ICON2)

[Address 003F16]

b	Name	Functions	At reset	RW
0	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
1	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
2	Timer 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
3	Timer 4 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
4	CNTR0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
5	Timer Y/CNTR1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
6	AD converter interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
7	Write “0” to this bit at writing.		0	RW

Fig. 4.33 Structure of Interrupt request register 2

LCD display RAM

address		bit 7	6	5	4	3	2	1	0	reset	RW
		COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0		
0040_{16}	LRAM0	SEG_1				SEG_0				Undefined	RW
0041_{16}	LRAM1	SEG_3				SEG_2				Undefined	RW
0042_{16}	LRAM2	SEG_5				SEG_4				Undefined	RW
0043_{16}	LRAM3	SEG_7				SEG_6				Undefined	RW
0044_{16}	LRAM4	SEG_9				SEG_8				Undefined	RW
0045_{16}	LRAM5	SEG_{11}				SEG_{10}				Undefined	RW
0046_{16}	LRAM6	SEG_{13}				SEG_{12}				Undefined	RW
0047_{16}	LRAM7	SEG_{15}				SEG_{14}				Undefined	RW
0048_{16}	LRAM8	SEG_{17}				SEG_{16}				Undefined	RW
0049_{16}	LRAM9	SEG_{19}				SEG_{18}				Undefined	RW
$004A_{16}$	LRAM10	SEG_{21}				SEG_{20}				Undefined	RW
$004B_{16}$	LRAM11	SEG_{23}				SEG_{22}				Undefined	RW

Fig. 4.34 LCD display RAM

Serial I/O1 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O1 control register (SIO1CON)

[Address 0FE0$_{16}$]

b	Name	Functions	At reset	RW
0	BRG count source selection bit (CSS)	0 : f(XIN) (Note1) 1 : f(XIN)/4 (Note2)	0	RW
1	Serial I/O1 synchronous clock selection bit (SCS)	In clock synchronous serial I/O mode 0 : BRG output divided by 4 1 : External clock input In UART mode 0 : BRG output divided by 16 1 : External clock input divided by16	0	RW
2	$\overline{SRDY1}$ output enable bit (SRDY)	0 : I/O port (P57 pin) 1 : $\overline{SRDY1}$ output pin	0	RW
3	Transmit interrupt source selection bit (TIC)	0: Transmit buffer register empty 1: Transmit shift operation of transmit shift register completed	0	RW
4	Transmit enable bit (TE)	0: Transmit disabled 1: Transmit enabled	0	RW
5	Receive enable bit (RE)	0: Receive disabled 1: Receive enabled	0	RW
6	Serial I/O1 mode selection bit (SIOM)	0: UART mode 1: Clock synchronous serial I/O mode	0	RW
7	Serial I/O1 enable bit (SIOE)	0: Serial I/O1 disabled (P54 to P57: I/O port) 1: Serial I/O1 enabled (P54 to P57: Serial I/O1 pins)	0	RW

Notes:
1. f(XCIN) in low speed mode
2. f(XCIN)/4 in low speed mode

Fig. 4.35 Structure of Serial I/O1 control register

UART1 control register

b7 b6 b5 b4 b3 b2 b1 b0
1 1 1

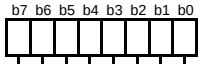
UART1 control register (UART1CON)

[Address 0FE1$_{16}$]

b	Name	Functions	At reset	RW
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	RW
1	Parity enable bit (PARE)	0: Parity checking disabled 1: Parity checking enabled	0	RW
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	RW
3	Stop bit length selection bit (STPS)	0: 1 stop bit 1: 2 stop bits	0	RW
4	P55/TxD1 P-channel output disable bit(POFF)	In output mode 0: CMOS output 1: N-channel open-drain output	0	RW
5	The contents are “1” at reading. If writing to these bits, write “1”.		1	RO
6			1	RO
7			1	RO

Fig. 4.36 Structure of UART1 control register

Baud rate generator i



Baud rate generator i (BRGi) (i=1,2)

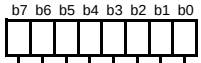
[Address 0FE2$_{16}$,0FE5$_{16}$]

b	Functions	At reset	RW
0	Set the divided value of BRG count source. The baud rate generator divides the frequency of the count source by 1/(n+1), where n is the value written to the baud rate generator.	Undefined	RW
1		Undefined	RW
2		Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Note: Only write to this register while transmit/receive operation is stopped.

Fig. 4.37 Structure of Baud rate generator i (i=1,2)

Serial I/O2 control register



Serial I/O2 control register (SIO2CON)

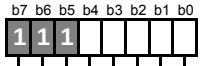
[Address 0FE3$_{16}$]

b	Name	Functions	At reset	RW
0	BRG count source selection bit (CSS)	0 : f(XIN) (Note1) 1 : f(XIN)/4 (Note2)	0	RW
1	Serial I/O2 synchronous clock selection bit (SCS)	In clock synchronous serial I/O mode 0 : BRG output divided by 4 1 : External clock input In UART mode 0 : BRG output divided by 16 1 : External clock input divided by16	0	RW
2	$\overline{SRDY2}$ output enable bit (SRDY)	0 : I/O port (P3$_0$ pin) 1 : $\overline{SRDY2}$ output pin	0	RW
3	Transmit interrupt source selection bit (TIC)	0: Transmit buffer register empty 1: Transmit shift operation of transmit shift register completed	0	RW
4	Transmit enable bit (TE)	0: Transmit disabled 1: Transmit enabled	0	RW
5	Receive enable bit (RE)	0: Receive disabled 1: Receive enabled	0	RW
6	Serial I/O2 mode selection bit (SIOM)	0: UART mode 1: Clock synchronous serial I/O mode	0	RW
7	Serial I/O2 enable bit (SIOE)	0: Serial I/O2 disabled (P3$_0$ to P3$_3$: I/O port) 1: Serial I/O2 enabled (P3$_0$ to P3$_3$: Serial I/O1 pins)	0	RW

Notes:
1. f(XCIN) in low speed mode
2. f(XCIN)/4 in low speed mode

Fig. 4.38 Structure of Serial I/O2 control register

UART2 control register



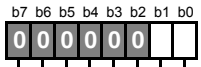
UART2 control register (UART2CON)

[Address 0FE4$_{16}$]

b	Name	Functions	At reset	RW
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	RW
1	Parity enable bit (PARE)	0: Parity checking disabled 1: Parity checking enabled	0	RW
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	RW
3	Stop bit length selection bit (STPS)	0: 1 stop bit 1: 2 stop bits	0	RW
4	P3$_2$/TxD$_2$ P-channel output disable bit(POFF)	In output mode 0: CMOS output 1: N-channel open-drain output	0	RW
5	The contents are “1” at reading. If writing to these bits, write “1”.		1	RO
6			1	RO
7			1	RO

Fig. 4.39 Structure of UART2 control register

Oscillation output control register



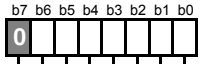
Oscillation output control register (OSCOUT)

[Address 0FF0$_{16}$]

b	Name	Functions	At reset	RW
0	P4$_0$/P4$_1$ oscillation output control bits	b1 b0 00: P4$_0$/ P4$_1$ = Normal port 01: P4$_1$ = Normal port, P4$_0$ = XOUT 10: P4$_1$ = Normal port, P4$_0$ = XCOUT 11: P4$_1$ = XCOUT, P4$_0$ = XOUT	0	RW
1			0	RW
2	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.40 Structure of Oscillation output control register

PULL register



PULL register (PULL)

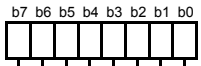
[Address 0FF1$_{16}$]

b	Name	Functions	At reset	RW
0	Ports P3$_0$ to P3$_3$ pull-up control	0 : No pull-up 1 : Pull-up	0	RW
1	Ports P3$_4$ to P3$_7$ pull-up control	0 : No pull-up 1 : Pull-up	0	RW
2	Ports P4$_0$ to P4$_3$ pull-up control	0 : No pull-up 1 : Pull-up	0	RW
3	Ports P4$_4$ to P4$_7$ pull-up control	0 : No pull-up 1 : Pull-up	0	RW
4	Ports P5$_0$ to P5$_3$ pull-up control	0 : No pull-up 1 : Pull-up	0	RW
5	Ports P5$_4$ to P5$_7$ pull-up control	0 : No pull-up 1 : Pull-up	0	RW
6	Ports P6$_0$ to P6$_2$ pull-up control	0 : No pull-up 1 : Pull-up	0	RW
7	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO

Note: In ports set to output mode, this bit becomes invalid and pull-up resistor is not connected.

Fig. 4.41 Structure of PULL register

Key input control register



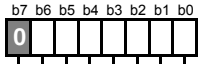
Key input control register (KIC)

[Address 0FF2$_{16}$]

b	Name	Functions	At reset	RW
0	Port P5$_4$ key input control bit	0 : Key input interrupt disabled 1 : Key input interrupt enabled	0	RW
1	Port P5$_5$ key input control bit	0 : Key input interrupt disabled 1 : Key input interrupt enabled	0	RW
2	Port P5$_6$ key input control bit	0 : Key input interrupt disabled 1 : Key input interrupt enabled	0	RW
3	Port P5$_7$ key input control bit	0 : Key input interrupt disabled 1 : Key input interrupt enabled	0	RW
4	Port P0$_0$ key input control bit	0 : Key input interrupt disabled 1 : Key input interrupt enabled	0	RW
5	Port P0$_1$ key input control bit	0 : Key input interrupt disabled 1 : Key input interrupt enabled	0	RW
6	Port P0$_2$ key input control bit	0 : Key input interrupt disabled 1 : Key input interrupt enabled	0	RW
7	Port P0$_3$ key input control bit	0 : Key input interrupt disabled 1 : Key input interrupt enabled	0	RW

Fig. 4.42 Structure of Key input control register

Timer 1234 mode register



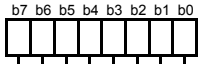
Timer 1234 mode register (T1234M)

[Address 0FF3$_{16}$]

b	Name	Functions	At reset	RW
0	T_{3OUT} output active edge switch bit	0: Start output at "L" 1: Start output at "H"	0	RW
1	T_{4OUT} output active edge switch bit	0: Start output at "L" 1: Start output at "H"	0	RW
2	Timer 3 output selection bit ($P5_2$)	0 : I/O port 1 : Timer 3 output	0	RW
3	Timer 4 output selection bit ($P5_3$)	0 : I/O port 1 : Timer 4 output	0	RW
4	Timer 2 write control bit	0 : Write data to both timer latch and timer 1 : Write data to timer latch only	0	RW
5	Timer 3 write control bit	0 : Write data to both timer latch and timer 1 : Write data to timer latch only	0	RW
6	Timer 4 write control bit	0 : Write data to both timer latch and timer 1 : Write data to timer latch only	0	RW
7	The contents are "0" at reading. If writing to these bits, write "0".		0	RO

Fig. 4.43 Structure of Timer 1234 mode register

Timer X control register



Timer X control register (TXCON)

[Address 0FF4$_{16}$]

b	Name	Functions	At reset	RW
0	Noise filter sampling clock selection bit	0 : f(XIN)/2 1 : f(XIN)/4	0	RW
1	External trigger delay time selection bits	b2 b1 0 0 : Not delayed 0 1 : (4/f(XIN)) µs 1 0 : (8/f(XIN)) µs 1 1 : (16/f(XIN)) µs	0	RW
2			0	RW
3	Timer X output control bit 1 (P51)	0 : Not used 1 : INT1 interrupt used	0	RW
4	Timer X output control bit 2 (P34)	0 : Not used 1 : INT2 interrupt used	0	RW
5	Timer X output edge switch bit	0 : Start at "L" output 1 : Start at "H" output	0	RW
6	CNTR0 active edge switch bits	This function changes according to timer X operation mode. (Refer to Table 4.2)	0	RW
7			0	RW

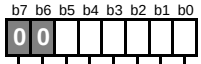
Fig. 4.44 Structure of Timer X control register

Table 4.2 CNTR1 active edge switch bit function

Timer X operation mode	Set value b7 b6	Timer function / CNTR0 pin function	CNTR0 interrupt request occurrence source
Timer mode	0 0	External interrupt pin	CNTR0 input signal falling edge (No influence to timer count)
	0 1		CNTR0 input signal rising edge (No influence to timer count)
	1 0		Input signal falling and rising edges (No influence to timer count)
	1 1		
Pulse output mode	0 0		Input signal falling edge (No influence to timer count)
	0 1		Input signal rising edges (No influence to timer count)
	1 0		Input signal falling and rising edges (No influence to timer count)
	1 1		
IGBT output mode	0 0		Input signal falling edge (No influence to timer count)
	0 1		Input signal rising edges (No influence to timer count)
	1 0		Input signal falling and rising edges (No influence to timer count)
	1 1		
PWM mode	0 0		Input signal falling edge (No influence to timer count)
	0 1		Input signal rising edges (No influence to timer count)
	1 0		Input signal falling and rising edges (No influence to timer count)
	1 1		
Event counter mode	0 0	Count at rising edge	Input signal falling edge
	0 1	Count at falling edge	Input signal rising edge
	1 0	Count at both edges	Input signal falling and rising edges
	1 1	Count at both edges	Input signal falling and rising edges
Pulse width measurement mode	0 0	Measure "H" pulse width	Input signal falling edge
	0 1	Measure "L" pulse width	Input signal rising edge
	1 0	Not available (Note)	
	1 1		

Note: In pulse width measurement mode, set bit 7 of CNTR0 active edge switch bit to "0".

Timer 12 frequency division selection register



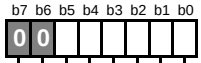
Timer 12 frequency division selection register (PRE12)

[Address 0FF5$_{16}$]

b	Name	Functions	At reset	RW
0	Timer 1 frequency division selection bits	b2 b1 b0 0 0 0 : 1/16 × f(XIN) or 1/16 × f(XCIN) 0 0 1 : 1/1 × f(XIN) or 1/1 × f(XCIN) 0 1 0 : 1/2 × f(XIN) or 1/2 × f(XCIN) 0 1 1 : 1/32 × f(XIN) or 1/32 × f(XCIN) 1 0 0 : 1/64 × f(XIN) or 1/64 × f(XCIN) 1 0 1 : 1/128 × f(XIN) or 1/128 × f(XCIN) 1 1 0 : 1/256 × f(XIN) or 1/256 × f(XCIN) 1 1 1 : 1/1024 × f(XIN) or 1/1024 × f(XCIN)	0	RW
1			0	RW
2			0	RW
3	Timer 2 frequency division selection bits	b5 b4 b3 0 0 0 : 1/16 × f(XIN) or 1/16 × f(XCIN) 0 0 1 : 1/1 × f(XIN) or 1/1 × f(XCIN) 0 1 0 : 1/2 × f(XIN) or 1/2 × f(XCIN) 0 1 1 : 1/32 × f(XIN) or 1/32 × f(XCIN) 1 0 0 : 1/64 × f(XIN) or 1/64 × f(XCIN) 1 0 1 : 1/128 × f(XIN) or 1/128 × f(XCIN) 1 1 0 : 1/256 × f(XIN) or 1/256 × f(XCIN) 1 1 1 : 1/1024 × f(XIN) or 1/1024 × f(XCIN)	0	RW
4			0	RW
5			0	RW
6	The contents are “0” at reading. If writing to these bits, write“0”.		0	RO
7			0	RO

Fig. 4.45 Structure of Timer 12 frequency division selection register

Timer 34 frequency division selection register



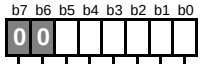
Timer 34 frequency division selection register (PRE34)

[Address 0FF6$_{16}$]

b	Name	Functions	At reset	RW
0	Timer 3 frequency division selection bits	b2 b1 b0 0 0 0 : 1/16 × f(XIN) or 1/16 × f(XCIN) 0 0 1 : 1/1 × f(XIN) or 1/1 × f(XCIN) 0 1 0 : 1/2 × f(XIN) or 1/2 × f(XCIN) 0 1 1 : 1/32 × f(XIN) or 1/32 × f(XCIN) 1 0 0 : 1/64 × f(XIN) or 1/64 × f(XCIN) 1 0 1 : 1/128 × f(XIN) or 1/128 × f(XCIN) 1 1 0 : 1/256 × f(XIN) or 1/256 × f(XCIN) 1 1 1 : 1/1024 × f(XIN) or 1/1024 × f(XCIN)	0	RW
1			0	RW
2			0	RW
3	Timer 4 frequency division selection bits	b5 b4 b3 0 0 0 : 1/16 × f(XIN) or 1/16 × f(XCIN) 0 0 1 : 1/1 × f(XIN) or 1/1 × f(XCIN) 0 1 0 : 1/2 × f(XIN) or 1/2 × f(XCIN) 0 1 1 : 1/32 × f(XIN) or 1/32 × f(XCIN) 1 0 0 : 1/64 × f(XIN) or 1/64 × f(XCIN) 1 0 1 : 1/128 × f(XIN) or 1/128 × f(XCIN) 1 1 0 : 1/256 × f(XIN) or 1/256 × f(XCIN) 1 1 1 : 1/1024 × f(XIN) or 1/1024 × f(XCIN)	0	RW
4			0	RW
5			0	RW
6	The contents are “0” at reading. If writing to these bits, write“0”.		0	RO
7			0	RO

Fig. 4.46 Structure of Timer 34 frequency division selection register

Timer XY frequency division selection register



Timer XY frequency division selection register (PREXY)

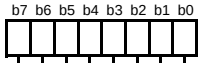
[Address 0FF7$_{16}$]

b	Name	Functions	At reset	RW
0	Timer X frequency division selection bits	b2 b1 b0 0 0 0 : 1/16 × f(XIN) or 1/16 × f(XCIN) 0 0 1 : 1/1 × f(XIN) or 1/1 × f(XCIN) 0 1 0 : 1/2 × f(XIN) or 1/2 × f(XCIN) 0 1 1 : 1/32 × f(XIN) or 1/32 × f(XCIN) 1 0 0 : 1/64 × f(XIN) or 1/64 × f(XCIN) 1 0 1 : 1/128 × f(XIN) or 1/128 × f(XCIN) 1 1 0 : 1/256 × f(XIN) or 1/256 × f(XCIN) 1 1 1 : 1/1024 × f(XIN) or 1/1024 × f(XCIN)	0	RW
1			0	RW
2			0	RW
3	Timer Y frequency division selection bits	b5 b4 b3 0 0 0 : 1/16 × f(XIN) or 1/16 × f(XCIN) 0 0 1 : 1/1 × f(XIN) or 1/1 × f(XCIN) 0 1 0 : 1/2 × f(XIN) or 1/2 × f(XCIN) 0 1 1 : 1/32 × f(XIN) or 1/32 × f(XCIN) 1 0 0 : 1/64 × f(XIN) or 1/64 × f(XCIN) 1 0 1 : 1/128 × f(XIN) or 1/128 × f(XCIN) 1 1 0 : 1/256 × f(XIN) or 1/256 × f(XCIN) 1 1 1 : 1/1024 × f(XIN) or 1/1024 × f(XCIN)	0	RW
4			0	RW
5			0	RW
6	The contents are “0” at reading. If writing to these bits, write“0”.		0	RO
7			0	RO

Fig. 4.47 Structure of Timer XY frequency division selection register

When port P0 direction register is set as output mode

Segment output disable register 0



Segment output disable register 0 (SEG0)

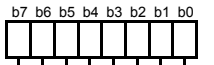
[Address 0FF8$_{16}$]

b	Name	Functions	At reset	RW
0	Segment output disable bit 0	0 : Segment output SEG0 1 : Output ports P00	1	RW
1	Segment output disable bit 1	0 : Segment output SEG1 1 : Output ports P01	1	RW
2	Segment output disable bit 2	0 : Segment output SEG2 1 : Output ports P02	1	RW
3	Segment output disable bit 3	0 : Segment output SEG3 1 : Output ports P03	1	RW
4	Segment output disable bit 4	0 : Segment output SEG4 1 : Output ports P04	1	RW
5	Segment output disable bit 5	0 : Segment output SEG5 1 : Output ports P05	1	RW
6	Segment output disable bit 6	0 : Segment output SEG6 1 : Output ports P06	1	RW
7	Segment output disable bit 7	0 : Segment output SEG7 1 : Output ports P07	1	RW

Fig. 4.48 Structure of Segment output disable register 0

When port P1 direction register is set as output mode

Segment output disable register 1



Segment output disable register 1 (SEG1)

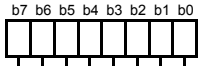
[Address 0FF9$_{16}$]

b	Name	Functions	At reset	RW
0	Segment output disable bit 8	0 : Segment output SEG$_8$ 1 : Output ports P1$_0$	1	RW
1	Segment output disable bit 9	0 : Segment output SEG$_9$ 1 : Output ports P1$_1$	1	RW
2	Segment output disable bit 10	0 : Segment output SEG$_{10}$ 1 : Output ports P1$_2$	1	RW
3	Segment output disable bit 11	0 : Segment output SEG$_{11}$ 1 : Output ports P1$_3$	1	RW
4	Segment output disable bit 12	0 : Segment output SEG$_{12}$ 1 : Output ports P1$_4$	1	RW
5	Segment output disable bit 13	0 : Segment output SEG$_{13}$ 1 : Output ports P1$_5$	1	RW
6	Segment output disable bit 14	0 : Segment output SEG$_{14}$ 1 : Output ports P1$_6$	1	RW
7	Segment output disable bit 15	0 : Segment output SEG$_{15}$ 1 : Output ports P1$_7$	1	RW

Fig. 4.49 Structure of Segment output disable register 1

When port P2 direction register is set as output mode

Segment output disable register 2



Segment output disable register 2 (SEG2)

[Address 0FFA$_{16}$]

b	Name	Functions	At reset	RW
0	Segment output disable bit 16	0 : Segment output SEG$_{16}$ 1 : Output ports P2$_0$	1	RW
1	Segment output disable bit 17	0 : Segment output SEG$_{17}$ 1 : Output ports P2$_1$	1	RW
2	Segment output disable bit 18	0 : Segment output SEG$_{18}$ 1 : Output ports P2$_2$	1	RW
3	Segment output disable bit 19	0 : Segment output SEG$_{19}$ 1 : Output ports P2$_3$	1	RW
4	Segment output disable bit 20	0 : Segment output SEG$_{20}$ 1 : Output ports P2$_4$	1	RW
5	Segment output disable bit 21	0 : Segment output SEG$_{21}$ 1 : Output ports P2$_5$	1	RW
6	Segment output disable bit 22	0 : Segment output SEG$_{22}$ 1 : Output ports P2$_6$	1	RW
7	Segment output disable bit 23	0 : Segment output SEG$_{23}$ 1 : Output ports P2$_7$	1	RW

Fig. 4.50 Structure of Segment output disable register 2

When port Pi (i = 0-2) direction register is set as input mode

Segment output disable register i

b7 b6 b5 b4 b3 b2 b1 b0

Segment output disable register i (SEGi) (i=0 to 2)

[Address 0FF8$_{16}$,0FF9$_{16}$,0FFA$_{16}$]

b	Name	Functions	At reset	RW
0	Port Pi$_0$ pull-up	0 : No pull-up 1 : Pull-up	1	RW
1	Port Pi$_1$ pull-up	0 : No pull-up 1 : Pull-up	1	RW
2	Port Pi$_2$ pull-up	0 : No pull-up 1 : Pull-up	1	RW
3	Port Pi$_3$ pull-up	0 : No pull-up 1 : Pull-up	1	RW
4	Port Pi$_4$ pull-up	0 : No pull-up 1 : Pull-up	1	RW
5	Port Pi$_5$ pull-up	0 : No pull-up 1 : Pull-up	1	RW
6	Port Pi$_6$ pull-up	0 : No pull-up 1 : Pull-up	1	RW
7	Port Pi$_7$ pull-up	0 : No pull-up 1 : Pull-up	1	RW

Note: In the port set as output mode, a pull-up resistor is not connected.

Fig. 4.51 Structure of Segment output disable register i (i=0 to 2)

Timer Y mode register 2

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 0 0 0 0 0

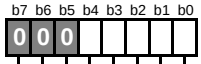
Timer Y mode register 2 (TYM2)

[Address 0FFB$_{16}$]

b	Name	Functions	At reset	RW
0	Timer Y write control bit	0 : Write data to both timer latch and timer 1 : Write data to timer latch only	0	RW
1	The contents are “0” at reading. If writing to these bits, write“0”.		0	RO
2			0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.52 Structure of Timer Y mode register 2

Flash memory control register



Flash memory control register (FMCR)

[Address 0FFE16]

b	Name	Functions	At reset	RW
0	RY/$\overline{BY}$ status flag	0 : Busy (being written or erased) 1 : Ready	1	RO
1	CPU rewrite mode select bit (Note 2)	0 : Normal mode (Software commands invalid) 1 : CPU rewrite mode (Software commands acceptable)	0	RW
2	CPU rewrite mode entry flag	0 : Normal mode 1 : CPU rewrite mode	0	RO
3	Flash memory reset bit (Note 3)	0 : Normal operation 1 : Reset	0	RW
4	User area / Boot area select bit	0 : User ROM area accessed 1 : Boot ROM area accessed	0	RW
5	The contents are undefined at reading. If writing to this bit, write “0”.		Undefined	-
6			Undefined	-
7			Undefined	-

Notes:
1. The contents of flash memory control register are “XXX00001” just after reset release.
2. For this bit to be set to “1”, the user needs to write “0” and then “1” to it in succession. Use the control program in the RAM for write to this bit.
3. This bit is valid when the CPU rewrite mode select bit is “1”. Set this bit 3 to “0” subsequently after setting bit 3 to “1”.

Fig. 4.53 Structure of Flash memory control register

5. Reference

Renesas Technology Corporation Semiconductor Home Page
http://www.renesas.com

E-mail Support
E-mail:support_apl@renesas.com

Data Sheet
38C2 Group (A version) Data sheet
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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.20.04	—	First edition issued

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