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April 1st, 2010
Renesas Electronics Corporation

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38C2 Group

LCD Drive Control Circuit (Internal Dividing Resistor Usage-1)

1. Abstract

The following article introduces and shows an example of how to use the LCD Drive Control Circuit (Internal Dividing Resistor Usage-1) on the 38C2 group device.

2. Introduction

The explanation of this issue is applied to the following condition:

Applicable MCU: 38C2 Group

Oscillation frequency: 8MHz

In this sample program, the bit of the function which is not used may be operated on account of bit arrangement of SFR. Please set these setting values according to the use situation of a user system.

3. Contents

3.1 LCD Panel Display (Use of Internal Dividing Resistor: VL1, VL2=output)

Outline: The LCD panel is displayed by using the LCD drive control circuit.

Specifications:

- Segment output SEG0-SEG13 and common COM0-COM3 are used.
- Frame frequency=61Hz
- VL2 pin is used as P27 and VL1 pin is used as P26.
- Duty ratio number=4, Bias value=1/3
- Waveform type B
- Internal dividing resistor is used
- “M38C2” is displayed

Figure 3.1 shows a Segment Allocation Example; Figure 3.2 shows the Circuit Example (When Using Internal Dividing Resistor); Figure 3.3 shows the LCD Display RAM Map; Figure 3.4 shows a LCD Display RAM Setting Example; Figures 3.5 and 3.6 show the Relevant Registers Setting; Figure 3.7 shows the Control Procedure.

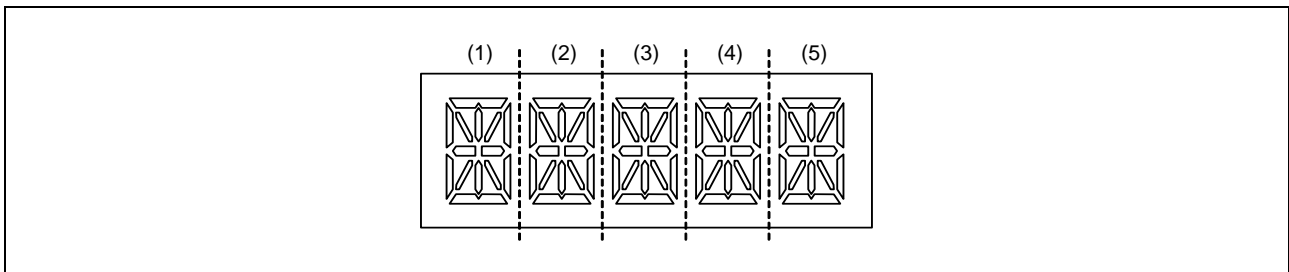


Figure 3.1 Segment Allocation Example

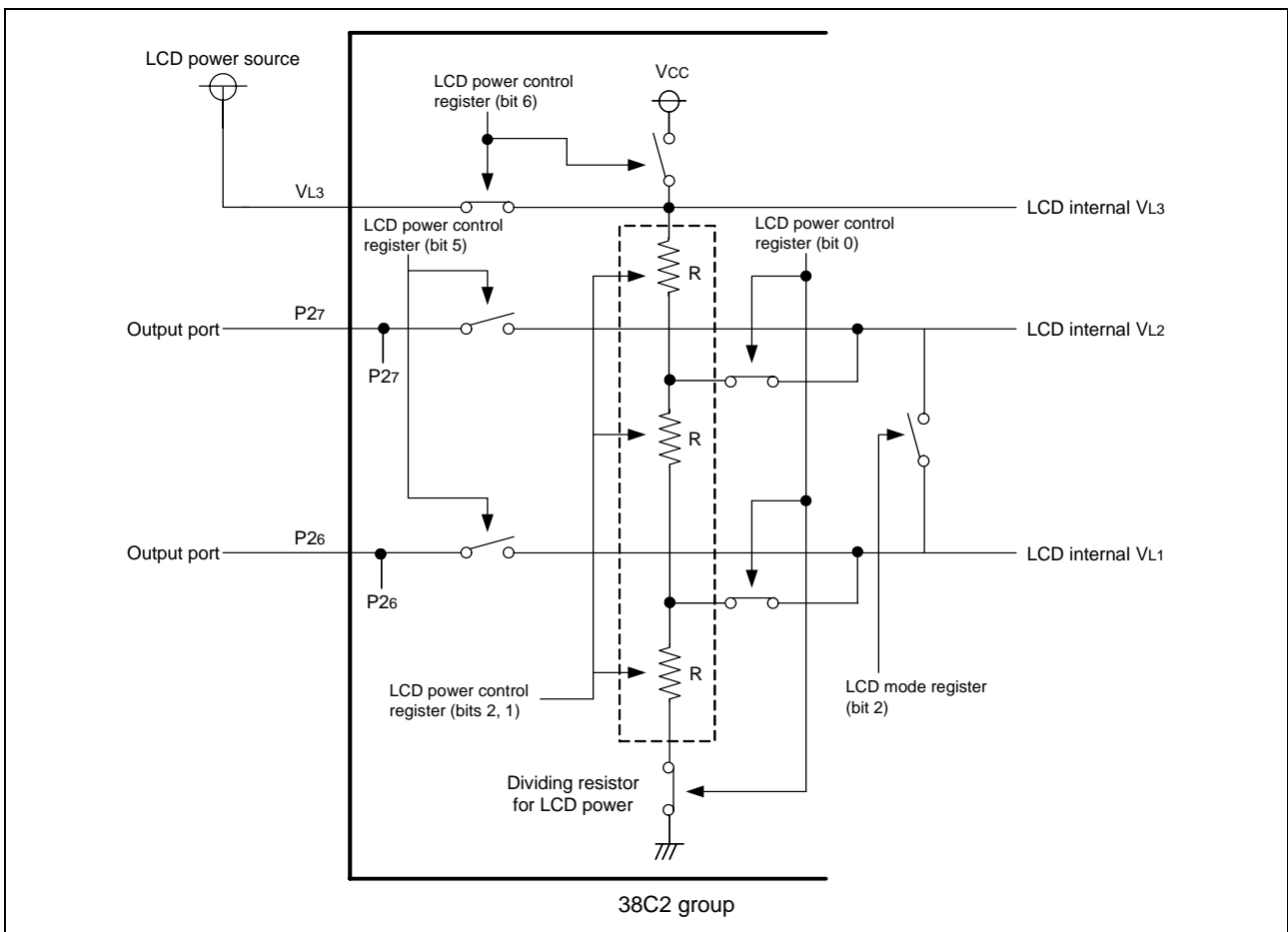


Figure 3.2 Circuit Example (When Using Internal Dividing Resistor)

Address		Bit							
		7	6	5	4	3	2	1	0
		COM ₃	COM ₂	COM ₁	COM ₀	COM ₃	COM ₂	COM ₁	COM ₀
Address 0040 ₁₆	LRAM0	SEG ₁				SEG ₀			
Address 0041 ₁₆	LRAM1	SEG ₃				SEG ₂			
Address 0042 ₁₆	LRAM2	SEG ₅				SEG ₄			
Address 0043 ₁₆	LRAM3	SEG ₇				SEG ₆			
Address 0044 ₁₆	LRAM4	SEG ₉				SEG ₈			
Address 0045 ₁₆	LRAM5	SEG ₁₁				SEG ₁₀			
Address 0046 ₁₆	LRAM6	SEG ₁₃				SEG ₁₂			
Address 0047 ₁₆	LRAM7	SEG ₁₅				SEG ₁₄			
Address 0048 ₁₆	LRAM8	SEG ₁₇				SEG ₁₆			
Address 0049 ₁₆	LRAM9	SEG ₁₉				SEG ₁₈			
Address 004A ₁₆	LRAM10	SEG ₂₁				SEG ₂₀			
Address 004B ₁₆	LRAM11	SEG ₂₃				SEG ₂₂			

Figure 3.3 LCD Display RAM Map

Address		Bit								Digit
		7	6	5	4	3	2	1	0	
		COM ₃	COM ₂	COM ₁	COM ₀	COM ₃	COM ₂	COM ₁	COM ₀	
Address 0040 ₁₆	LRAM0	h	g	f	e	d	c	b	a	→(1)
Address 0041 ₁₆	LRAM1	n	m		l	k	j		i	→(1)
Address 0042 ₁₆	LRAM2	h	g	f	e	d	c	b	a	→(2)
Address 0043 ₁₆	LRAM3	n	m		l	k	j		i	→(2)
Address 0044 ₁₆	LRAM4	h	g	f	e	d	c	b	a	→(3)
Address 0045 ₁₆	LRAM5	n	m		l	k	j		i	→(3)
Address 0046 ₁₆	LRAM6	h	g	f	e	d	c	b	a	→(4)
Address 0047 ₁₆	LRAM7	n	m		l	k	j		i	→(4)
Address 0048 ₁₆	LRAM8	h	g	f	e	d	c	b	a	→(5)
Address 0049 ₁₆	LRAM9	n	m		l	k	j		i	→(5)
Address 004A ₁₆	LRAM10									
Address 004B ₁₆	LRAM11									

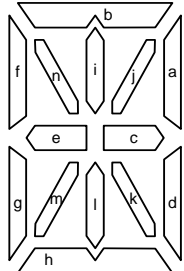


Figure 3.4 LCD Display RAM Setting Example

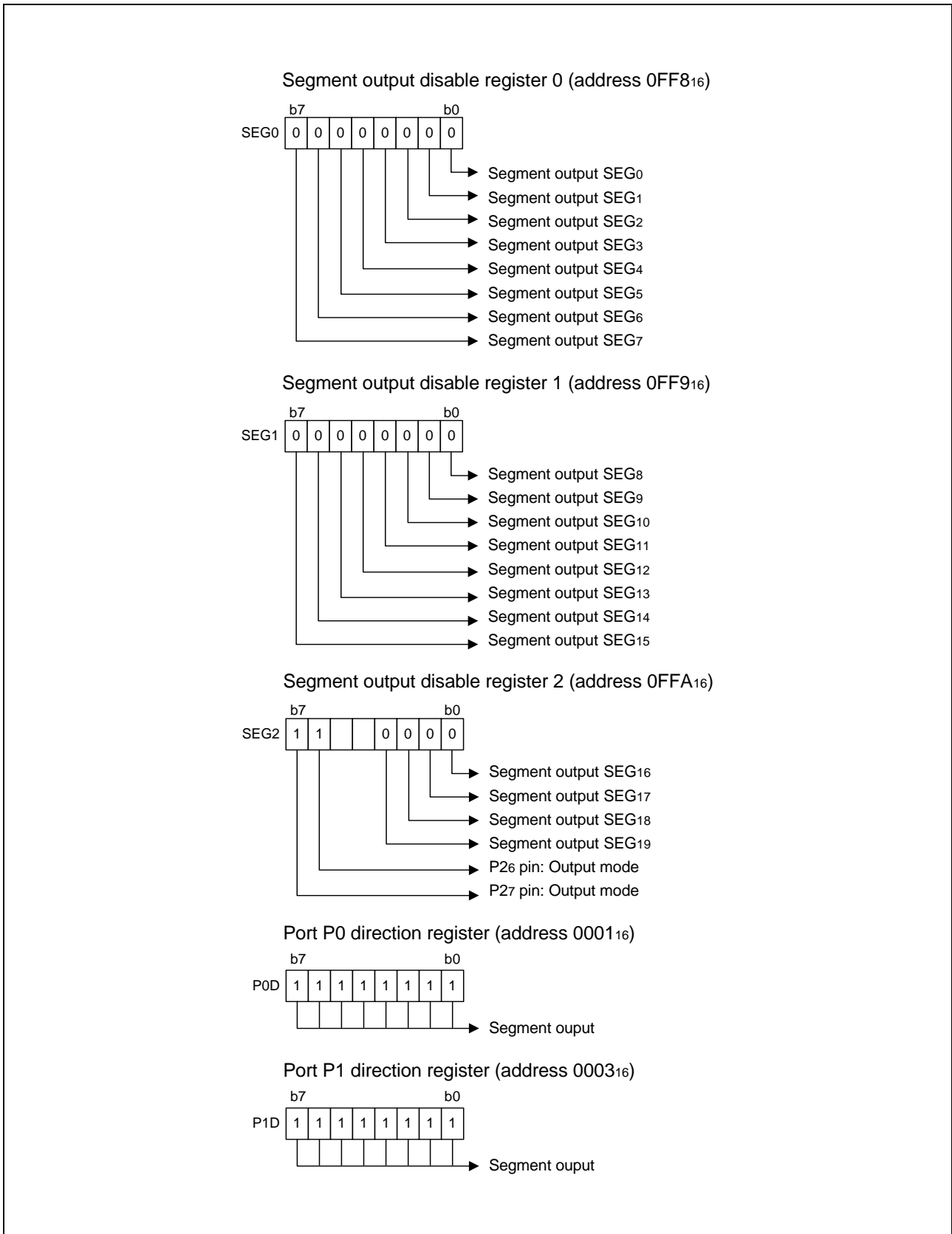
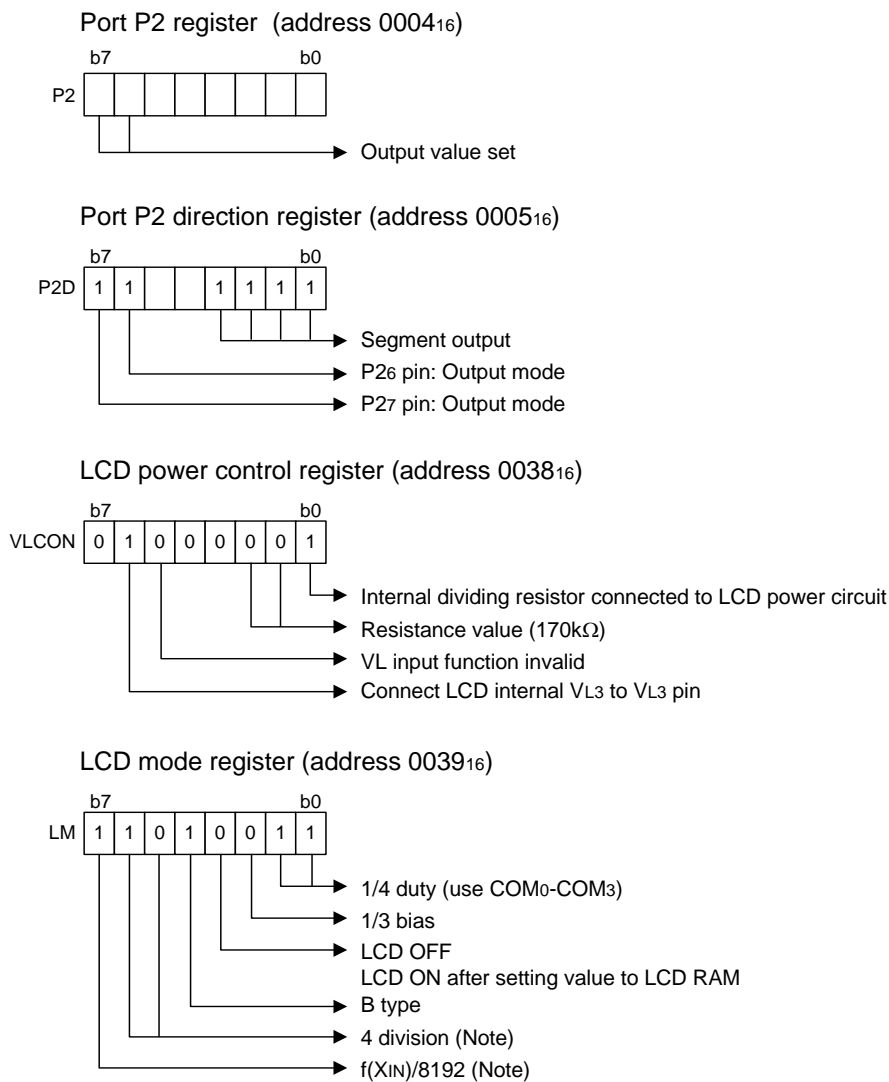


Figure 3.5 Relevant Register Setting (1)



Notes: Frame frequency= $f(\text{LCDCK})/\text{Duty ratio}$
 $f(\text{LCDCK})=\text{frequency of count source for LCDCK}/\text{Divider division ratio for LCD circuit}$
 Therefore, the frame frequency at $f(X_{IN})=8\text{MHz}$ is as follows.

$$\text{Frame frequency} = \{(8 \times 10^6 / 8192) / 4\} / 4 \approx 61.035\text{Hz}$$

	Segment output disable register		
Direction register	0	1	
0	Input port No pull-up	Input port Pull-up	← Initial status
1	Segment output	Port output	

Figure 3.6 Relevant Register Setting (2)

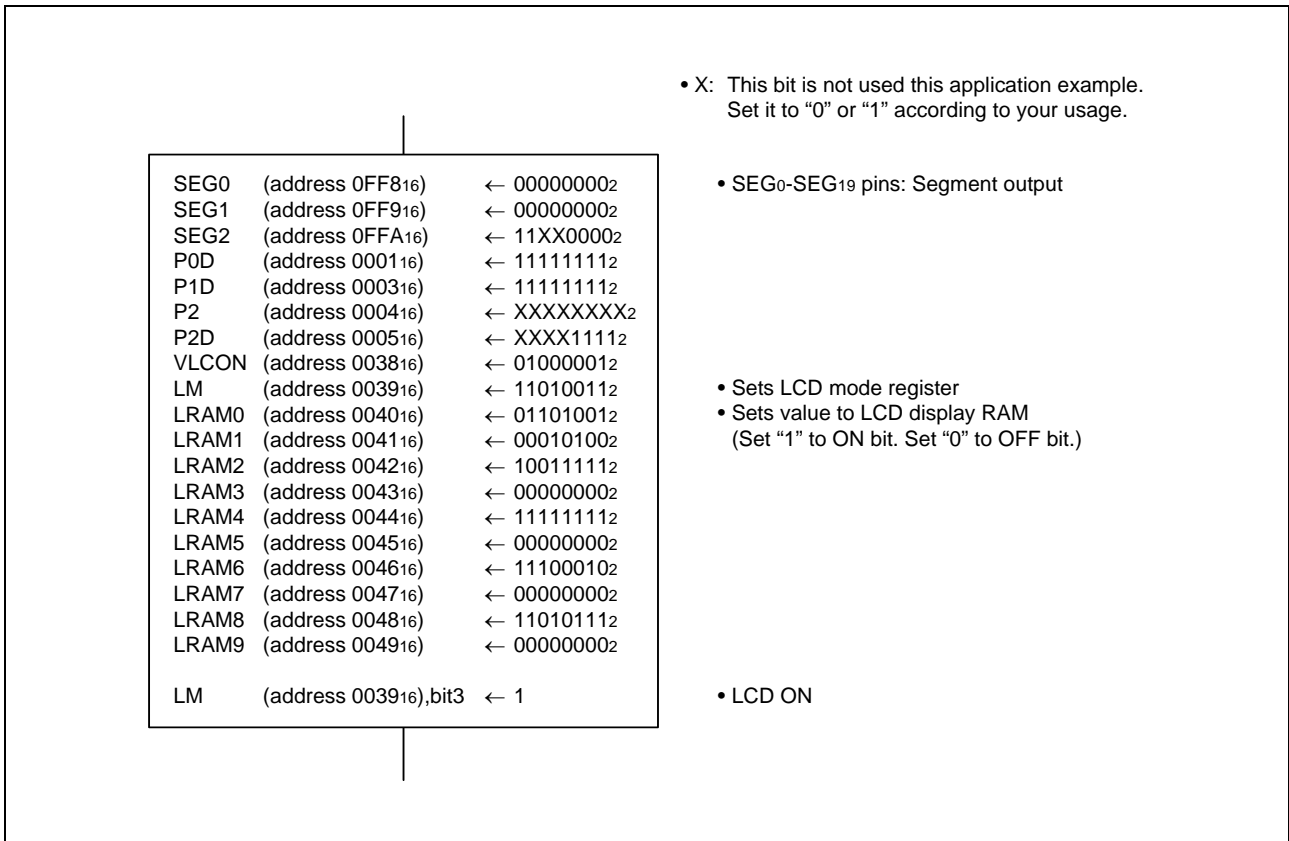


Figure 3.7 Control Procedure

4. Sample Programming Code

```
[Main processing]
__MAIN:
    LDA  #00000000          ;Set Segment output disable register 0
    STA  SEG0
    LDA  #00000000          ;Set Segment output disable register 1
    STA  SEG1
    LDA  #11110000          ;Set Segment output disable register 2
    STA  SEG2
    LDM  #11111111,P0D      ;Set Port P0 direction register
    LDM  #11111111,P1D      ;Set Port P1 direction register
    LDM  #00000000,P2       ;Set Port P2 data register
    LDM  #11111111,P2D      ;Set Port P2 direction register
    LDM  #01000001,VLCON    ;Set LCD power control register
    LDM  #11010011,LM       ;Set LCD mode register
;
    LDM  #01101001,LRAM0    ;Set LCD display RAM
    LDM  #00010100,LRAM1
    LDM  #10011111,LRAM2
    LDM  #00000000,LRAM3
    LDM  #11111111,LRAM4
    LDM  #00000000,LRAM5
    LDM  #11100010,LRAM6
    LDM  #00000000,LRAM7
    LDM  #11010111,LRAM8
    LDM  #00000000,LRAM9
;
    SEB  3,LM               ;LCD display ON
;
```

5. Reference

Renesas Technology Corporation Semiconductor Home Page
<http://www.renesas.com>

E-mail Support
E-mail: support_apl@renesas.com

Data Sheet
38C2 Group (A version) Data sheet
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REVISION HISTORY	38C2 Group LCD Drive Control Circuit (Internal Dividing Resistor Usage-1)
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Rev.	Date	Description	
		Page	Summary
1.00	Sep 25, 2004	-	First Edition issued

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