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April 1<sup>st</sup>, 2010  
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## 3850A Group

### A/D Converter

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#### 1. Abstract

This document describes the A/D conversion operation of the 3850A Group MCU.

#### 2. Introduction

This document applies to the following MCU:

- Applicable MCU: 3850A Group

### 3. Contents

#### 3.1 A/D Conversion Operation

The A/D converter starts by writing “0” to the AD conversion completion bit. Internal operations during A/D conversion are shown below:

1. The value in the A/D conversion buffer register becomes “00h” when A/D conversion starts.
2. The highest-order bit in the A/D conversion buffer register becomes “1” and comparison voltage Vref is input to a comparator. Then, Vref and analog input voltage VIN are compared.
3. If the comparison result is Vref < VIN, the highest-order bit in the A/D conversion buffer register is held as “1”. If Vref > VIN, the highest-order bit becomes “0”.

By performing the above operations to the lowest-order bit in the A/D conversion buffer register, the A/D converter converts an analog value to a digital value. A/D conversion ends in 61 cycles of 2tc(XIN) (15.25 μs when f(XIN) = 8 MHz) in high-speed and middle-speed modes and 40 μs in low-speed mode after A/D conversion starts. Then the conversion results are stored in the A/D conversion register (addresses 003516 and 003616). An A/D conversion interrupt request is generated at the same time as the A/D conversion is completed, and the A/D conversion interrupt request bit becomes “1”

\* tc(XIN) = Main clock input cycle time

Table 3.1 Relational Expression of Vref and A/D Converter Reference Voltage VREF

When n = 0	Vref = 0
When n = 1 to 1023	$V_{ref} = \frac{V_{REF}}{1024} \times n$

n: Value of A/D conversion register (decimal notation)

Table 3.2 Changes of A/D Conversion Buffer Register During A/D Conversion

	Changes in the A/D conversion buffer register <sup>(1)</sup>	Comparison voltage (Vref) value
Conversion starts	0 0 0 0 0 0 0 0 0 0	0
First comparison	1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2}$
Second comparison	* 1 1 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4}$
Third comparison	* 1 2 1 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8}$
⋮	⋮	⋮
Tenth comparison completed	A/D conversion result * 1 2 3 4 5 6 7 8 9 10	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \dots \pm \frac{V_{REF}}{1024}$

\*1 to \*10: Comparison results of 1 to 10

Note:

1. The A/D conversion buffer register is in the A/D converter. Changes cannot be seen in the middle of comparisons.

Figure 3.1 shows an A/D Converter Equivalent Circuit and Figure 3.2 shows an A/D Conversion Timing Chart.

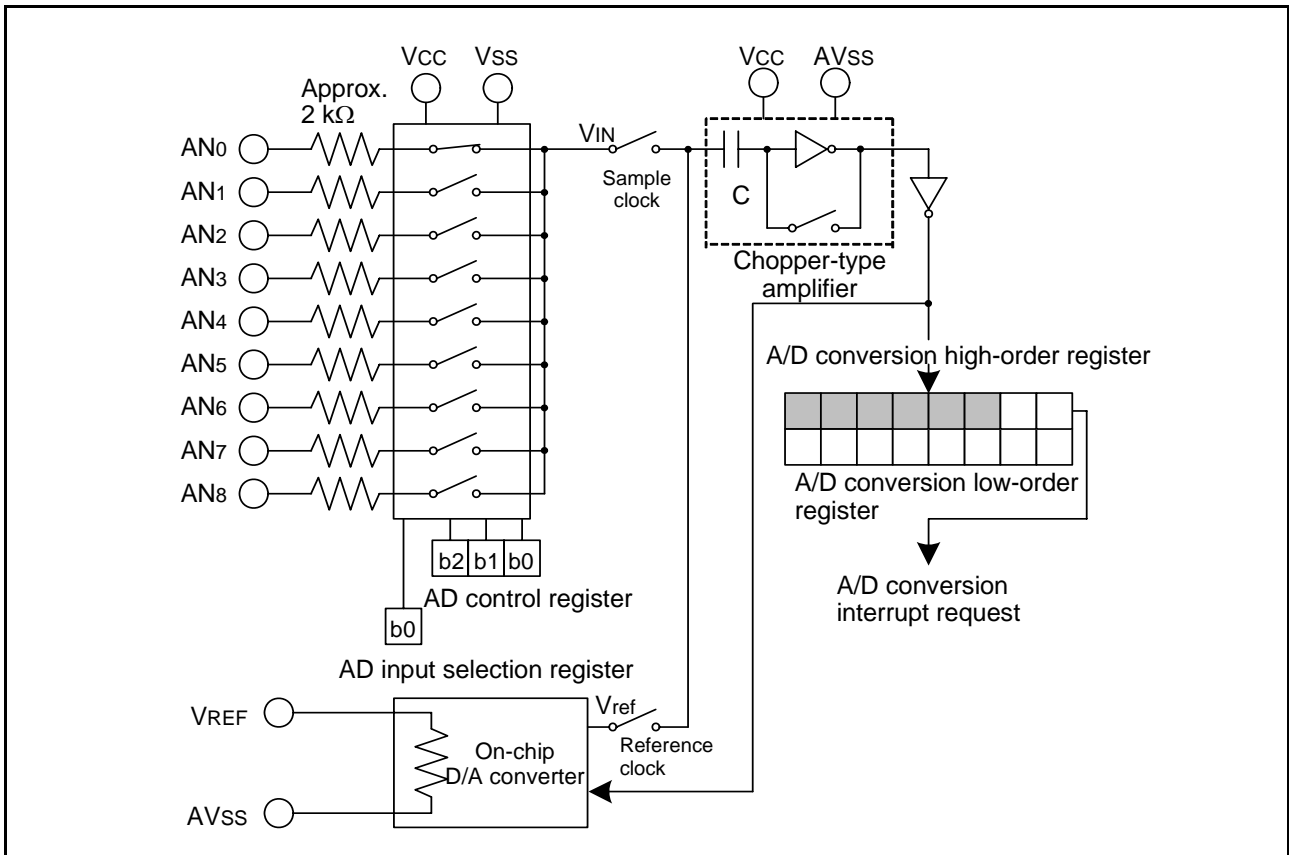


Figure 3.1 A/D Converter Equivalent Circuit

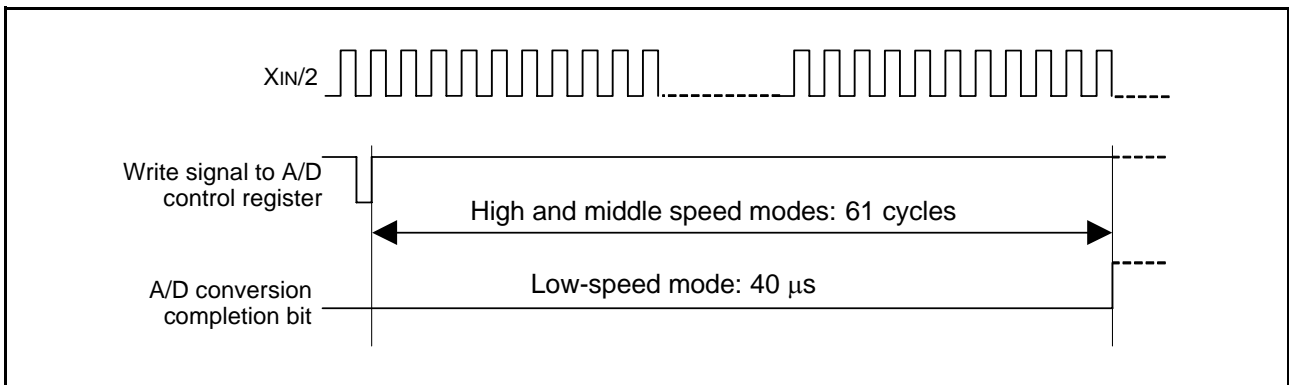


Figure 3.2 A/D Conversion Timing Chart

#### 4. Reference Document

Datasheet

3850 Group (Spec. A) Datasheet

3850 Group (Spec. A QzROM version) Datasheet

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REVISION HISTORY	3850A Group A/D Converter
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Rev.	Date	Description	
		Page	Summary
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