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3823 Group
List of Registers

1. Abstract

The following article introduces and shows the SFR registers of the 3823 Group.

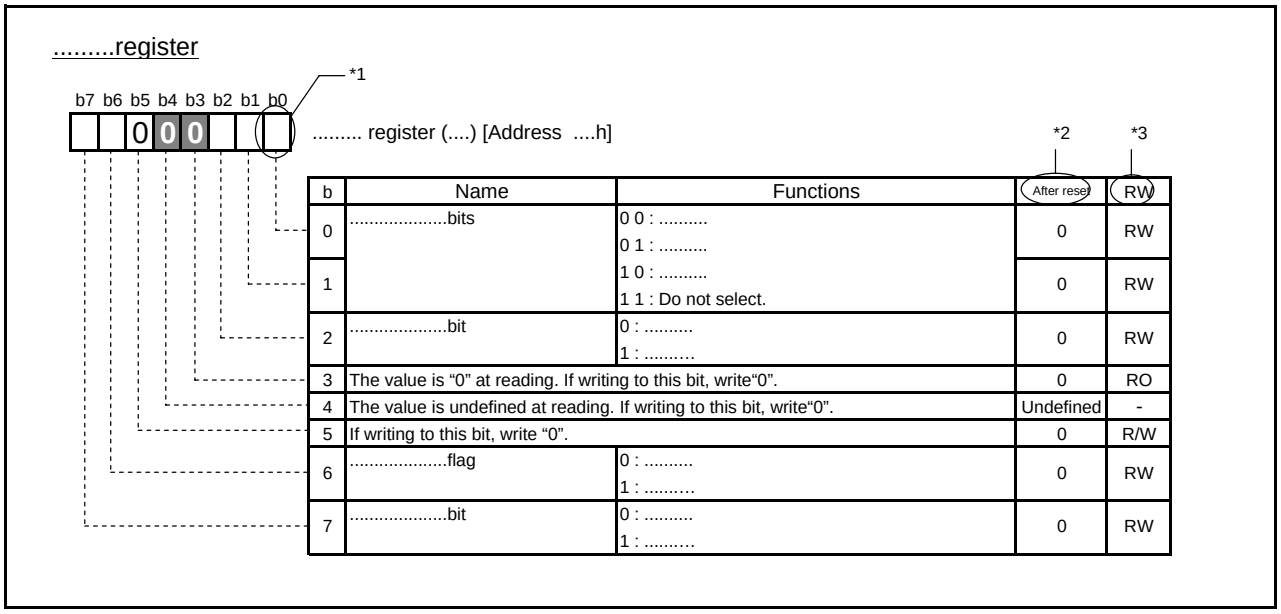
2. Introduction

The explanation of this issue is applied to the following MCU:

Applicable MCU: 3823 Group

3. Structure of Register

The following is an example of the SFR register structure figure used in this application note and definitions of codes or abbreviations used in this figure are explained below.



b	Name	Functions	After reset	RW
0	.....bits	0 0 : ..... 0 1 : ..... 1 0 : ..... 1 1 : Do not select.	0	RW
1			0	RW
2	.....bit	0 : ..... 1 :	0	RW
3	The value is “0” at reading. If writing to this bit, write“0”.		0	RO
4	The value is undefined at reading. If writing to this bit, write“0”.		Undefined	-
5	If writing to this bit, write “0”.		0	R/W
6	.....flag	0 : ..... 1 :	0	RW
7	.....bit	0 : ..... 1 :	0	RW

*1

Blank	: Set “1” or “0” to this bit according to use.
0	: If writing to this bit, write "0".
1	: If writing to this bit, write "1".
×	: This bit is not used in the specific mode or state.
	: Nothing is arranged for this bit.

*2

0	: “0” after reset
1	: “1” after reset
Undefined	: Undefined after reset

*3

RW	: Read enabled. Write enabled.
RO	: Read enabled. This value depends on each bit at writing.
WO	: Write enabled. Undefined at reading.
-	: Undefined at reading. This value depends on each bit at writing.

4. List of Registers

Port Pi register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi register (Pi) (i = 0 to 2, 5 to 6)

[addresses 0000h, 0002h, 0004h, 000Ah, 000Ch]

b	Name	Functions	After reset	RW
0	Port Pi_0	•In output mode Write •••••••• Port latch Read •••••••• Port latch or output of peripheral functions (Note) •In input mode Write •••••••• Port latch Read •••••••• Value of pin	Undefined	RW
1	Port Pi_1		Undefined	RW
2	Port Pi_2		Undefined	RW
3	Port Pi_3		Undefined	RW
4	Port Pi_4		Undefined	RW
5	Port Pi_5		Undefined	RW
6	Port Pi_6		Undefined	RW
7	Port Pi_7		Undefined	RW

Note: The output value is read when shared output function is selected at the following ports.
$P5_2$/RTP_0, $P5_3$/RTP_1, $P5_4$/$CNTR_0$, $P5_6$/T_{OUT}

Fig. 4.1 Structure of Port Pi register (i = 0 to 2, 5 to 6)

Port Pi direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (PiD) (i = 2, 5, 6)

[addresses 0005h, 000Bh, 000Dh]

b	Name	Functions	After reset	RW
0	Port Pi_0 direction register	0 : Input mode 1 : Output mode	0	WO
1	Port Pi_1 direction register	0 : Input mode 1 : Output mode	0	WO
2	The value is undefined at reading. If writing to this bit,	0 : Input mode 1 : Output mode	0	WO
3	Port Pi_3 direction register	0 : Input mode 1 : Output mode	0	WO
4	Port Pi_4 direction register	0 : Input mode 1 : Output mode	0	WO
5	Port Pi_5 direction register	0 : Input mode 1 : Output mode	0	WO
6	Port Pi_6 direction register	0 : Input mode 1 : Output mode	0	WO
7	Port Pi_7 direction register	0 : Input mode 1 : Output mode	0	WO

Note: In port(s) set to output mode, the corresponding pull-up control bit(s) become invalid and pull-up resistor is not connected.

Fig. 4.2 Structure of Port Pi direction register (i = 2, 5, 6)

Port Pi direction register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	

Port Pi direction register (PiD) (i = 0, 1)

[addresses 0001h, 0003h]

b	Name	Functions	After reset	RW
0	Port Pi_0 to Pi_7 direction register	0 : Input mode 1 : Output mode	0	WO
1	The values are “0” at reading. If writing to these bits, write “0”.		0	RO
2			0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Note: In port(s) set to output mode, the corresponding pull-down control bit(s) become invalid and pull-down resistor is not connected.

Fig. 4.3 Structure of Port Pi direction register (i = 0, 1)

Port P3 register

b7	b6	b5	b4	b3	b2	b1	b0
				0	0	0	0

Port P3 register (P3)

[address 0006h]

b	Name	Functions	After reset	RW
0	The values are "0" at reading. If writing to these bits, write “0”.		0	RO
1			0	RO
2			0	RO
3			0	RO
4	Port $P3_4$	The value is the value of each pin at reading. If writing to these bits, write “0”.	Undefined	RO
5	Port $P3_5$		Undefined	RO
6	Port $P3_6$		Undefined	RO
7	Port $P3_7$		Undefined	RO

Fig. 4.4 Structure of Port P3 register

Port P4 register

b7 b6 b5 b4 b3 b2 b1 b0

Port P4 register (P4)

[address 0008h]

b	Name	Functions	After reset	RW
0	Port $P4_0$	The value is the value of the pin at reading. If writing to this bit, write "0".	Undefined	RO
1	Port $P4_1$	• In output mode	Undefined	RW
2	Port $P4_2$	Write •••••••• Port latch	Undefined	RW
3	Port $P4_3$	Read •••••••• Port latch or output of	Undefined	RW
4	Port $P4_4$	peripheral functions (Note)	Undefined	RW
5	Port $P4_5$	• In input mode	Undefined	RW
6	Port $P4_6$	Write •••••••• Port latch	Undefined	RW
7	Port $P4_7$	Read •••••••• Value of pin	Undefined	RW

Note: The output value is read when shared output function is selected at $P4_1/\phi$.

Fig. 4.5 Structure of Port P4 register

Port P4 direction register

b7 b6 b5 b4 b3 b2 b1 b0

0

Port P4 direction register (P4D)

[address 0009h]

b	Name	Functions	After reset	RW
0	The value is "0" at reading. If writing to this bit, write "0".		0	RO
1	Port $P4_1$ direction register	0 : Input mode 1 : Output mode	0	WO
2	Port $P4_2$ direction register	0 : Input mode 1 : Output mode	0	WO
3	Port $P4_3$ direction register	0 : Input mode 1 : Output mode	0	WO
4	Port $P4_4$ direction register	0 : Input mode 1 : Output mode	0	WO
5	Port $P4_5$ direction register	0 : Input mode 1 : Output mode	0	WO
6	Port $P4_6$ direction register	0 : Input mode 1 : Output mode	0	WO
7	Port $P4_7$ direction register	0 : Input mode 1 : Output mode	0	WO

Notes: 1. Output structure of pin(s) at port $P4_5$ and $P4_7$ can be selected at $P4_5$/TxD, $P4_7/\overline{SRDY}/S_{OUT}$ P-channel output disable bit (bit 4 at UART control register (address 001Bh)) and P-channel output disable selection bit (bits 2 and 3 at peripheral function expansion register (address 0030h)).

2. In port(s) set to output mode, the corresponding pull-up control bit(s) become invalid and pull-up resistor is not connected.

Fig. 4.6 Structure of Port P4 direction register

Port P7 register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

Port P7 register (P7)

[address 000Eh]

b	Name	Functions	After reset	RW
0	Port $P7_0$	•In output mode Write •••••••• Port latch Read •••••••• Port latch	Undefined	RW
1	Port $P7_1$	•In input mode Write •••••••• Port latch Read •••••••• Value of pin	Undefined	RW
2	The values are "0" at reading. If writing to these bits, write “0”.		0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Fig.4.7 Structure of Port P7 register

Port P7 direction register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

Port P7 direction register (P7D)

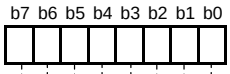
[address 000Fh]

b	Name	Functions	After reset	RW
0	Port $P7_0$ direction register	0 : Input mode 1 : Output mode	0	WO
1	Port $P7_1$ direction register	0 : Input mode 1 : Output mode	0	WO
2	The values are “0” at reading. If writing to these bits, write “0”.		0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Note: In port(s) set to output mode, the corresponding pull-up control bit(s) become invalid and pull-up resistor is not connected.

Fig.4.8 Structure of Port P7 direction register

ROM correction address 1 high-order register, ROM correction address 1 low-order register



ROM correction address 1 high-order register (RCA1H) [address 0010h]

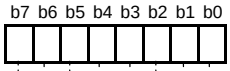
ROM correction address 1 low-order register (RCA1L) [address 0011h]

b	Functions	After reset	RW
0	This register sets the start address of the program to be corrected.	Undefined	RW
1		Undefined	RW
2		Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Notes: 1. Specify the start address of each instruction (operation code address) as ROM correction address.
2. Do not set any addresses other than those located in the ROM area to ROM correction address registers. Do not set the same addresses to both ROM correction address 1 registers and ROM correction address 2 registers.

Fig.4.9 Structure of ROM correction address 1 high-order register, ROM correction address 1 low-order register

ROM correction address 2 high-order register, ROM correction address 2 low-order register



ROM correction address 2 high-order register (RCA2H) [address 0012h]

ROM correction address 2 low-order register (RCA2L) [address 0013h]

b	Functions	After reset	RW
0	This register sets the start address of the program to be corrected.	Undefined	RW
1		Undefined	RW
2		Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Notes: 1. Specify the start address of each instruction (operation code address) as ROM correction address.
2. Do not set any addresses other than those located in the ROM area to ROM correction address registers. Do not set the same addresses to both ROM correction address 1 registers and ROM correction address 2 registers.

Fig.4.10 Structure of ROM correction address 2 high-order register, ROM correction address 2 low-order register

ROM correction enable register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 0 0 0 ROM correction enable register (RCR)

[address 0014h]

b	Name	Functions	After reset	RW
0	Address 1 enable bit (RC0)	0 : Disable 1 : Enable	0	RW
1	Address 2 enable bit (RC1)	0 : Disable 1 : Enable	0	RW
2	The values are “0” at reading. If writing to these bits, write “0”.		0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Note: When using ROM correction function, make sure to enable address enable bits after setting ROM correction address registers.

Fig.4.11 Structure of ROM correction enable register

PULL register A

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 | | | | | |

PULL register A (PULLA)

[address 00hh]

b	Name	Functions	After reset	RW
0	Port $P0_0$ to $P0_7$ pull-down control bit (Note 1)	0 : No pull-down 1 : Pull-down	1	RW
1	Port $P1_0$ to $P1_7$ pull-down control bit (Note 1)	0 : No pull-down 1 : Pull-down	1	RW
2	Port $P2_0$ to $P2_7$ pull-up control bit (Note 2)	0 : No pull-up 1 : Pull-up	0	RW
3	Port $P3_4$ to $P3_7$ pull-down control bit (Note 1)	0 : No pull-down 1 : Pull-down	1	RW
4	Port $P7_0$, $P7_1$ pull-up control bit (Note 2)	0 : No pull-up 1 : Pull-up	0	RW
5	The values are "0" at reading. If writing to these bits, write "0".		0	RO
6			0	RO
7			0	RO

Notes: 1. In port(s) set to output mode, the corresponding bit(s) become invalid and pull-down resistor is not connected. Also, when each pin at segment output enable bits 0 to 5 (bit 0 to 5 at segment output enable register (address 0038h)) is set to "1" (segment output), the corresponding bit becomes invalid and pull-down resistor is not connected.

2. In port(s) set to output mode, the corresponding bit(s) become invalid and pull-up resistor is not connected.

Fig. 4.12 Structure of PULL register A

PULL register B

b7 b6 b5 b4 b3 b2 b1 b0
0 0 | | | | | | |

PULL register B (PULLB)

[address 0017h]

b	Name	Functions	After reset	RW
0	Port $P4_1$ to $P4_3$ pull-up control bit	0 : No pull-up 1 : Pull-up	0	RW
1	Port $P4_4$ to $P4_7$ pull-up control bit	0 : No pull-up 1 : Pull-up	0	RW
2	Port $P5_0$ to $P5_3$ pull-up control bit	0 : No pull-up 1 : Pull-up	0	RW
3	Port $P5_4$ to $P5_7$ pull-up control bit	0 : No pull-up 1 : Pull-up	0	RW
4	Port $P6_0$ to $P6_3$ pull-up control bit	0 : No pull-up 1 : Pull-up	0	RW
5	Port $P6_4$ to $P6_7$ pull-up control bit	0 : No pull-up 1 : Pull-up	0	RW
6	The values are "0" at reading. If writing to these bits, write "0".		0	RO
7			0	RO

Note: In port(s) set to output mode, the corresponding bit(s) become invalid and pull-up resistor is not connected.

Fig. 4.13 Structure of PULL register B

Transmit buffer register

b7 b6 b5 b4 b3 b2 b1 b0

Transmit buffer register (TB)

[address 0018h]

b	Functions	After reset	RW
0	Transmit data is written to this buffer register.	Undefined	WO
1	Write transmit data to this register.	Undefined	WO
2		Undefined	WO
3		Undefined	WO
4		Undefined	WO
5		Undefined	WO
6		Undefined	WO
7		Undefined	WO

Note: This register is located at the same address as receive buffer register.
This register is write-only.

Receive buffer register

b7 b6 b5 b4 b3 b2 b1 b0

Receive buffer register (RB)

[address 0018h]

b	Functions	After reset	RW
0	Receive data is read from this buffer register.	Undefined	RO
1	Read receive data from this register.	Undefined	RO
2		Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

Note: This register is located at the same address as transmit buffer register.
This register is read-only.

Fig.4.14 Structure of Transmit buffer register / Receive buffer register

Serial I/O status register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O status register (SIOSTS)

[address 0019h]

b	Name	Functions	After reset	RW
0	Transmit buffer empty flag (TBE) (Note 1)	0 : Buffer register full 1 : Buffer register empty	0	RO
1	Receive buffer full flag (RBF) (Note 1, 2)	0 : Buffer register empty 1 : Buffer register full	0	RO
2	Transmit shift completion flag (TSC) (Note 1)	0 : Transmit shift in progress 1 : Transmit shift completed	0	RO
3	Overrun error flag (OE) (Note 3)	0 : No overrun error 1 : Overrun error	0	RO
4	Parity error flag (PE) (Note 3)	0 : No parity error 1 : Parity error	0	RO
5	Framing error flag (FE) (Note 3)	0 : No framing error 1 : Framing error	0	RO
6	Summing error flag (SE) (Note 3)	0 : (OE) U (PE) U (FE) = 0 1 : (OE) U (PE) U (FE) = 1	0	RO
7	The value is "1" at reading. If writing to this bit, write "1".		1	RO

Notes: 1. If writing to these bits, write "0".
2. This bit becomes "0" when receive buffer register is read.
3. These bits become "0" by writing to this register. If writing to these bits, write "0".

Fig. 4.15 Structure of Serial I/O status register

Serial I/O control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O control register (SIOCON)

[address 001Ah]

b	Name	Functions	After reset	RW
0	BRG count source selection bit (CSS)	0 : f(XIN) (f(SUB) in low-speed Mode) (Note 1) 1 : f(XIN)/4 (f(SUB)/4 in low-speed Mode) (Note 1)	0	RW
1	Serial I/O synchronous clock selection bit (SCS)	In clock synchronous serial I/O Mode 0 : BRG output divided by 4 1 : External clock input In UART Mode 0 : BRG output divided by 16 1 : External clock input divided by 16	0	RW
2	$\overline{SRDY}$, SOUT output enable bit (SRDY)	0 : Output disabled (P47 pin : I/O port) 1 : Output enabled (P47 pin : $\overline{SRDY}$, SOUT output) (Note 2)	0	RW
3	Transmit interrupt source selection bit (TIC)	0 : When the transmit buffer has become empty (TBE=1) 1 : When transmit shift operation is completed (TSC=1)	0	RW
4	Transmit enable bit (TE)	0 : Transmission disabled 1 : Transmission enabled	0	RW
5	Receive enable bit (RE)	0 : Reception disabled 1 : Reception enabled	0	RW
6	Serial I/O mode selection bit (SIOM)	0 : UART Mode 1 : Clock synchronous serial I/O Mode	0	RW
7	Serial I/O enable bit (SIOE)	0 : Serial I/O disabled (Pins P44 to P47 : I/O ports) 1 : Serial I/O enabled (Pins P44 to P47 : Serial I/O pins)	0	RW

Notes: 1. f(SUB) is the source oscillation frequency in low-speed mode and shows the oscillation frequency of XCIN or on-chip oscillator.

2. When selecting SOUT output, set the synchronous serial I/O output pin selection bit (bit 1 at peripheral function expansion register (0030h)) to "1".
When disabling transmission while selecting SOUT, set transmit enable bit and $\overline{SRDY}$, SOUT output enable bit to "0".
When selecting $\overline{SRDY}$ output, set synchronous serial I/O output pin selection bit (bit 1 at peripheral function expansion register (0030h)) to "0".

Fig. 4.16 Structure of Serial I/O control register

UART control register

b7 b6 b5 b4 b3 b2 b1 b0
1 1 1

UART control register (UARTCON)
[address 001Bh]

b	Name	Functions	After reset	RW
0	Character length selection bit (CHAS)	0 : 8 bits 1 : 7 bits	0	RW
1	Parity enable bit (PARE)	0 : Parity checking disabled 1 : Parity checking enabled	0	RW
2	Parity selection bit (PARS)	0 : Even parity 1 : Odd parity	0	RW
3	Stop bit length selection bit (STPS)	0 : 1 stop bit 1 : 2 stop bits	0	RW
4	$P4_5$/TxD, $P4_7$/$\overline{SRDY}$/SOUT P-channel output disable bit (POFF) (Note)	In output mode 0 : CMOS output 1 : N-channel open drain output In input mode, this bit is invalid.	0	RW
5	The values are "1" at reading. If writing to these bits, write "1".		1	RO
6			1	RO
7			1	RO

Note: Set this bit to "1" after selecting the pin to disable P-channel output at P-channel output disable selection bits (bits 3 and 2 at peripheral function expansion register (address 0030h)).

Fig. 4.17 Structure of UART control register

Baud rate generator

b7 b6 b5 b4 b3 b2 b1 b0

Baud rate generator (BRG)
[address 001Ch]

b	Functions	After reset	RW
0	Set the frequency divide value of BRG count source. BRC count source is divided by "n+1" when a set value is "n".	Undefined	RW
1		Undefined	RW
2		Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Note: Write to this register only while transmit/receive operation is stopped.

Fig.4.18 Structure of Baud rate generator

Timer X high-order register , Timer X low-order register

b7 b6 b5 b4 b3 b2 b1 b0

Timer X high-order register (TXH) [address 0021h]

Timer X low-order register (TXL) [address 0020h]

b	Functions	After reset	RW
0	Set the count initial value. These registers count "n+1" times, when a set value is "n". [At writing] Depending on the timer X write control bit, these registers operate as follows. •When Timer X write control bit = "0" Write value in both timer X latch and timer X simultaneously. •When Timer X write control bit = "1" Write value in timer X latch only. Write value from TXL to TXH. This operation is not affected by the timer X stop control bit. [At reading] The value is the count value of timer X at reading. Read value from TXH to TXL.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Note: When underflow and writing to high-order timer latch occur almost at the same time while selecting writing to timer latch only, the value is set to timer and timer latch simultaneously. At this time, any unexpected values may be set to high-order timer.

Fig.4.19 Structure of Timer X high-order register , Timer X low-order register

Timer Y high-order register , Timer Y low-order register

b7 b6 b5 b4 b3 b2 b1 b0

Timer Y high-order register (TYH) [address 0023h]

Timer Y low-order register (TYL) [address 0022h]

b	Functions	After reset	RW
0	Set the count initial value. These registers count "n+1" times, when the set value is "n". [At writing] Write value in both timer Y latch and timer Y simultaneously. Write value from TYL to TYH. [At reading] The value is the count value of timer Y at reading. Read value from TYH to TYL.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig.4.20 Structure of Timer Y high-order register, Timer Y low-order register

Timer 1 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 1 register (T1)

[address 0024h]

b	Functions	After reset	RW
0	Set the count initial value.	1	RW
1	This register counts "n+1" times, when the set value is "n".	1	RW
2	[At writing]	1	RW
3	Write value in both timer 1 latch and timer 1 simultaneously.	1	RW
4	[At reading]	1	RW
5	The value is the count value of timer 1 at reading.	1	RW
6		1	RW
7		1	RW

Note: This register is used to generate waiting time at reset and exiting from stop mode.

Fig.4.21 Structure of Timer 1 register

Timer 2 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 2 register (T2)

[address 0025h]

b	Functions	After reset	RW
0	Set the count initial value. This register counts "n+1" times, when the set value is "n".	1	RW
1	[At writing] Depending on the value of Timer 2 write control bit, these registers	0	RW
2	operate as follows. •When Timer 2 write control bit = “0”	0	RW
3	Write value in both timer 2 latch and timer 2 simultaneously. •When Timer 2 write control bit = “1”	0	RW
4	Write value in timer 2 latch only. [At reading]	0	RW
5	The value is the count value of timer 2 at reading.	0	RW
6		0	RW
7		0	RW

Note: This register is used to generate waiting time at reset and exiting from stop mode.

Fig.4.22 Structure of Timer 2 register

Timer 3 register

b7 b6 b5 b4 b3 b2 b1 b0

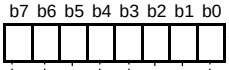
Timer 3 register (T3)

[address 0026h]

b	Functions	After reset	RW
0	Set the count initial value.	1	RW
1	This register counts "n+1" times, when the set value is "n".	1	RW
2	[At writing]	1	RW
3	Write value in both timer 3 latch and timer 3 simultaneously.	1	RW
4	[At reading]	1	RW
5	The value is the count value of timer 3 at reading.	1	RW
6		1	RW
7		1	RW

Fig.4.23 Structure of Timer 3 register

Timer X mode register



Timer X mode register (TXM)
[address 0027h]

b	Name	Functions	After reset	RW
0	Timer X write control bit	0 : Write value in both latch and timer simultaneously 1 : Write value in latch only	0	RW
1	Real time port control bit	0 : Real time port function invalid 1 : Real time port function valid	0	RW
2	RTP_0 data for real time port	0 : "L" output from $P5_2/RTP_0$ pin 1 : "H" output from $P5_2/RTP_0$ pin	0	RW
3	RTP_1 data for real time port	0 : "L" output from $P5_3/RTP_1$ pin 1 : "H" output from $P5_3/RTP_1$ pin	0	RW
4	Timer X operating mode bits	b5 b4 0 0 : Timer mode 0 1 : Pulse output mode 1 0 : Event counter mode 1 1 : Pulse width measurement mode	0	RW
5			0	RW
6	$CNTR_0$ active edge switch bit	This function changes depending on timer X operation mode (Refer to Table 4.1)	0	RW
7	Timer X stop control bit	0 : Count starts 1 : Count stops	0	RW

Fig.4.24 Structure of Timer X mode register

Table 4.1 $CNTR_0$ active edge switch bit function

Timer X operation mode	Set value	Timer function/$CNTR_0$ pin function	$CNTR_0$ Interrupt request occurrence source
Timer mode	"0"	External interrupt pin	$CNTR_0$ input signal falling edge (No influence on timer count)
	"1"		$CNTR_0$ input signal rising edge (No influence on timer count)
Pulse output mode	"0"	Pulse output start from "H"	Output signal falling edge
	"1"	Pulse output start from "L"	Output signal rising edge
Event counter mode	"0"	Count at rising edge	Input signal falling edge
	"1"	Count at falling edge	Input signal rising edge
Pulse width measurement mode	"0"	Measure "H" pulse width	Input signal falling edge
	"1"	Measure "L" pulse width	Input signal rising edge

Timer Y mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer Y mode register (TYM)

[address 0028h]

b	Name	Functions	After reset	RW
0	The values are “0” at reading. If writing to these bits, write“0”.		0	RO
1			0	RO
2			0	RO
3			0	RO
4	Time Y operating mode bits	b5 b4 0 0 : Timer mode 0 1 : Period measurement mode 1 0 : Event counter mode 1 1 : Pulse width HL continuous measurement mode	0	RW
5			0	RW
6	CNTR1 active edge switch bit	This function changes depending on timer Y operation mode (Refer to Table 4.2)	0	RW
7	Timer Y count stop bit	0 : Count starts 1 : Count stops	0	RW

Fig.4.25 Structure of Timer Y mode register

Table 4.2 CNTR1 active edge switch bit function

Timer Y operation mode	Set value	Timer function selection	CNTR1 interrupt request occurrence source
Timer mode	"0"	External interrupt pin	CNTR1 input signal falling edge (No influence on timer count)
	"1"		CNTR1 input signal rising edge (No influence on timer count)
Period measurement mode	"0"	Measure the period from falling edge to falling edge	Input signal falling edge
	"1"	Measure the period from rising edge to rising edge	Input signal rising edge
Event counter mode	"0"	Count at rising edge	Input signal falling edge
	"1"	Count at falling edge	Input signal rising edge
Pulse width HL continuous measurement mode	"0"	Measure "H" and "L" pulse width	Input signal falling and rising edges
	"1"		

Timer 123 mode register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 □ □ □ □ □ □ Timer 123 mode register (T123M)
[address 0029h]

b	Name	Functions	After reset	RW
0	T_{out} output active edge switch bit	0 : Output starts from "H" level 1 : Output starts from "L" level	0	RW
1	T_{out} output control bit	0 : T_{out} output disabled ($P5_6$ pin : I/O port) 1 : T_{out} output enabled ($P5_6$ pin : T_{out} output pin)	0	RW
2	Timer 2 write control bit	0 : Write value to both latch and timer simultaneously 1 : Write data to latch only	0	RW
3	Timer 2 count source selection bit	0 : Timer 1 output signal 1 : f(X_{IN})/16 in medium/high speed mode f(SUB)/16 in low speed mode (Note 1)	0	RW
4	Timer 3 count source selection bit	0 : Timer 1 output signal 1 : f(X_{IN})/16 in medium/high-speed mode f(SUB)/16 in low-speed mode (Note 1)	0	RW
5	Timer 1 count source selection bit	0 : f(X_{IN})/16 in medium/high-speed mode f(SUB)/16 in low-speed mode (Note 1) 1 : f(SUB) (Note 1)	0	RW
6	The values are “0” at reading. If writing to these bits, write “0”.		0	RO
7			0	RO

Notes: 1. f(SUB) is the source oscillation frequency in low-speed mode and shows the oscillation frequency of X_{CIN} or on-chip oscillator.
Internal system clock ϕ is f(SUB)/2 in low-speed mode.
2. Set the value of timer in the order of timer 1 register, timer 2 register, and timer 3 register after setting the count source of timer 1, 2 and 3.

Fig.4.26 Structure of Timer 123 mode register

ϕ output control register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0 0 0 □ ϕ output control register (CKOUT)
[address 002Ah]

b	Name	Functions	After reset	RW
0	ϕ output control bit	0 : Port function ($P4_1$ pin : I/O port) 1 : Internal system clock ϕ output, or X_{CIN} frequency signal output (Note) ($P4_1$ pin : ϕ output pin)	0	RW
1	The values are “0” at reading. If writing to these bits, write “0”.		0	RO
2			0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Note: Set output clock selection bit (bit 4 at peripheral function expansion register (address 0030h)) and port $P4_1$ direction register to "1" when X_{CIN} frequency signal is output.

Fig.4.27 Structure of ϕ output control register

CPU mode expansion register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

CPU mode expansion register (EXPCM)

[address 002Bh]

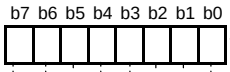
b	Name	Functions	After reset	RW
0	On-chip oscillator control bit	0 : On-chip oscillator not used 1 : On-chip oscillator used (Note 1)	0	RW
1	Frequency/4 mode control bit (Note 2)	0 : Frequency/2 mode ϕ = f(X_{IN})/2 1 : Frequency/4 mode ϕ = f(X_{IN})/4	0	RW
2	If writing to these bits, write “0”.		0	RW
3			0	RW
4			0	RW
5			0	RW
6			0	RW
7			0	RW

Note: 1. On-chip oscillator is selected as operation clock in low-speed mode regardless of X_{CIN}-X_{COUT} oscillation.

2.Valid only when the main clock division ratio selection bit (bit 6 in the CPU mode register ($003B_{16}$)) is set to “0”. When selecting f(X_{IN})/4 as system clock ϕ, set the main clock division ratio selection bit to “0” after setting this bit to “1”. When “1” (frequency/8 mode) is selected by the main clock division ratio selection bit or when the internal system clock selection bit (bit 7 in the CPU mode register) is set to “1”, set “0” to the frequency/4 mode control bit.

Fig.4.28 Structure of CPU mode expansion register

Temporary data register 0



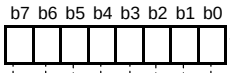
Temporary data register 0 (TD0)

[address 002Ch]

b	Functions	After reset	RW
0	DB_0 data storage	0	RW
1	DB_1 data storage	0	RW
2	DB_2 data storage	0	RW
3	DB_3 data storage	0	RW
4	DB_4 data storage	0	RW
5	DB_5 data storage	0	RW
6	DB_6 data storage	0	RW
7	DB_7 data storage	0	RW

Fig.4.29 Structure of Temporary data register 0

Temporary data register 1



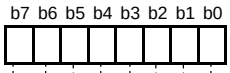
Temporary data register 1 (TD1)

[address 002Dh]

b	Functions	After reset	RW
0	DB_0 data storage	0	RW
1	DB_1 data storage	0	RW
2	DB_2 data storage	0	RW
3	DB_3 data storage	0	RW
4	DB_4 data storage	0	RW
5	DB_5 data storage	0	RW
6	DB_6 data storage	0	RW
7	DB_7 data storage	0	RW

Fig.4.30 Structure of Temporary data register 1

Temporary data register 2



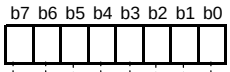
Temporary data register 2 (TD2)

[address 002Eh]

b	Functions	After reset	RW
0	DB_0 data storage	0	RW
1	DB_1 data storage	0	RW
2	DB_2 data storage	0	RW
3	DB_3 data storage	0	RW
4	DB_4 data storage	0	RW
5	DB_5 data storage	0	RW
6	DB_6 data storage	0	RW
7	DB_7 data storage	0	RW

Fig.4.31 Structure of Temporary data register 2

RRF register

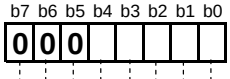


[address 002Fh]

b	Functions	After reset	RW
0	DB_0 data storage	0	RW
1	DB_1 data storage	0	RW
2	DB_2 data storage	0	RW
3	DB_3 data storage	0	RW
4	DB_4 data storage	0	RW
5	DB_5 data storage	0	RW
6	DB_6 data storage	0	RW
7	DB_7 data storage	0	RW

Fig.4.32 Structure of RRF register

Peripheral function expansion register



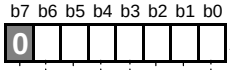
[address 0030h]

b	Name	Functions	After reset	RW
0	Transfer direction selection bit (Note 1)	0: LSB first 1: MSB first	0	RW
1	Synchronous serial I/O output pin selection bit (Note 1)	0: $P4_5/TxD$ pin 1: $P4_7/SOUT$ pin	0	RW
2	P-channel output disable selection bit (Note 2)	b3 b2 0 0 : $P4_5/TxD$ pin	0	RW
3		0 1 : Bit 4 at UART control register is invalid 1 0 : $P4_5/TxD$ pin and $P4_7/\overline{SRDY}/SOUT$ pin 1 1 : $P4_7/\overline{SRDY}/SOUT$ pin	0	RW
4	Output clock selection bit (Note 3)	0 : Internal system clock ϕ output 1 : X_{CIN} frequency signal output	0	RW
5	If writing to these bits, write “0”.		0	RW
6			0	RW
7	If writing to this bit, write “0”. Do not write "1".		0	RW

Notes: 1. These functions are valid only when serial I/O mode selection bit (bit 6 at serial I/O control register (address 001Ah)) is set to "1" (when clock synchronous serial I/O is selected).
2. Set $P4_5/TxD$, $P4_7/\overline{SRDY}/SOUT$ P-channel output disable bit (bit 4 at UART control register (address 001Bh)) to "1" after selecting the pin to disable P-channel output in these bits.
3. Set f output control bit (bit 0 at f output control register (address 002Ah)) and bit 1 at port P4 direction register to "1" in order to output X_{CIN} frequency signal.

Fig.4.33 Structure of Peripheral function expansion register

AD control register



b	Name	Functions	After reset	RW
0	Analog input pin selection bits	b2 b1 b0 0 0 0 : P6$_0$/AN$_0$ 0 0 1 : P6$_1$/AN$_1$ 0 1 0 : P6$_2$/AN$_2$ 0 1 1 : P6$_3$/AN$_3$ 1 0 0 : P6$_4$/AN$_4$ 1 0 1 : P6$_5$/AN$_5$ 1 1 0 : P6$_6$/AN$_6$ 1 1 1 : P6$_7$/AN$_7$	0	RW
1			0	RW
2			0	RW
3	AD conversion completion bit	0 : Conversion in progress 1 : Conversion completed	1	RW (Note)
4	V_{REF} input switch bit	0 : ON during conversion 1 : Always ON	0	RW
5	AD external trigger valid bit	0 : A/D external trigger invalid 1 : A/D external trigger valid	0	RW
6	Interrupt source selection bit	0 : Interrupt request at A/D conversion completed 1 : Interrupt request at ADT input falling	0	RW
7	The value is “0” at reading. If writing to this bit, write “0”.		0	RO

Note: This bit can be set to “0” but not to “1” by program.

Fig.4.34 Structure of AD control register

AD conversion high-order register

b7 b6 b5 b4 b3 b2 b1 b0

AD conversion high-order register (ADH)

[address 0035h]

b	Name	Functions	After reset	RW
0	A/D conversion results can be read. Write “00h” to these bits at writing.	In 10-bit A/D mode: b7 b6 b5 b4 b3 b2 b1 b0 = b9 b8 b7 b6 b5 b4 b3 b2 In 8-bit A/D mode: b7 b6 b5 b4 b3 b2 b1 b0 = b7 b6 b5 b4 b3 b2 b1 b0	Undefined	RO
1			Undefined	RO
2			Undefined	RO
3			Undefined	RO
4			Undefined	RO
5			Undefined	RO
6			Undefined	RO
7			Undefined	RO

Note: Do not read this register during A/D conversion.

Fig.4.35 Structure of AD conversion high-order register

AD conversion low-order register

b7 b6 b5 b4 b3 b2 b1 b0 (0 0 0)

AD conversion low-order register (ADL)

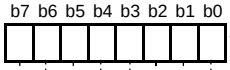
[address 0036h]

b	Name	Functions	After reset	RW
0	Conversion mode selection bit	0 : 8-bit A/D mode 1 : 10-bit A/D mode	0	RW
1	AD conversion speed selection bit	b1 b0 0 0 : f(XIN)/2 (Note 1) 0 0 : f(XIN) (Note 1) 1 0 : On-chip oscillator (Note 2) 1 1 : Do not select.	0	RW
2			0	RW
3	The values are “0” at reading. If writing to these bits, write “0”.		0	RO
4			0	RO
5			0	RO
6	• A/D conversion results in 10-bit A/D mode can be read. • In 8-bit A/D mode, the values are undefined at reading. If writing to these bits, write “0”.	In 10-bit A/D mode: b7 b6 b5 b4 b3 b2 b1 b0 = b1 b0	Undefined	RO
7			Undefined	RO

Note: 1. Available only when internal system clock selection bit (bit 7 at CPU mode register (003Bh)) is set to "0". Do not select when it is set to "1".
2. Available only when both internal system clock selection bit and on-chip oscillator control bit (bit 0 at CPU mode expansion register (002Bh)) are set to "1". Do not select when both of these bits are not set to "1".
3. Do not read this register during A/D conversion.

Fig.4.36 Structure of AD conversion low-order register

Watchdog timer control register



Watchdog timer control register (WDTCON)

[address 0037h]

b	Name	Functions	After reset	RW
0	Watchdog timer H		1	RW
1			1	RW
2			1	RW
3			1	RW
4			1	RW
5			1	RW
6	STP instruction function selection bit (Note 1)	0 : Enter stop mode by STP instruction execution 1 : Internal reset occurs by STP instruction execution.	0	RW
7	Watchdog timer count source selection bit (Note 1)	0 : f(XIN)/1024 (f(SUB)/1024 at low-speed mode) 1 : f(XIN)/4 (f(SUB)/4 at low-speed mode)	0	RW

Notes: 1. This bit can be written only once after reset is released.
After being written once, this bit is locked and can not be rewritten.
2. Watchdog timer becomes "FFh" by writing to this register.

Fig.4.37 Structure of Watchdog timer control register

Segment output enable register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 | | | | | | |

Segment output enable register (SEG)

[address 0038h]

b	Name	Functions	After reset	RW
0	Segment output enable bit 0	0 : Input port $P3_4$ to $P3_7$ 1 : Segment output SEG_{12} to SEG_{15}	0	RW
1	Segment output enable bit 1	0 : I/O port $P0_0$, $P0_1$ 1 : Segment output SEG_{16}, SEG_{17}	0	RW
2	Segment output enable bit 2	0 : Input port $P0_2$ to $P0_7$ 1 : Segment output SEG_{18} to SEG_{23}	0	RW
3	Segment output enable bit 3	0 : I/O port $P1_0$, $P1_1$ 1 : Segment output SEG_{24}, SEG_{25}	0	RW
4	Segment output enable bit 4	0 : I/W port $P1_2$ 1 : Segment output SEG_{26}	0	RW
5	Segment output enable bit 5	0 : I/O port $P1_3$ to $P1_7$ 1 : Segment output SEG_{27} to SEG_{31}	0	RW
6	The value is "0" at reading. If writing to this bit, write "0".		0	RO
7	If writing to this bit, write "0". Do not write "1".		0	RW

Fig.4.38 Structure of Segment output enable register

LCD mode register

b7 b6 b5 b4 b3 b2 b1 b0

| | | | 0 | | | | |

LCD mode register (LM)

[address 0039h]

b	Name	Functions	After reset	RW
0	Duty ratio selection bits	b1 bo 0 0 : Do not select. 0 1 : 2 (Use COM_0, COM_1) 1 0 : 3 (Use COM_0 to COM_2) 1 1 : 4 (Use COM_0 to COM_3)	0	RW
1			0	RW
2	Bias control bit	0 : 1/3 bias 1 : 1/2 bias	0	RW
3	LCD enable bit	0 : LCD OFF 1 : LCD ON	0	RW
4	If writing to this bit, write "0". Do not write "1".		0	RW
5	LCD circuit divider division ratio selection bits	b6 b5 0 0 : Clock input 0 1 : 2 division of clock input 1 0 : 4 division of clock input 1 1 : 8 division of clock input	0	RW
6			0	RW
7	LCDCK count source selection bit (Note 1) (Note 2)	0 : f(SUB)/32 1 : $f(X_{IN})$/8192 (in frequency/2, 4 or 8 mode) f(SUB)/8192 (in low-speed mode)	0	RW

Notes: 1. LCDCK is a clock for LCD timing controller.
2. f(SUB) is source oscillation frequency in low-speed mode and shows oscillation frequency of X_{CIN} or on-chip oscillator.

Fig.4.39 Structure of LCD mode register

Interrupt edge selection register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

Interrupt edge selection register (INTEDGE)

[address 003Ah]

b	Name	Functions	After reset	RW
0	INT_0 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
1	INT_1 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
2	INT_2 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
3	INT_3 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
4	The values are "0" at reading. If writing to these bits, write "0".		0	RO
5			0	RO
6			0	RO
7			0	RO

Fig.4.40 Structure of Interrupt edge selection register

CPU mode register

b7	b6	b5	b4	b3	b2	b1	b0
				1			

CPU mode register (CPUM)

[address 003Bh]

b	Name	Functions	After reset	RW
0	Processor mode selection bits	b1 b0 0 0 : Single-chip mode 0 1 : Do not select. 1 0 : Do not select. 1 1 : Do not select.	0	RW
1			0	RW
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	RW
3	If writing to this bit, write "1". Do not write "0".		1	RW
4	Port X_C switch bit (Note 3)	0 : I/O port function (Stop oscillation) 1 : X_{CIN}-X_{COUT} oscillation function	0	RW
5	Main clock (X_{IN}-X_{OUT}) stop bit (Note 4)	0 : Oscillating 1 : Stop oscillating	0	RW
6	Main clock division ratio selection bit	0 : f(X_{IN})/2 (frequency/2 mode) or f(X_{IN})/4 (frequency/4 mode) (Note 1) 1 : f(X_{IN})/8 (frequency/8 mode)	1	RW
7	Internal system clock selection bit	0 : X_{IN}-X_{OUT} selected (frequency/2, 4, or 8 mode) 1 : X_{IN}-X_{OUT} or on-chip oscillator selected (low-speed mode) (Note 2)	0	RW

Notes:
1. When the system clock ϕ is divided by 4 of f(X_{IN}), set this bit to "0" after setting frequency/4 mode control bit (bit 1 at CPU mode expansion register (address 002Bh)) to "1".
2. When using on-chip oscillator in low-speed mode, set this bit to "1" after setting on-chip oscillator control bit (bit 0 at CPU mode expansion register) to "1".
3. In low-speed mode (X_{CIN} is selected as the system clock ϕ), the X_{CIN} - X_{COUT} oscillation stops if the port X_C switch bit is set to "0".
4. In frequency/2/4/8 mode, the X_{IN} - X_{OUT} oscillation does not stop even if the main clock (X_{IN} - X_{OUT}) stop bit is set to "1".

Fig.4.41 Structure of CPU mode register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1)

[address 003Ch]

b	Name	Functions	After reset	RW
0	INT_0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
1	INT_1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
2	Serial I/O receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
3	Serial I/O transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
4	Timer X interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
5	Timer Y interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
6	Timer 2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
7	Timer 3 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)

Note: Each bit can be set to "0" but not to "1" by program.

Fig.4.42 Structure of Interrupt request register 1

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2 (IREQ2)

[address 003Dh]

b	Name	Functions	After reset	RW
0	$CNTR_0$ interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
1	$CNTR_1$ interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
2	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
3	INT_2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
4	INT_3 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
5	Key input interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
6	ADT/AD conversion interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
7	The value is "0" at reading. If writing to this bit, write "0".		0	RO

Note: Each bit can be set to "0" but not to "1" by program.

Fig.4.43 Structure of Interrupt request register 2

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1)

[address 003Eh]

b	Name	Functions	After reset	RW
0	INT_0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
1	INT_1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
2	Serial I/O receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
3	Serial I/O transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
4	Timer X interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
5	Timer Y interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
6	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
7	Timer 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW

Fig.4.44 Structure of Interrupt control register 1

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

Interrupt control register 2 (ICON2)

[address 003Fh]

b	Name	Functions	After reset	RW
0	$CNTR_0$ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
1	$CNTR_1$ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
2	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
3	INT_2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
4	INT_3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
5	Key input interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
6	ADT/AD conversion interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
7	If writing to this bit, write “0”. Do not write "1".		0	RW

Fig.4.45 Structure of Interrupt request register 2

LCD display RAM

address		bit 7 COM3	6 COM2	5 COM1	4 COM0	3 COM3	2 COM2	1 COM1	0 COM0	After reset	RW
0040h	LRAM0	SEG_1				SEG_0				Undefined	RW
0041h	LRAM1	SEG_3				SEG_2				Undefined	RW
0042h	LRAM2	SEG_5				SEG_4				Undefined	RW
0043h	LRAM3	SEG_7				SEG_6				Undefined	RW
0044h	LRAM4	SEG_9				SEG_8				Undefined	RW
0045h	LRAM5	SEG_{11}				SEG_{10}				Undefined	RW
0046h	LRAM6	SEG_{13}				SEG_{12}				Undefined	RW
0047h	LRAM7	SEG_{15}				SEG_{14}				Undefined	RW
0048h	LRAM8	SEG_{17}				SEG_{16}				Undefined	RW
0049h	LRAM9	SEG_{19}				SEG_{18}				Undefined	RW
004Ah	LRAM10	SEG_{21}				SEG_{20}				Undefined	RW
004Bh	LRAM11	SEG_{23}				SEG_{22}				Undefined	RW
004Ch	LRAM12	SEG_{25}				SEG_{24}				Undefined	RW
004Dh	LRAM13	SEG_{27}				SEG_{26}				Undefined	RW
004Eh	LRAM14	SEG_{29}				SEG_{28}				Undefined	RW
004Fh	LRAM15	SEG_{31}				SEG_{30}				Undefined	RW

Fig. 4.46 LCD display RAM

5. Reference

Data Sheet
3823 Group Data sheet
(Use the most recent version of the document on the Renesas Technology Website.)

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Website and Support

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REVISION HISTORY	3823 Group List of Registers

Rev.	Date	Description	
		Page	Summary
1.00	Jan 10, 2007	—	First edition issued
2.00	Aug 08, 2007	17	Figure 4.28 CPU mode expansion register: Note2 revised
		22	Figure 4.37 Watchdog timer control register: Bit 7 revised
		24	Figure 4.41 CPU mode register: Notes 3 and 4 added

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