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April 1st, 2010
Renesas Electronics Corporation

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3823 Group

Clock Generating Circuit (Processing During a Power Failure)

1. Abstract

The following article introduces and shows an example of how to use the Clock Generating Circuit (Processing During a Power Failure) on the 3823 group device.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: 3823 Group

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

3. Contents

3.1 Clock Generating Circuit (Processing During a Power Failure)

Outline: During a power failure, the backup power supply enables the clock count in low-speed and wait modes and allows low power consumption operation.

Specifications:

- High-speed mode operation is selected under normal conditions.
- When a power failure is detected, operation is switched to low-speed mode and the main clock oscillation stops.
- Using wait mode, the timer interrupt routine that occurs every second confirms the recovery condition.
- When recovery from power failure is detected, the main clock oscillation starts. Once oscillation is stabilized, the system clock is switched to high-speed mode.

Figure 3.1 shows a Mode Transition Example of System Clock ϕ During Power Failure, Figure 3.2 shows the Relevant Register Settings, and Figure 3.3 shows the Control Procedure.

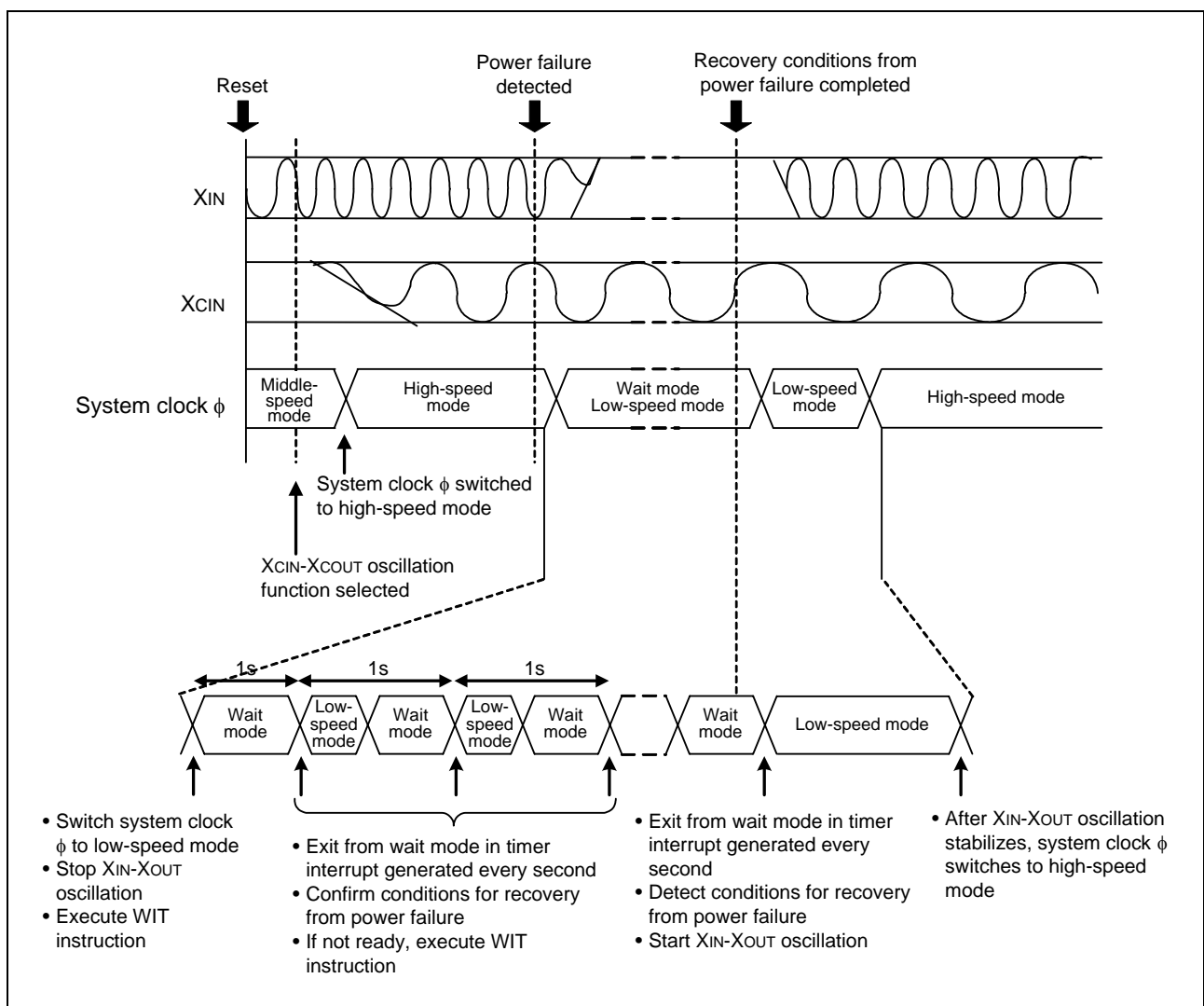


Figure 3.1 Mode Transition Example of System Clock ϕ During a Power Failure

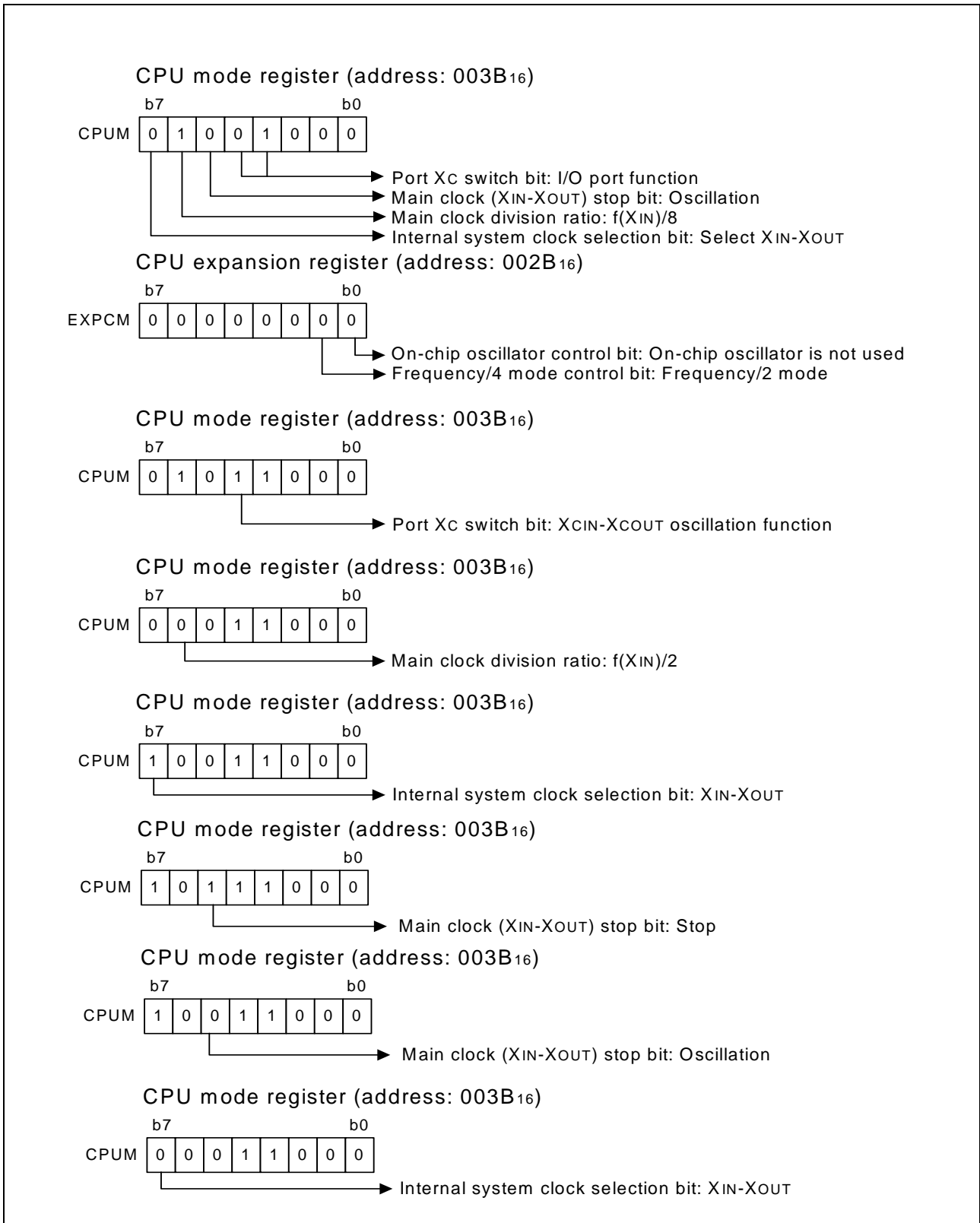


Figure 3.2 Relevant Register Settings

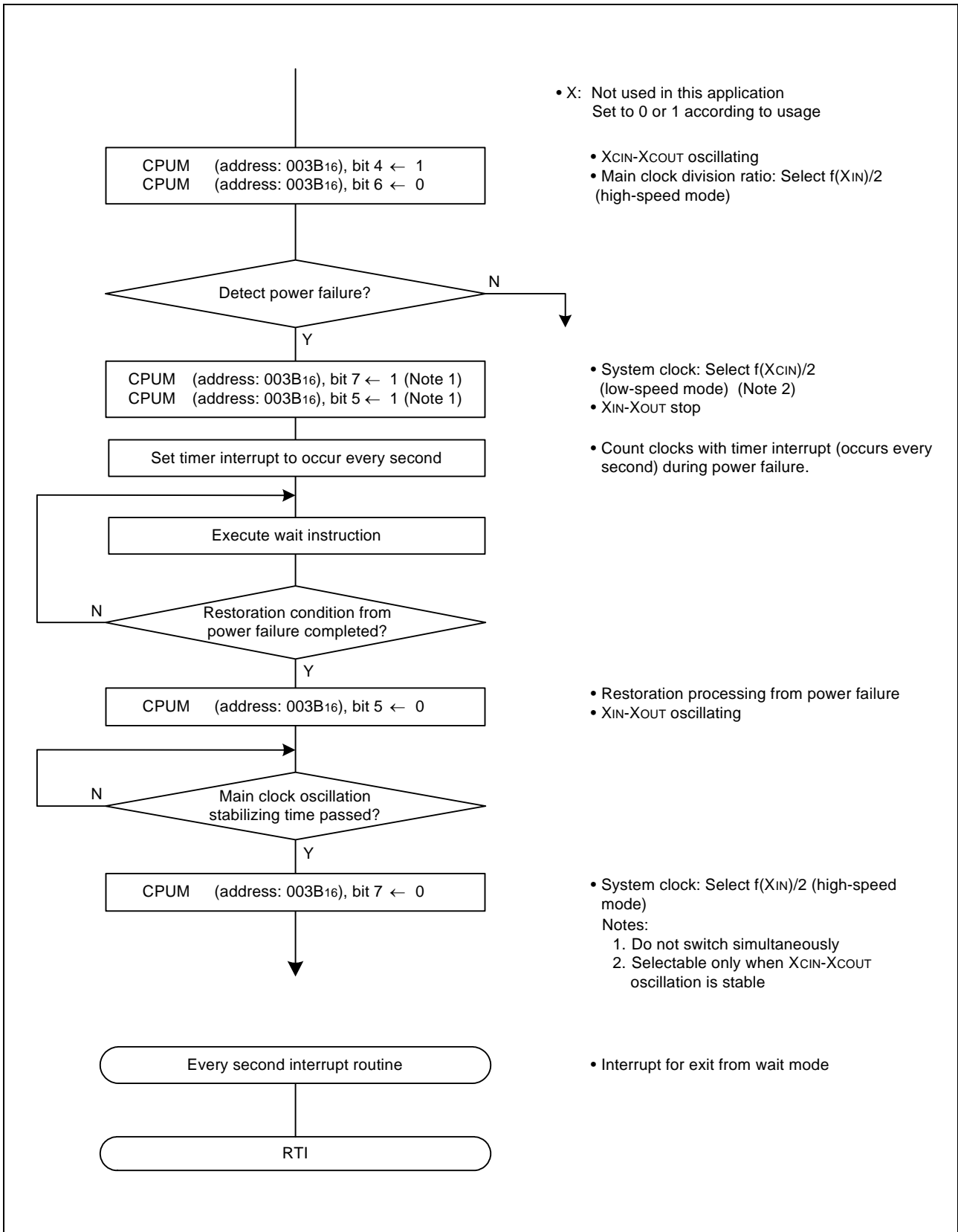


Figure 3.3 Control Procedure

4. Sample Programming Code

Download a sample program from the Renesas Technology website.
To download, click “Application Notes” in the left side menu on the page of the 3823 Group.

5. Reference Document

Datasheet
3823 Group Data sheet
Download the latest version from the Renesas Technology website.

Technical News/Technical Update
Download the latest information from the Renesas Technology website.

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REVISION HISTORY	3823 Group Clock Generating Circuit (Processing During a Power Failure)
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Rev.	Date	Description	
		Page	Summary
1.00	Aug 10, 2006	-	First Edition issued

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