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## 3803H/3803L Group

### Flash Memory Version CPU Rewrite Mode (EW0 Mode)

#### 1. Abstract

This document describes an application example for the flash memory version CPU rewrite mode (EW0 mode) in the 3803H/3803L Group.

#### 2. Introduction

The application example described in this document is applied to the following MCU and parameter(s):

- MCU : 3803H Group, 3803L Group
- Oscillation frequency : 16 MHz

Reference data:

Reference values for erase and program time are shown below.

Block erase:	Block 0, 1 (8 Kbytes)	Typ = 0.5 s, Max = 9 s
	Block 2 (16 Kbytes)	Typ = 0.9 s, Max = 9 s
	Block 3 (24 Kbytes)	Typ = 1.3 s, Max = 9 s
	Block A, B (2 Kbytes)	Typ = 0.3 s, Max = 9 s
Program:	Per byte	Typ = 60 $\mu$ s, Max = 400 $\mu$ s

This sample program may include operations of unused bit functions for the SFR bit layout. Set these values according to the operating conditions of the user system.

### 3. Application Description

#### 3.1 Flash Memory CPU Rewrite Mode

CPU rewrite mode allows the operations (read, program, erase, etc.) of the internal flash memory via the control from the central processing unit (CPU).

In CPU rewrite mode, the flash memory cannot be read/written from the CPU. The rewrite program should be executed on the RAM after being transferred to the internal RAM.

• **EW0 mode**

In EW0 mode, the CPU rewrite program is transferred to RAM, the program and erase commands are issued by the CPU rewrite program on the RAM. This allows the user ROM area and data block area to be rewritten.

Specifications:

- Set the system clock  $\phi$  to  $f(XIN)/2$  at normal operation, and  $f(XIN)/8$  at CPU rewrite mode operation.
- Execute the CPU rewrite program on the RAM after transferring to RAM.
- Erase and program data block B.

Figure 3.1 shows the Block Diagram of Internal Flash Memory (ROM 60K), Figure 3.2 shows the CPU Rewrite Program Allocation Map, Figure 3.3 shows the Relevant Register Settings, and Figure 3.4 shows the CPU Rewrite Mode (EW0 Mode) Control Flow.

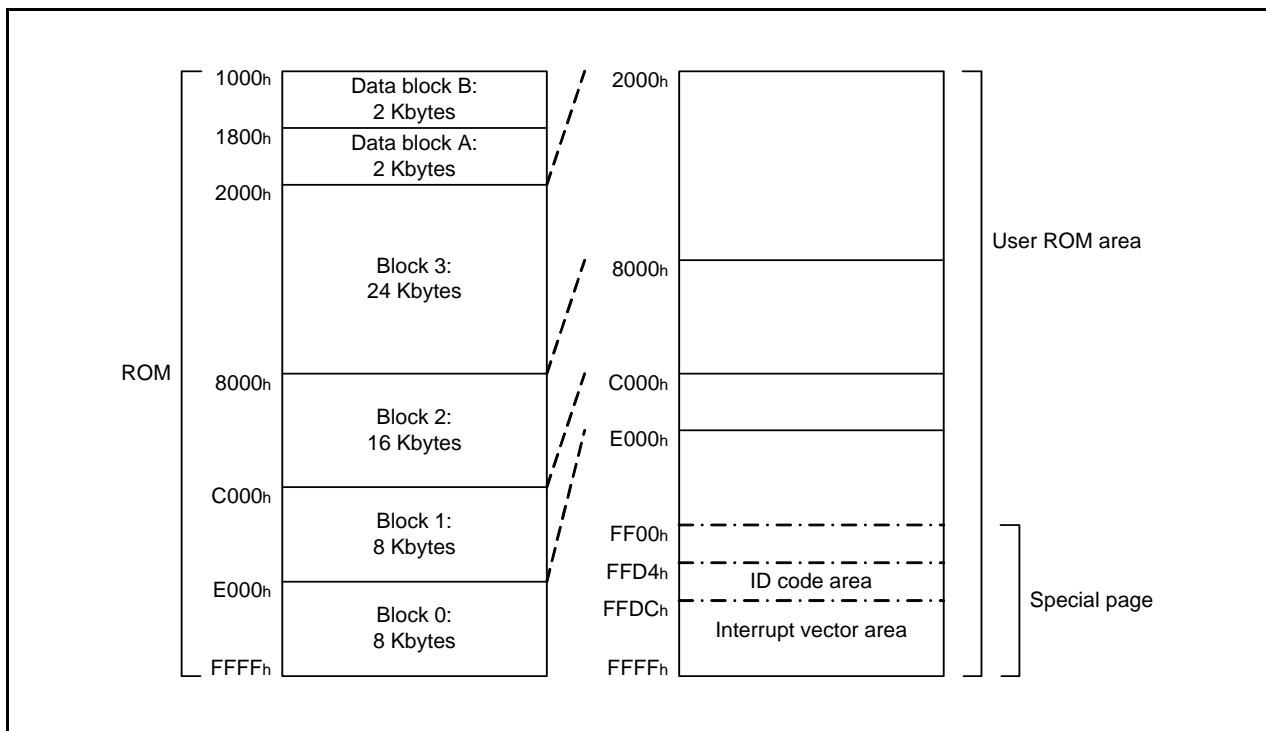


Figure 3.1 Block Diagram of Internal Flash Memory (ROM 60K)

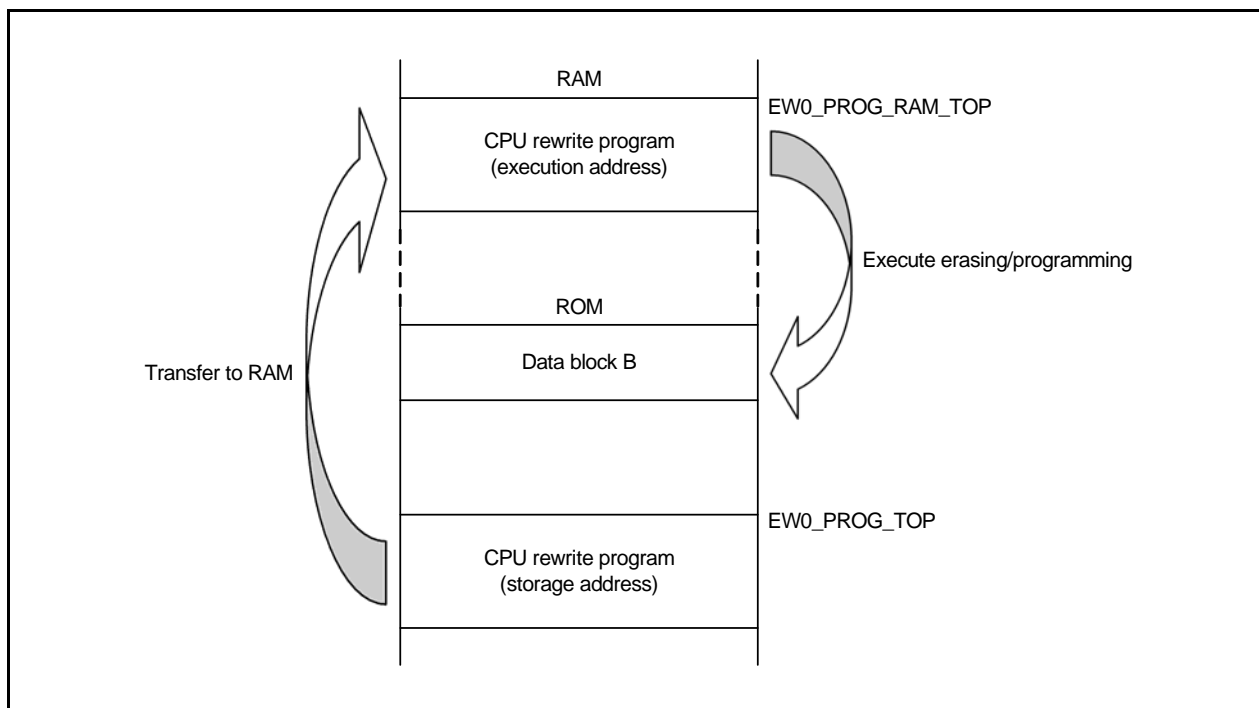


Figure 3.2 CPU Rewrite Program Allocation Map

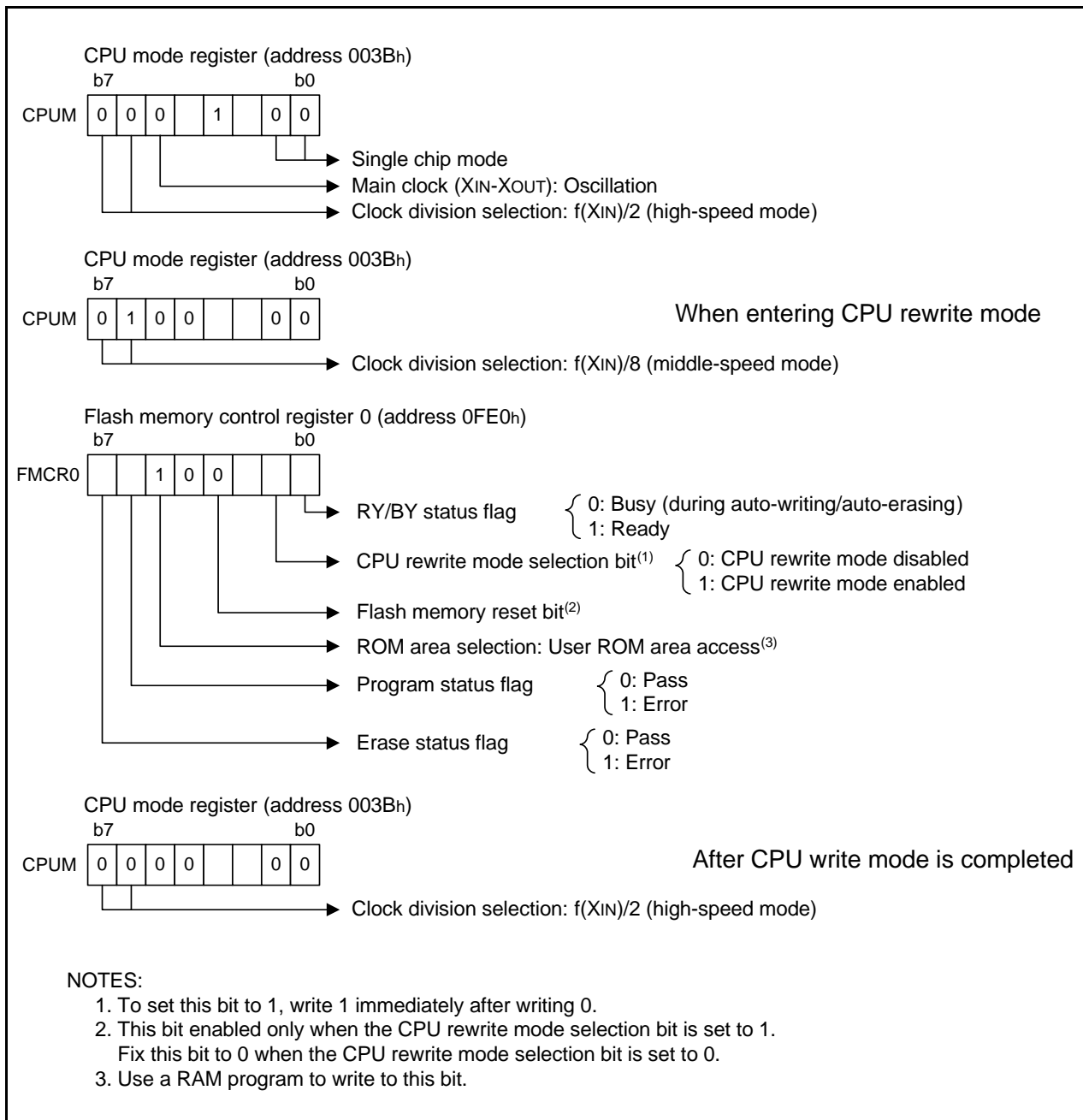


Figure 3.3 Relevant Register Settings

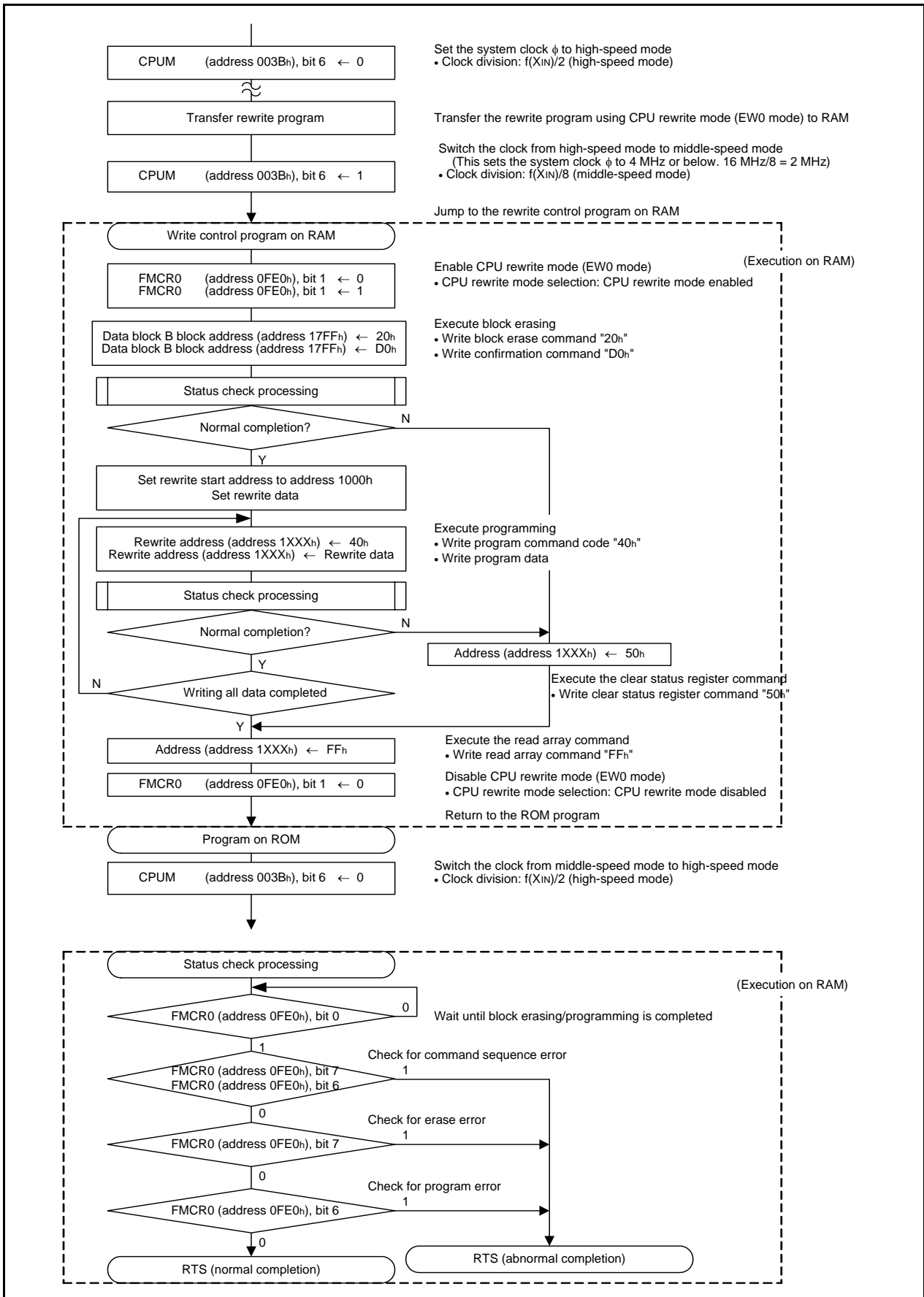


Figure 3.4 CPU Rewrite Mode (EW0 Mode) Control Flow

- **EW0 mode**

When the flash memory is written using CPU mode, the following should be noted:

(1) Operating speed

During CPU rewrite mode, set the system clock  $\phi$  to 4.0 MHz or below by the clock division selection bits (bits 6 and 7 of address 003Bh).

(2) Unavailable Instruction

During CPU rewrite mode, no instruction to refer to the data in the flash memory can be used.

(3) Interrupt

During CPU rewrite mode, no interrupt can be used as it refers to the data in the flash memory.

(4) Watchdog timer

If the watchdog timer is already activated, it is always cleared during programming or erasing so that no internal reset occurs by underflow.

(5) Reset

A reset can be accepted any time. After releasing reset, the boot mode is activated when CNVSS = H. This allows the program to start from the address stored in the addresses FFFCh, FFFDh in the boot ROM area.



#### **4. Sample Programming Code**

A sample program can be downloaded from the Renesas Technology website.  
For download, click “Application Notes” in the left-hand side menu of the 3803H Group, 3803L Group page.

#### **5. Reference Documents**

Datasheets

3803 Group (Sepc. H) Datasheet

3803 Group (Sepc. L) Datasheet

The latest versions can be downloaded from the Renesas Technology website.

Technical Update/Technical News

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REVISION HISTORY	3803H/3803L Group Flash Memory Version CPU Rewrite Mode (EW0 Mode)
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 13, 2007	–	First Edition issued

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