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3803 Group (Spec.H)

Peripheral Function Application

1. Introduction

The following article introduces and shows an application example of peripheral function.

The explanation of this issue is applied to the following condition:
Applicable MCU: 3803 Group (Spec.H)

2. Application

2.1 I/O port

This paragraph describes the setting method of I/O port relevant registers, notes etc.

2.1.1 Memory map

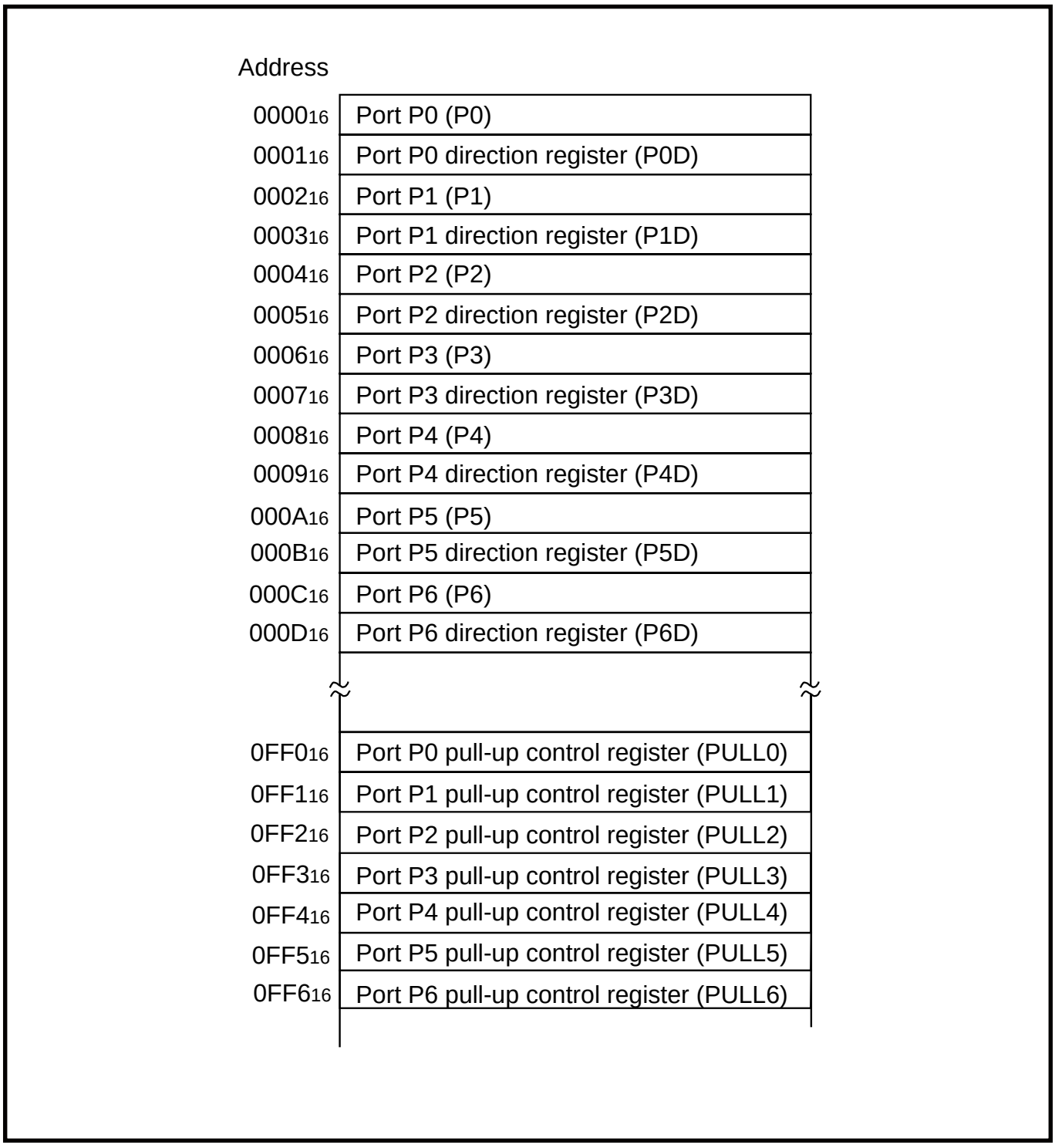


Fig. 2.1.1 Memory map of I/O port relevant registers

2.1.2 Relevant registers

Port Pi

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi (i = 0, 1, 2, 3, 4, 5, 6)
(Pi: addresses 0000_{16}, 0002_{16}, 0004_{16}, 0006_{16}, 0008_{16}, $000A_{16}$, $000C_{16}$)

b	Name	Functions	At reset	R	W
0	Port P_{i0}	●In output mode Write •••••••• Port latch Read •••••••• Port latch ●In input mode Write •••••••• Port latch Read •••••••• Value of pin	0	○	○
1	Port P_{i1}		0	○	○
2	Port P_{i2}		0	○	○
3	Port P_{i3}		0	○	○
4	Port P_{i4}		0	○	○
5	Port P_{i5}		0	○	○
6	Port P_{i6}		0	○	○
7	Port P_{i7}		0	○	○

Fig. 2.1.2 Structure of Port Pi (i = 0 to 6)

Port Pi direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (i = 0, 1, 2, 3, 4, 5, 6)
(PiD: addresses 0001_{16}, 0003_{16}, 0005_{16}, 0007_{16}, 0009_{16}, $000B_{16}$, $000D_{16}$)

b	Name	Functions	At reset	R	W
0	Port Pi direction register	0 : Port P_{i0} input mode 1 : Port P_{i0} output mode	0	×	○
1		0 : Port P_{i1} input mode 1 : Port P_{i1} output mode	0	×	○
2		0 : Port P_{i2} input mode 1 : Port P_{i2} output mode	0	×	○
3		0 : Port P_{i3} input mode 1 : Port P_{i3} output mode	0	×	○
4		0 : Port P_{i4} input mode 1 : Port P_{i4} output mode	0	×	○
5		0 : Port P_{i5} input mode 1 : Port P_{i5} output mode	0	×	○
6		0 : Port P_{i6} input mode 1 : Port P_{i6} output mode	0	×	○
7		0 : Port P_{i7} input mode 1 : Port P_{i7} output mode	0	×	○

Fig. 2.1.3 Structure of Port Pi direction register (i = 0 to 6)

Port Pi pull-up control register (i = 0 to 2, 4 to 6)

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi pull-up control register (i = 0 to 2, 4 to 6)
(PULLi: addresses 0FF0$_{16}$, 0FF1$_{16}$, 0FF2$_{16}$, 0FF4$_{16}$, 0FF5$_{16}$, 0FF6$_{16}$)

b	Name	Functions	At reset	R	W
0	Port Pi$_0$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
1	Port Pi$_1$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
2	Port Pi$_2$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
3	Port Pi$_3$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
4	Port Pi$_4$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
5	Port Pi$_5$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
6	Port Pi$_6$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
7	Port Pi$_7$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○

Fig. 2.1.4 Structure of Port Pi pull-up control register (i = 0, 1, 2, 4, 5, 6)

Port P3 pull-up control register

b7 b6 b5 b4 b3 b2 b1 b0

Port P3 pull-up control register
(PULL3: address 0FF3$_{16}$)

b	Name	Functions	At reset	R	W
0	Port P3$_0$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
1	Port P3$_1$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
2	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “0”.		0	○	×
3			0	○	×
4	Port P3$_4$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
5	Port P3$_5$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
6	Port P3$_6$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
7	Port P3$_7$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○

Fig. 2.1.5 Structure of Port P3 pull-up control register

2.1.3 Port Pi pull-up control register

Valid/Invalid of pull-up resistor can be set by the pull-up control register by a bit unit. Pull-up control is valid only when each direction register is set to the input mode.

Note: Ports $P3_2$ and $P3_3$ do not have pull-up control bit because they are N-channel open-drain output.

2.1.4 Terminate unused pins

Table 2.1.1 Termination of unused pins (in single-chip mode)

Pins	Termination
P0, P1, P2, P3, P4, P5, P6	• Set to the input mode and connect each to V_{CC} or V_{SS} through a resistor of 1 kΩ to 10 kΩ. • Set to the output mode and open at “L” or “H” output state.
V_{REF}	Connect to Vss (GND).
AV_{SS}	Connect to Vss (GND).
X_{OUT}	Open (only when using external clock)

2.1.5 Notes on I/O port

(1) Notes in standby state

In standby state*1 for low-power dissipation, do not make input levels of an I/O port “undefined”, especially for I/O ports of the N-channel open-drain.
Pull-up (connect the port to VCC) or pull-down (connect the port to VSS) these ports through a resistor.
When determining a resistance value, note the following points:
• External circuit
• Variation of output levels during the ordinary operation

When using built-in pull-up resistor, note on varied current values:
• When setting as an input port : Fix its input level
• When setting as an output port : Prevent current from flowing out to external

● **Reason**

Even when setting as an output port with its direction register, when the content of the port latch is “1”, the transistor becomes the OFF state, which causes the ports to be the high-impedance state. Note that the level becomes “undefined” depending on external circuits.
Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of an I/O port are “undefined”. This may cause power source current.

✻1 standby state: stop mode by executing **STP** instruction
wait mode by executing **WIT** instruction

(2) Modifying output data with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction*2, the value of the unspecified bit may be changed.

● **Reason**

The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit. Accordingly, when these instructions are executed on a bit of the port latch of an I/O port, the following is executed to all bits of the port latch.
•As for bit which is set for input port:
The pin state is read in the CPU, and is written to this bit after bit managing.
•As for bit which is set for output port:
The bit value is read in the CPU, and is written to this bit after bit managing.

Note the following:
•Even when a port which is set as an output port is changed for an input port, its port latch holds the output data.
•As for a bit of which is set for an input port, its value may be changed even when not specified with a bit managing instruction in case where the pin state differs from its port latch contents.

✻2 Bit managing instructions: **SEB** and **CLB** instructions

2.1.6 Termination of unused pins

(1) Terminate unused pins

① I/O ports :

- Set the I/O ports for the input mode and connect them to V_{CC} or V_{SS} through each resistor of 1 kΩ to 10 kΩ.
  Ports that permit the selecting of a built-in pull-up resistor can also use this resistor. Set the I/O ports for the output mode and open them at “L” or “H”.
- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

② The AVss pin when not using the A-D converter :

- When not using the A-D converter, handle a power source pin for the A-D converter, AVss pin as follows:
  AVss: Connect to the Vss pin.

(2) Termination remarks

① I/O ports :
Do not open in the input mode.

● **Reason**

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination ② and shown on the above.

② I/O ports :
When setting for the input mode, do not connect to V_{CC} or V_{SS} directly.

● **Reason**

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between a port and V_{CC} (or V_{SS}).

③ I/O ports :
When setting for the input mode, do not connect multiple ports in a lump to V_{CC} or V_{SS} through a resistor.

● **Reason**

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

- At the termination of unused pins, perform wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

2.2 Interrupt

This paragraph explains the registers setting method and the notes relevant to the interrupt.

2.2.1 Memory map

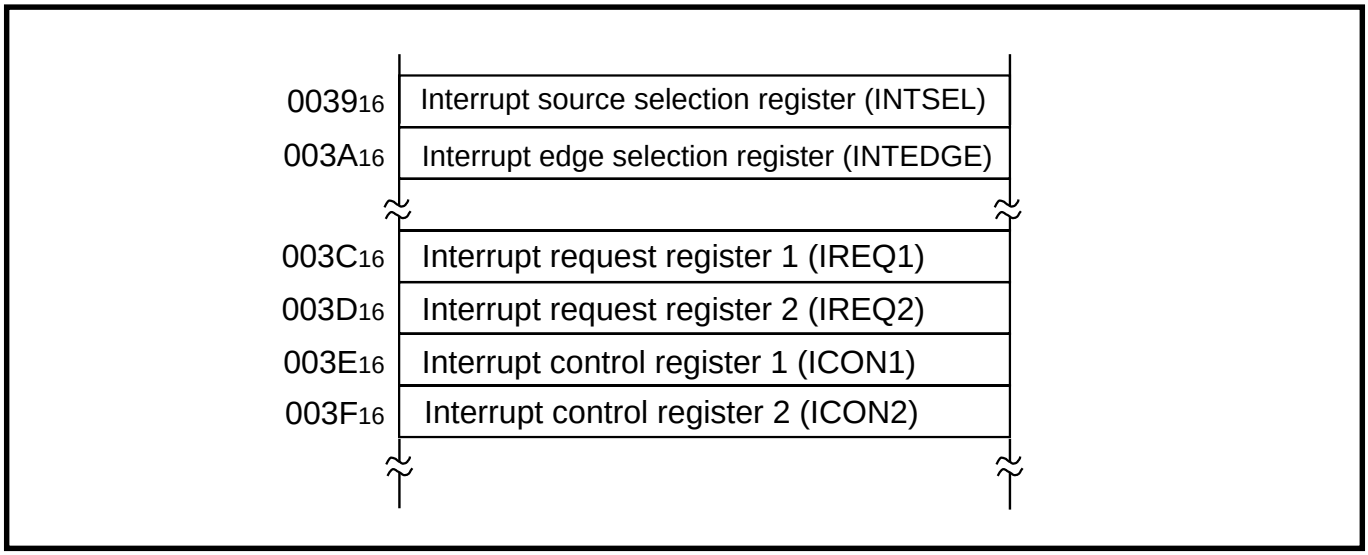
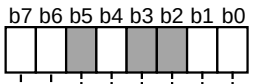


Fig. 2.2.1 Memory map of registers relevant to interrupt

2.2.2 Relevant registers

Interrupt source selection register



Interrupt source selection register
(INTSEL: address 0039₁₆)

b	Name	Functions	At reset	R	W
0	INT₀/Timer Z interrupt source selection bit (*1)	0: INT₀ interrupt 1: Timer Z interrupt	0	○	○
1	Serial I/O2/Timer Z interrupt source selection bit (*1)	0: Serial I/O2 interrupt 1: Timer Z interrupt	0	○	○
2	Nothing is arranged for these bits. Do not write “1” to these bits. When these bits are read out, the contents are “0”.		0	○	○
3			0	○	○
4	INT₄/CNTR₂ interrupt source selection bit	0: INT₄ interrupt 1: CNTR₂ interrupt	0	○	○
5	Nothing is arranged for this bit. Do not write “1” to this bit. When this bit is read out, the contents are “0”.		0	○	○
6	CNTR₁/Serial I/O3 receive interrupt source selection bit	0: CNTR₁ interrupt 1: Serial I/O3 receive interrupt	0	○	○
7	AD converter/Serial I/O3 transmit interrupt source selection bit	0: A-D converter interrupt 1: Serial I/O3 transmit interrupt	0	○	○

*1: Do not write “1” to these bits simultaneously.

Fig. 2.2.2 Structure of Interrupt source selection register

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt edge selection register
(INTEDGE: address 003A16)

b	Name	Functions	At reset	R	W
0	INT_0 active edge selection bit	0: Falling edge active 1: Rising edge active	0	○	○
1	INT_1 active edge selection bit	0: Falling edge active 1: Rising edge active	0	○	○
2	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are “0”.		0	○	×
3	INT_2 active edge selection bit	0: Falling edge active 1: Rising edge active	0	○	○
4	INT_3 active edge selection bit	0: Falling edge active 1: Rising edge active	0	○	○
5	INT_4 active edge selection bit	0: Falling edge active 1: Rising edge active	0	○	○
6	INT_0, INT_4 interrupt switch bit	0: INT_{00}, INT_{40} interrupt 1: INT_{01}, INT_{41} interrupt	0	○	○
7	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are “0”.		0	○	×

Fig. 2.2.3 Structure of Interrupt edge selection register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

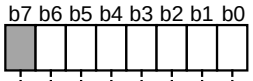
Interrupt request register 1
(IREQ1 : address 003C16)

b	Name	Functions	At reset	R	W
0	INT_0/Timer Z interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
1	INT_1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
2	Serial I/O1 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
3	Serial I/O1 transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
4	Timer X interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
5	Timer Y interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
6	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
7	Timer 2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*

*: “0” can be set by software, but “1” cannot be set.

Fig. 2.2.4 Structure of Interrupt request register 1

Interrupt request register 2



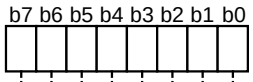
Interrupt request register 2
(IREQ2 : address 003D16)

b	Name	Functions	At reset	R	W
0	CNTR0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	CNTR1/Serial I/O3 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	Serial I/O2/Timer Z interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	INT2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	INT3 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	INT4/CNTR2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	AD converter/Serial I/O3 transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are “0”.		0	○	×

✻: “0” can be set by software, but “1” cannot be set.

Fig. 2.2.5 Structure of Interrupt request register 2

Interrupt control register 1

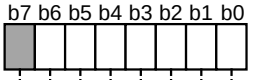


Interrupt control register 1
(ICON1 : address 003E16)

b	Name	Functions	At reset	R	W
0	INT0/Timer Z interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Serial I/O1 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Serial I/O1 transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Timer X interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Timer Y interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.2.6 Structure of Interrupt control register 1

Interrupt control register 2



Interrupt control register 2
(ICON2 : address 003F16)

b	Name	Functions	At reset	R	W
0	$CNTR_0$ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	$CNTR_1$/ Serial I/O3 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Serial I/O2/ Timer Z interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	INT_2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT_3 interrupt enable bit	0 : Interrupt disabled	0	○	○
5	INT_4/$CNTR_2$ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	AD converter/Serial I/O3 transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Nothing is arranged for this bit. Do not write “1” to this bit. When this bit is read out, the contents are “0”.		0	○	○

Fig. 2.2.7 Structure of Interrupt control register 2

2.2.3 Interrupt source

The 3803 group (Spec. H) 's interrupts are a type of vector and occur by 16 sources among 21 sources: eight external, twelve internal, and one software. These are vector interrupts with a fixed priority system. Accordingly, when two or more interrupt requests occur during the same sampling, the higher-priority interrupt is accepted first. This priority is determined by hardware, but a variety of priority processing can be performed by software, using an interrupt enable bit and an interrupt disable flag.
For interrupt sources, vector addresses and interrupt priority, refer to Tables 2.2.1.

Table 2.2.1 Interrupt sources, vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
Timer Z				At timer Z underflow	
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Serial I/O1 reception	4	$FFF7_{16}$	$FFF6_{16}$	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	$FFF5_{16}$	$FFF4_{16}$	At completion of serial I/O1 transmission shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X underflow	
Timer Y	7	$FFF1_{16}$	$FFF0_{16}$	At timer Y underflow	
Timer 1	8	$FFEF_{16}$	$FFEE_{16}$	At timer 1 underflow	STP release timer underflow
Timer 2	9	$FFED_{16}$	$FFEC_{16}$	At timer 2 underflow	
$CNTR_0$	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Serial I/O3 reception				At completion of serial I/O3 data reception	Valid when serial I/O3 is selected
Serial I/O2	12	$FFE7_{16}$	$FFE6_{16}$	At completion of serial I/O2 data transmission or reception	Valid when serial I/O2 is selected
Timer Z				At timer Z underflow	
INT_2	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
INT_3	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt (active edge selectable)
INT_4	15	$FFE1_{16}$	$FFE0_{16}$	At detection of either rising or falling edge of INT_4 input	External interrupt (active edge selectable)
$CNTR_2$				At detection of either rising or falling edge of $CNTR_2$ input	External interrupt (active edge selectable)
A-D converter	16	$FFDF_{16}$	$FFDE_{16}$	At completion of A-D conversion	
Serial I/O3 transmission				At completion of serial I/O3 transmission shift or when transmission buffer is empty	Valid when serial I/O3 is selected
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

2.2.4 Interrupt operation

When an interrupt request is accepted, the contents of the following registers just before acceptance of the interrupt requests are automatically pushed onto the stack area in the order of ①, ② and ③.

①High-order contents of program counter (PC_H)
②Low-order contents of program counter (PC_L)
③Contents of processor status register (PS)

After the contents of the above registers are pushed onto the stack area, the accepted interrupt vector address enters the program counter and consequently the interrupt processing routine is executed.
When the RTI instruction is executed at the end of the interrupt processing routine, the contents of the above registers pushed onto the stack area are restored to the respective registers in the order of ③, ② and ①; and the microcomputer resumes the processing executed just before acceptance of the interrupts.
Figure 2.2.8 shows an interrupt operation diagram.

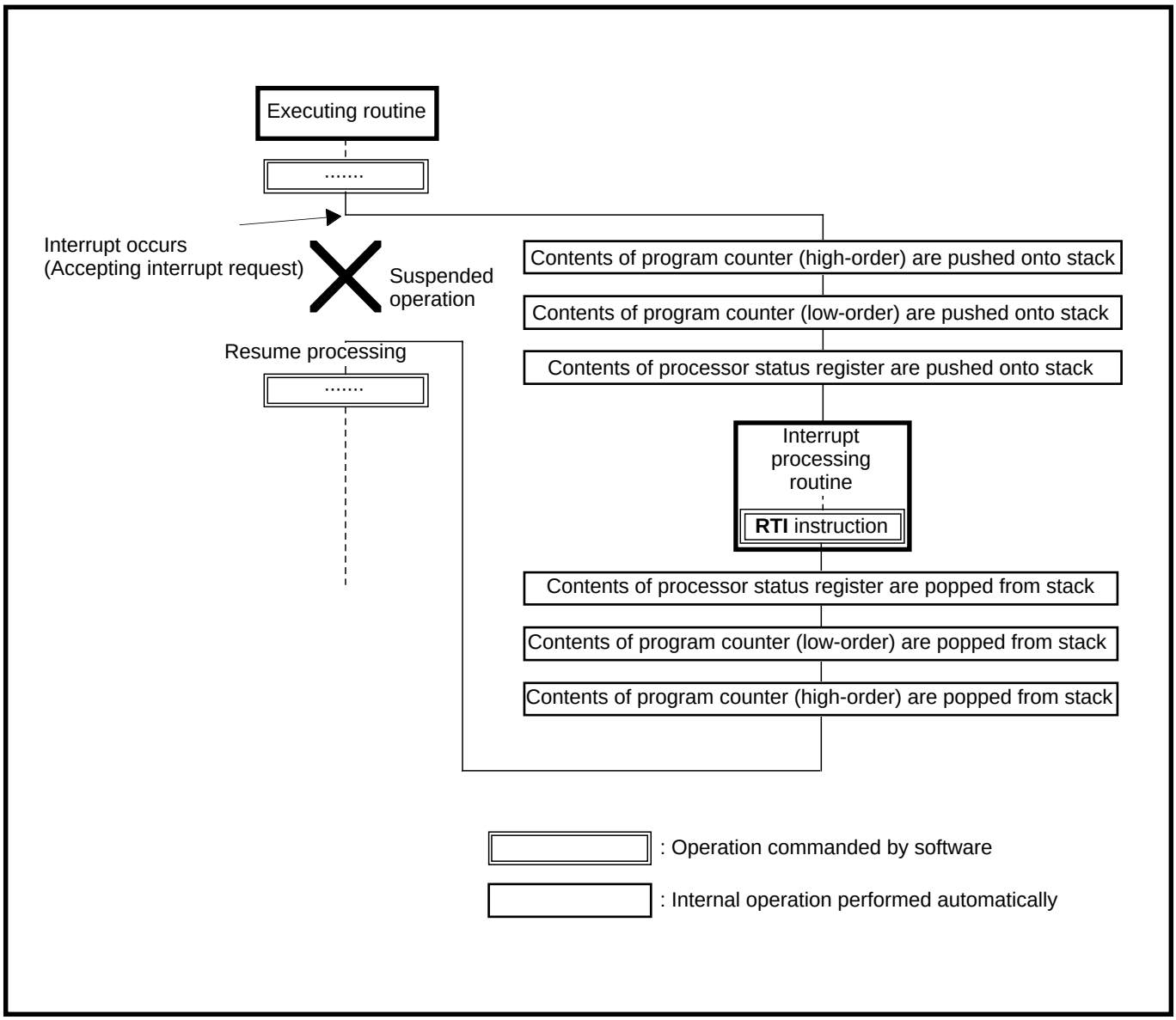


Fig. 2.2.8 Interrupt operation diagram

(1) Processing upon acceptance of interrupt request

Upon acceptance of an interrupt request, the following operations are automatically performed.

①The processing being executed is stopped.

②The contents of the program counter and the processor status register are pushed onto the stack area. Figure 2.2.9 shows the changes of the stack pointer and the program counter upon acceptance of an interrupt request.

③Concurrently with the push operation, the jump destination address (the beginning address of the interrupt processing routine) of the occurring interrupt stored in the vector address is set in the program counter, then the interrupt processing routine is executed.

④After the interrupt processing routine is started, the corresponding interrupt request bit is automatically cleared to “0”. The interrupt disable flag is set to “1” so that multiple interrupts are disabled.

Accordingly, for executing the interrupt processing routine, it is necessary to set the jump destination address in the vector area corresponding to each interrupt.

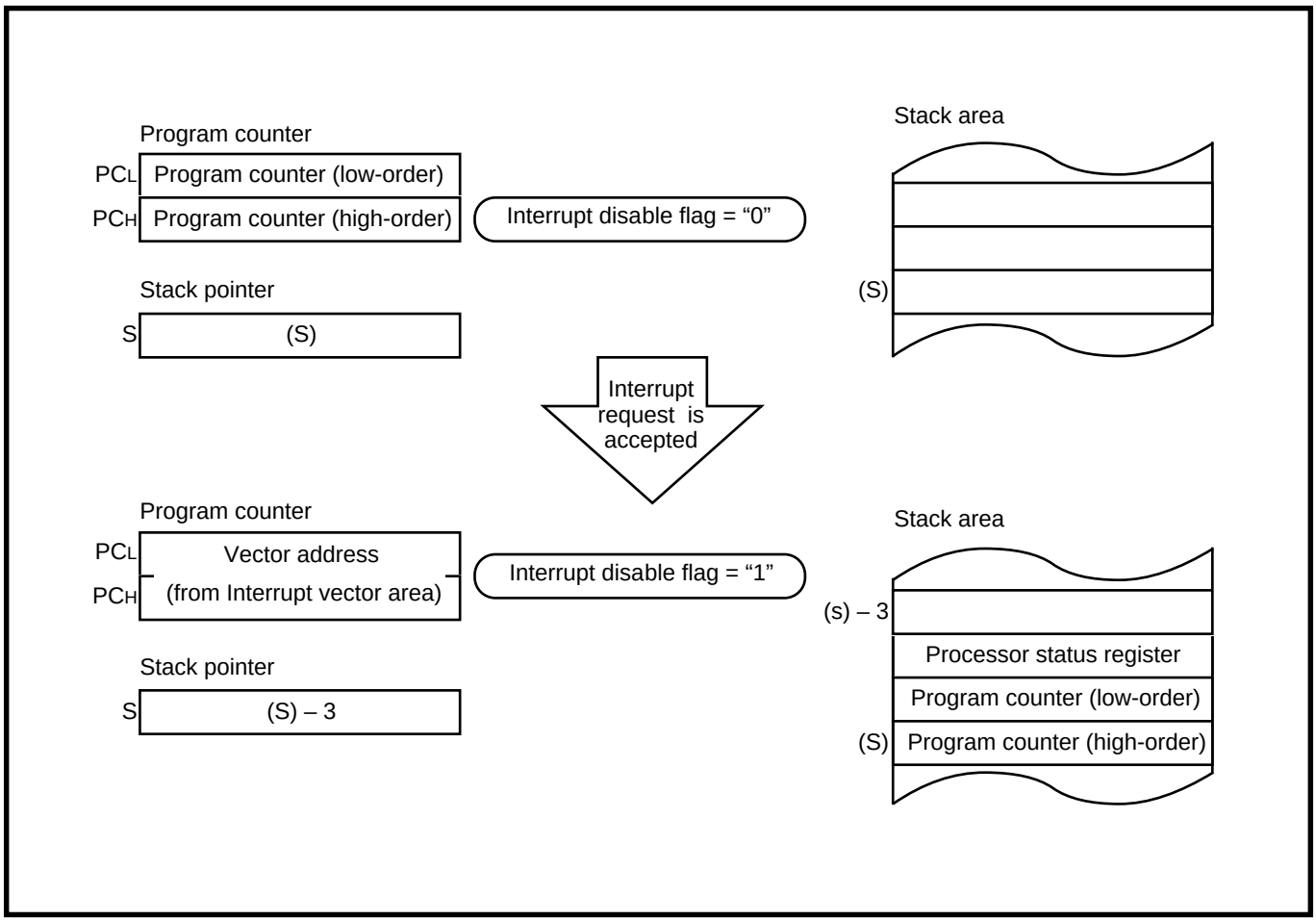


Fig. 2.2.9 Changes of stack pointer and program counter upon acceptance of interrupt request

(2) Timing after acceptance of interrupt request

The interrupt processing routine begins with the machine cycle following the completion of the instruction that is currently being executed.

Figure 2.2.10 shows the time up to execution of interrupt processing routine and Figure 2.2.11 shows the timing chart after acceptance of interrupt request.

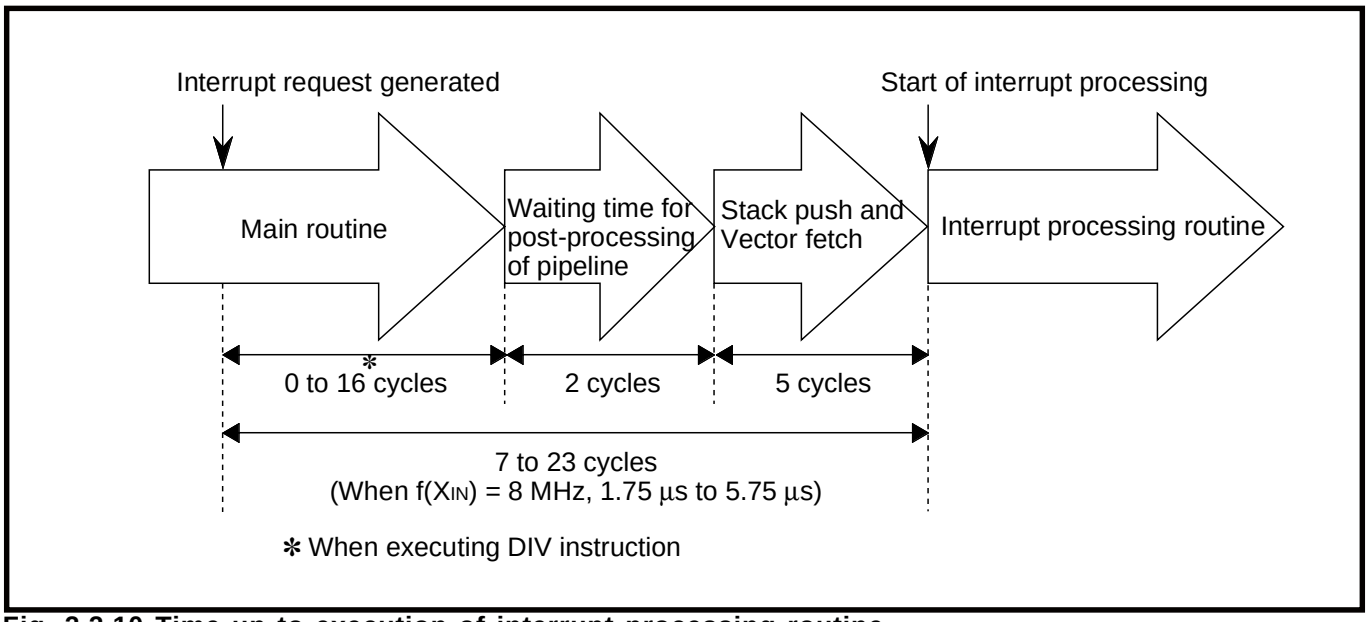


Fig. 2.2.10 Time up to execution of interrupt processing routine

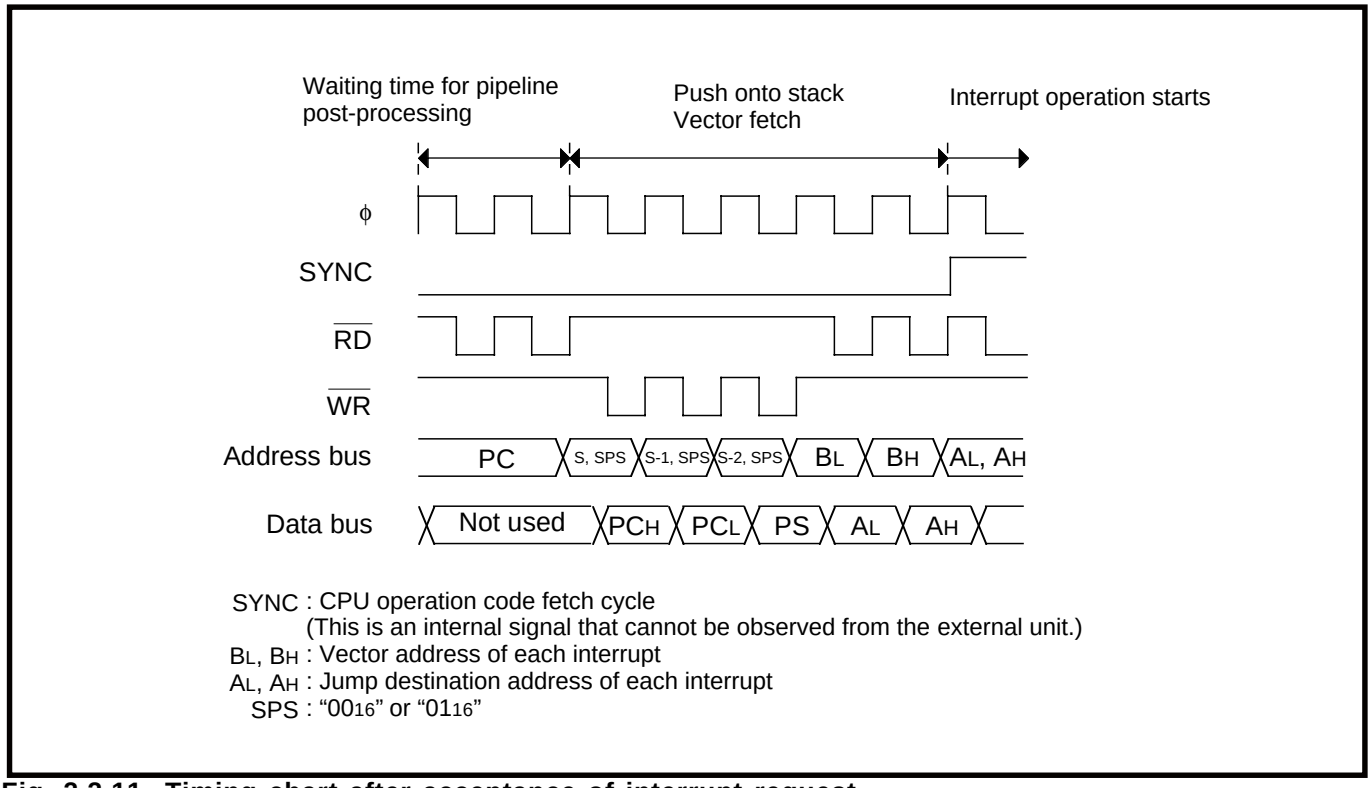


Fig. 2.2.11 Timing chart after acceptance of interrupt request

2.2.5 Interrupt control

The acceptance of all interrupts, excluding the BRK instruction interrupt, can be controlled by the interrupt request bit, interrupt enable bit, and an interrupt disable flag, as described in detail below. Figure 2.2.12 shows an interrupt control diagram.

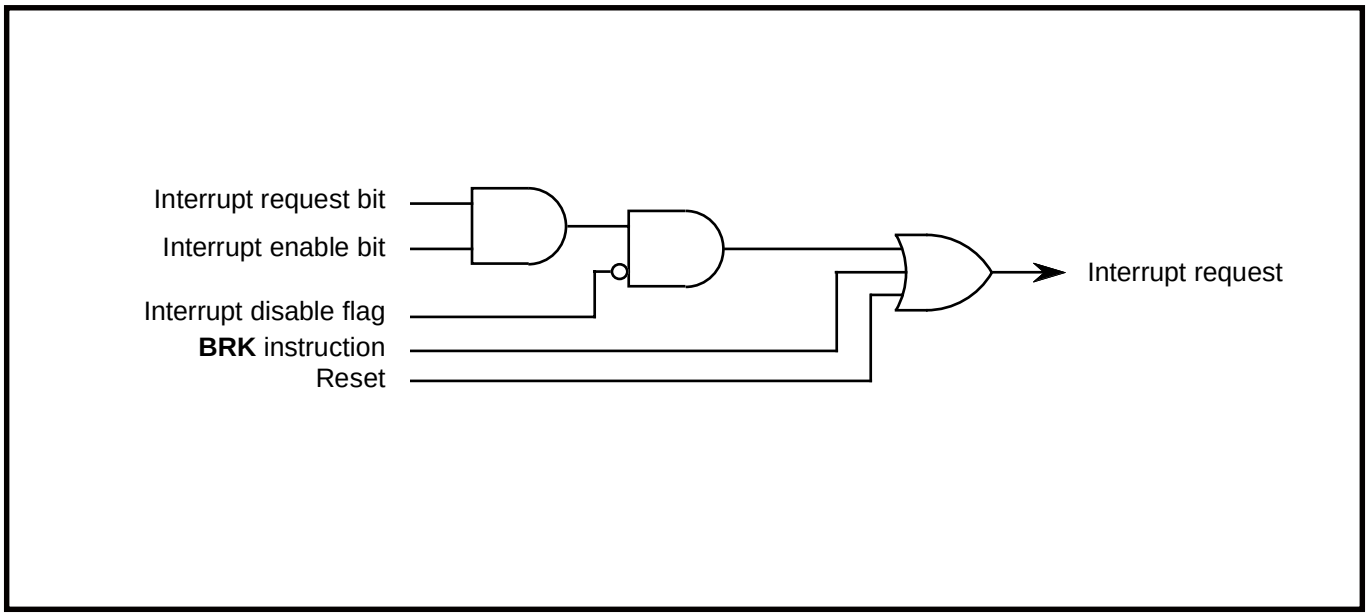


Fig. 2.2.12 Interrupt control diagram

The interrupt request bit, interrupt enable bit and interrupt disable flag function independently and do not affect each other. An interrupt is accepted when all the following conditions are satisfied.

- Interrupt request bit ..... "1"
- Interrupt enable bit ..... "1"
- Interrupt disable flag ..... "0"

Though the interrupt priority is determined by hardware, a variety of priority processing can be performed by software using the above bits and flag. Tables 2.2.2 shows list of interrupt control bits according to the interrupt source.

(1) Interrupt request bits

The interrupt request bits are allocated to the interrupt request register 1 (address $003C_{16}$) and interrupt request register 2 (address $003D_{16}$).

The occurrence of an interrupt request causes the corresponding interrupt request bit to be set to "1". The interrupt request bit is held in the "1" state until the interrupt is accepted. When the interrupt is accepted, this bit is automatically cleared to "0".

Each interrupt request bit can be set to "0", but cannot be set to "1", by software.

(2) Interrupt enable bits

The interrupt enable bits are allocated to the interrupt control register 1 (address $003E_{16}$) and the interrupt control register 2 (address $003F_{16}$).

The interrupt enable bits control the acceptance of the corresponding interrupt request.

When an interrupt enable bit is "0", the corresponding interrupt request is disabled. If an interrupt request occurs when this bit is "0", the corresponding interrupt request bit is set to "1" but the interrupt is not accepted. In this case, unless the interrupt request bit is set to "0" by software, the interrupt request bit remains in the "1" state.

When an interrupt enable bit is "1", the corresponding interrupt is enabled. If an interrupt request occurs when this bit is "1", the interrupt is accepted (when interrupt disable flag = "0").

Each interrupt enable bit can be set to "0" or "1" by software.

(3) Interrupt disable flag

The interrupt disable flag is allocated to bit 2 of the processor status register. The interrupt disable flag controls the acceptance of interrupt request except BRK instruction.

When this flag is “1”, the acceptance of interrupt requests is disabled. When the flag is “0”, the acceptance of interrupt requests is enabled. This flag is set to “1” with the SEI instruction and is set to “0” with the CLI instruction.

When a main routine branches to an interrupt processing routine, this flag is automatically set to “1”, so that multiple interrupts are disabled. To use multiple interrupts, set this flag to “0” with the CLI instruction within the interrupt processing routine. Figure 2.2.13 shows an example of multiple interrupts.

Table 2.2.2 List of interrupt bits according to interrupt source

Interrupt source	Interrupt enable bit		Interrupt request bit	
	Address	Bit	Address	Bit
INT_0/Timer Z	$003E_{16}$	b0	$003C_{16}$	b0
INT_1	$003E_{16}$	b1	$003C_{16}$	b1
Serial I/O1 reception	$003E_{16}$	b2	$003C_{16}$	b2
Serial I/O1 transmission	$003E_{16}$	b3	$003C_{16}$	b3
Timer X	$003E_{16}$	b4	$003C_{16}$	b4
Timer Y	$003E_{16}$	b5	$003C_{16}$	b5
Timer 1	$003E_{16}$	b6	$003C_{16}$	b6
Timer 2	$003E_{16}$	b7	$003C_{16}$	b7
$CNTR_0$	$003F_{16}$	b0	$003D_{16}$	b0
$CNTR_1$/Serial I/O3 reception	$003F_{16}$	b1	$003D_{16}$	b1
Serial I/O2/Timer Z	$003F_{16}$	b2	$003D_{16}$	b2
INT_2	$003F_{16}$	b3	$003D_{16}$	b3
INT_3	$003F_{16}$	b4	$003D_{16}$	b4
INT_4/$CNTR_2$	$003F_{16}$	b5	$003D_{16}$	b5
A-D converter/Serial I/O3 transmission	$003F_{16}$	b6	$003D_{16}$	b6

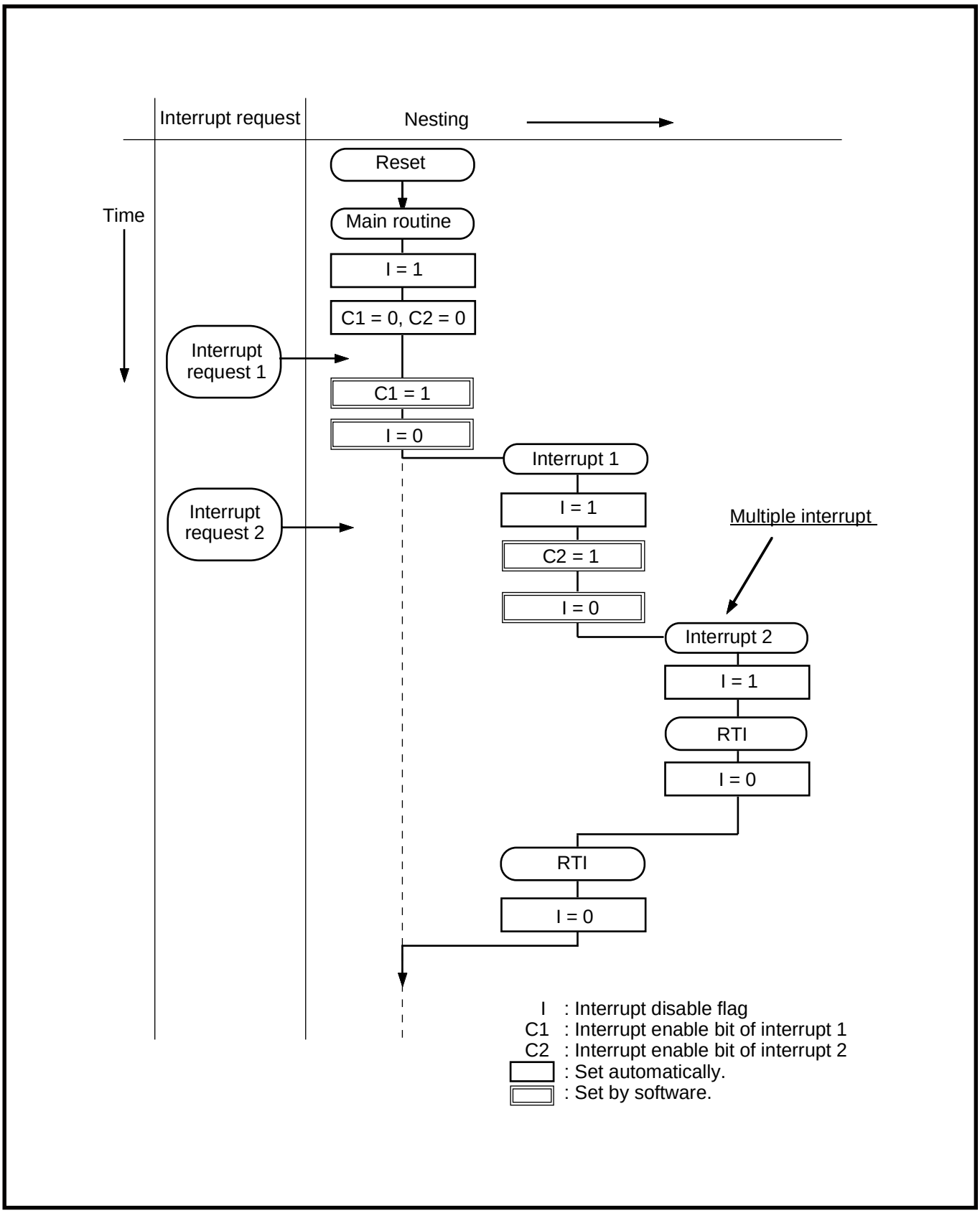


Fig. 2.2.13 Example of multiple interrupts

2.2.6 INT interrupt

The INT interrupt requests is generated when the microcomputer detects a level change of each INT pin (INT_0–INT_4).

(1) Active edge selection

INT_0–INT_4 can be selected from either a falling edge or rising edge detection as an active edge by the interrupt edge selection register. In the “0” state, the falling edge of the corresponding pin is detected. In the “1” state, the rising edge of the corresponding pin is detected.

(2) INT_0, INT_4 interrupt source selection

When using the following interrupt source, select which of the interrupt source by the interrupt source selection register (address 39_{16}). (Set these bits to “0” when using INT.)

- INT_0 or timer Z (bit 0)
- INT_4 or $CNTR_2$ (bit 4)

2.2.7 Notes on interrupts

(1) Change of relevant register settings

When the setting of the following registers or bits is changed, the interrupt request bit may be set to “1”. When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

•Interrupt edge selection register (address $003A_{16}$)
•Timer XY mode register (address 0023_{16})
•Timer Z mode register (address $002A_{16}$)

Set the above listed registers or bits as the following sequence.

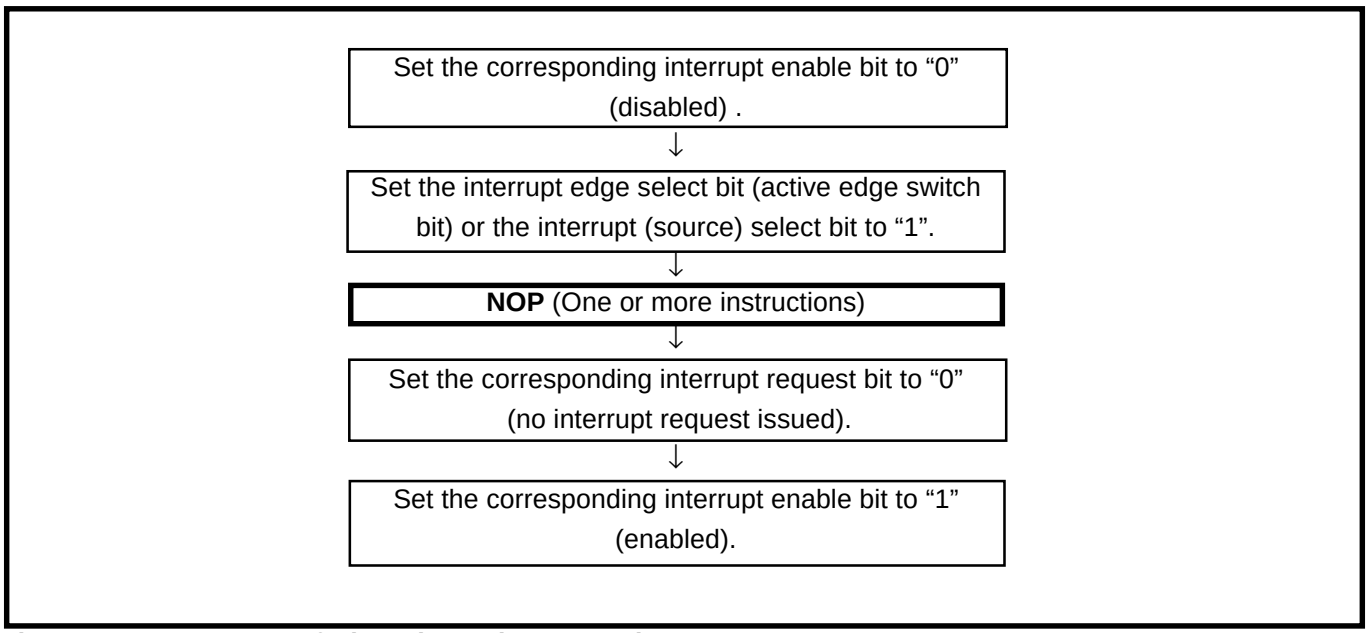


Fig. 2.2.14 Sequence of changing relevant register

■ **Reason**

When setting the followings, the interrupt request bit may be set to “1”.

•When setting external interrupt active edge
Concerned register: Interrupt edge selection register (address $003A_{16}$)
Timer XY mode register (address 0023_{16})
Timer Z mode register (address $002A_{16}$)

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated.
Concerned register: Interrupt source selection register (address 0039_{16})

(2) Check of interrupt request bit

- When executing the **BBC** or **BBS** instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to “0”, execute one or more instructions before executing the **BBC** or **BBS** instruction.

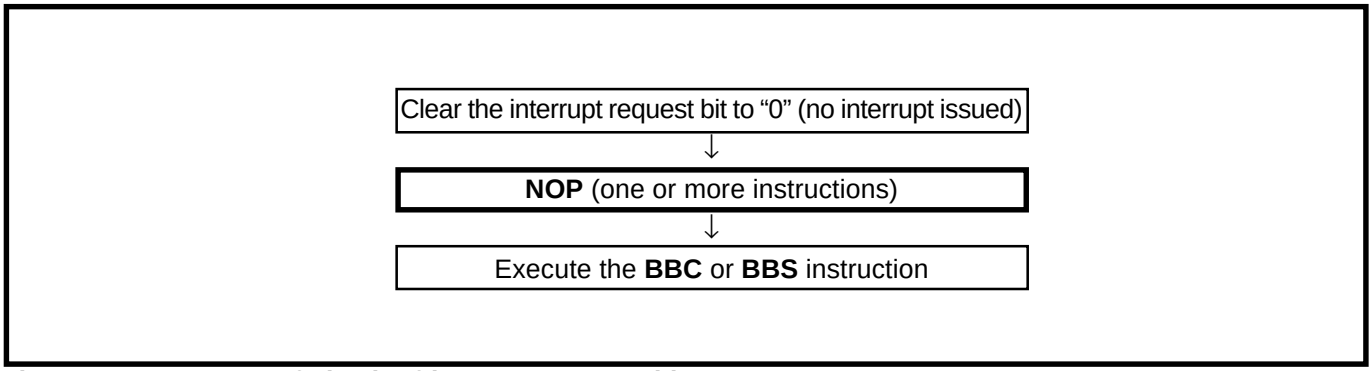


Fig. 2.2.15 Sequence of check of interrupt request bit

■ **Reason**

If the BBC or BBS instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to “0”, the value of the interrupt request bit before being cleared to “0” is read.

2.3 Timer

This paragraph explains the registers setting method and the notes relevant to the timers.

2.3.1 Memory map

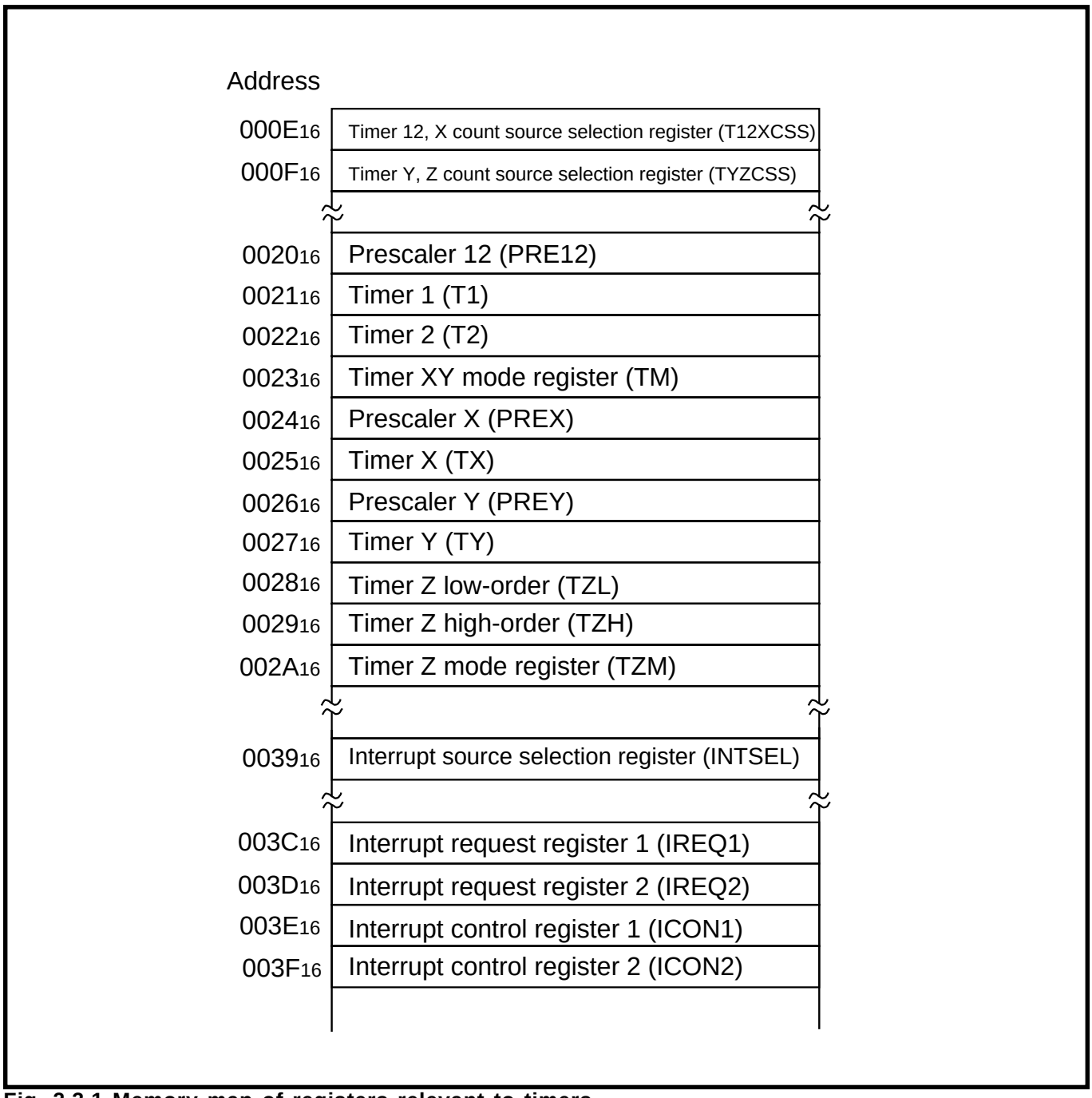


Fig. 2.3.1 Memory map of registers relevant to timers

2.3.2 Relevant registers

Prescaler 12, Prescaler X, Prescaler Y

b7 b6 b5 b4 b3 b2 b1 b0

Prescaler 12 (PRE12), Prescaler X (PREX), Prescaler Y (PREY)
(addresses 0020_{16}, 0024_{16}, 0026_{16})

b	Functions	At reset	R	W
0	• Set a count value of each prescaler. • The value set in this register is written to both each prescaler and the corresponding prescaler latch at the same time. • When this register is read out, the count value of the corresponding prescaler is read out.	1	○	○
1		1	○	○
2		1	○	○
3		1	○	○
4		1	○	○
5		1	○	○
6		1	○	○
7		1	○	○

Fig. 2.3.2 Structure of Prescaler 12, Prescaler X, Prescaler Y

Timer 1

b7 b6 b5 b4 b3 b2 b1 b0

Timer 1
(T1: address 0021_{16})

b	Functions	At reset	R	W
0	• Set timer 1 count value. • The value set in this register is written to both the timer 1 and the timer 1 latch at the same time. • When the timer 1 is read out, the count value of the timer 1 is read out.	1	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5		0	○	○
6		0	○	○
7		0	○	○

Fig. 2.3.3 Structure of Timer 1

Timer 2, Timer X, Timer Y

b7 b6 b5 b4 b3 b2 b1 b0

Timer 2 (T2), Timer X (TX), Timer Y (TY)
(addresses 0022_{16}, 0025_{16}, 0027_{16})

b	Functions	At reset	R	W
0	• Set each timer count value. • The value set in this register is written to both each timer and the corresponding timer latch at the same time. • When each timer is read out, the count value of the corresponding timer is read out.	1	○	○
1		1	○	○
2		1	○	○
3		1	○	○
4		1	○	○
5		1	○	○
6		1	○	○
7		1	○	○

Fig. 2.3.4 Structure of Timer 2, Timer X, Timer Y

Timer Z low-order, Timer Z high-order

b7 b6 b5 b4 b3 b2 b1 b0

Timer Z low-order (TZL), Timer Z high-order (TZH)
(addresses 0028_{16}, 0029_{16})

b	Functions	At reset	R	W
0	• Set each timer count value. [At write] • Depending on the write control bit (bit 3 of TZM), the value set to this register is written to each timer and the corresponding timer latch at the same time, or is written only to the latch. [At read] • The corresponding timer count value is read out by reading this register. • Read both registers in order of TZH and TZL following. • Write both registers in order of TZL and TZH following.	1	○	○
1		1	○	○
2		1	○	○
3		1	○	○
4		1	○	○
5		1	○	○
6		1	○	○
7		1	○	○

Fig. 2.3.5 Structure of Timer Z (low-order, high-order)

Timer XY mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer XY mode register
(TM: address 0023_{16})

b	Name	Functions	At reset	R	W
0	Timer X operating mode bits	b1 b0 0 0: Timer mode 0 1: Pulse output mode 1 0: Event counter mode 1 1: Pulse width measurement mode	0	○	○
1			0	○	○
2	$CNTR_0$ active edge switch bit	Refer to Table 2.3.1	0	○	○
3	Timer X count stop bit	0: Count start 1: Count stop	0	○	○
4	Timer Y operating mode bits	b5 b4 0 0: Timer mode 0 1: Pulse output mode 1 0: Event counter mode 1 1: Pulse width measurement mode	0	○	○
5			0	○	○
6	$CNTR_1$ active edge switch bit	Refer to Table 2.3.1	0	○	○
7	Timer Y count stop bit	0: Count start 1: Count stop	0	○	○

Fig. 2.3.6 Structure of Timer XY mode register

Table 2.3.1 $CNTR_0$ /$CNTR_1$ active edge switch bit function

Timer X /Timer Y operation modes	$CNTR_0$ / $CNTR_1$ active edge switch bit (0023_{16}) contents	
Timer mode	"0"	$CNTR_0$ / $CNTR_1$ interrupt request occurrence: Falling edge ; No influence to timer count
	"1"	$CNTR_0$ / $CNTR_1$ interrupt request occurrence: Rising edge ; No influence to timer count
Pulse output mode	"0"	Pulse output start: Beginning at "H" level $CNTR_0$ / $CNTR_1$ interrupt request occurrence: Falling edge
	"1"	Pulse output start: Beginning at "L" level $CNTR_0$ / $CNTR_1$ interrupt request occurrence: Rising edge
Event counter mode	"0"	Timer X / Timer Y: Rising edge count $CNTR_0$ / $CNTR_1$ interrupt request occurrence: Falling edge
	"1"	Timer X / Timer Y: Falling edge count $CNTR_0$ / $CNTR_1$ interrupt request occurrence: Rising edge
Pulse width measurement mode	"0"	Timer X / Timer Y: "H" level width measurement $CNTR_0$ / $CNTR_1$ interrupt request occurrence: Falling edge
	"1"	Timer X / Timer Y: "L" level width measurement $CNTR_0$ / $CNTR_1$ interrupt request occurrence: Rising edge

Timer Z mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer Z mode register
(TZM: address 002A16)

b	Name	Functions	At reset	R	W
0	Timer Z operating mode bits	b2b1b0 0 0 0: Timer/Event counter mode 0 0 1: Pulse output mode 0 1 0: Pulse period measurement mode 0 1 1: Pulse width measurement mode 1 0 0: Programmable waveform generating mode 1 0 1: Programmable one-shot generating mode 1 1 0: Not available 1 1 1: Not available	0	○	○
1			0	○	○
2			0	○	○
3	Timer Z write control bit	0: Writing data to both latch and timer simultaneousuly 1: Writing data only to latch	0	○	○
4	Output level latch	0: "L" output 1: "H" output	0	○	○
5	$CNTR_2$ active edge switch bit	Refer to Table 2.3.2.	0	○	○
6	Timer Z count stop bit	0: Count start 1: Count stop	0	○	○
7	Timer/Event counter mode switch bit **(Note)**	0: Timer mode 1: Event counter mode	0	○	○

Note: When selecting the modes except the timer/event counter mode, set "0" to this bit.

Fig. 2.3.7 Structure of Timer Z mode register

Table 2.3.2 $CNTR_2$ active edge switch bit function

Timer Z operation modes	$CNTR_2$ active edge switch bit (bit 5 of address $002A_{16}$) contents	
Timer mode	"0"	$CNTR_2$ interrupt request occurrence: Falling edge ; No influence to timer count
	"1"	$CNTR_2$ interrupt request occurrence: Rising edge ; No influence to timer count
Event counter mode	"0"	Timer Z: Rising edge count $CNTR_2$ interrupt request occurrence: Falling edge
	"1"	Timer Z: Falling edge count $CNTR_2$ interrupt request occurrence: Rising edge
Pulse output mode	"0"	Pulse output start: Beginning at "H" level $CNTR_2$ interrupt request occurrence: Falling edge
	"1"	Pulse output start: Beginning at "L" level $CNTR_2$ interrupt request occurrence: Rising edge
Pulse period measurement mode	"0"	Timer Z : Term from one falling edge to next falling edge measurement $CNTR_2$ interrupt request occurrence: Falling edge
	"1"	Timer Z : Term from one rising edge to next rising edge measurement $CNTR_2$ interrupt request occurrence: Rising edge
Pulse width measurement mode	"0"	Timer Z: "H" level width measurement $CNTR_2$ interrupt request occurrence: Falling edge
	"1"	Timer Z: "L" level width measurement $CNTR_2$ interrupt request occurrence: Rising edge
Programmable one-shot generating mode	"0"	Timer Z : Pulse output start from "L" level, and "H" level one-shot pulse is output. $CNTR_2$ interrupt request occurrence: Falling edge
	"1"	Timer Z : Pulse output start from "H" level, and "L" level one-shot pulse is output. $CNTR_2$ interrupt request occurrence: Rising edge

Timer 12, X count source selection register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 12, X count source selection register
(T12XCSS: address $000E_{16}$)

b	Name	Functions	At reset	R	W
0	Timer 12 count source selection bits	b3b2b1b0 0 0 0 0: f(XIN)/2 or f(XCIN)/2 0 0 0 1: f(XIN)/4 or f(XCIN)/4 0 0 1 0: f(XIN)/8 or f(XCIN)/8 0 0 1 1: f(XIN)/16 or f(XCIN)/16 0 1 0 0: f(XIN)/32 or f(XCIN)/32 0 1 0 1: f(XIN)/64 or f(XCIN)/64 0 1 1 0: f(XIN)/128 or f(XCIN)/128 0 1 1 1: f(XIN)/256 or f(XCIN)/256 1 0 0 0: f(XIN)/512 or f(XCIN)/512 1 0 0 1: f(XIN)/1024 or f(XCIN)/1024 1010 to 1111: Not available	1	○	○
1			1	○	○
2			0	○	○
3			0	○	○
4	Timer X count source selection bits	b7b6b5b4 0 0 0 0: f(XIN)/2 or f(XCIN)/2 0 0 0 1: f(XIN)/4 or f(XCIN)/4 0 0 1 0: f(XIN)/8 or f(XCIN)/8 0 0 1 1: f(XIN)/16 or f(XCIN)/16 0 1 0 0: f(XIN)/32 or f(XCIN)/32 0 1 0 1: f(XIN)/64 or f(XCIN)/64 0 1 1 0: f(XIN)/128 or f(XCIN)/128 0 1 1 1: f(XIN)/256 or f(XCIN)/256 1 0 0 0: f(XIN)/512 or f(XCIN)/512 1 0 0 1: f(XIN)/1024 or f(XCIN)/1024 1 0 1 0: f(XCIN) 1011 to 1111: Not available	1	○	○
5			1	○	○
6			0	○	○
7			0	○	○

Fig. 2.3.8 Structure of Timer 12, X count source selection register

Timer Y, Z count source selection register

b7 b6 b5 b4 b3 b2 b1 b0

Timer Y, Z count source selection register
(TYZCSS: address $000F_{16}$)

b	Name	Functions	At reset	R	W
0	Timer Y count source selection bits	b3b2b1b0 0 0 0 0: f(XIN)/2 or f(XCIN)/2 0 0 0 1: f(XIN)/4 or f(XCIN)/4 0 0 1 0: f(XIN)/8 or f(XCIN)/8 0 0 1 1: f(XIN)/16 or f(XCIN)/16 0 1 0 0: f(XIN)/32 or f(XCIN)/32 0 1 0 1: f(XIN)/64 or f(XCIN)/64 0 1 1 0: f(XIN)/128 or f(XCIN)/128 0 1 1 1: f(XIN)/256 or f(XCIN)/256 1 0 0 0: f(XIN)/512 or f(XCIN)/512 1 0 0 1: f(XIN)/1024 or f(XCIN)/1024 1 0 1 0: f(XCIN) 1011 to 1111: Not available	1	○	○
1			1	○	○
2			0	○	○
3			0	○	○
4	Timer Z count source selection bits	b7b6b5b4 0 0 0 0: f(XIN)/2 or f(XCIN)/2 0 0 0 1: f(XIN)/4 or f(XCIN)/4 0 0 1 0: f(XIN)/8 or f(XCIN)/8 0 0 1 1: f(XIN)/16 or f(XCIN)/16 0 1 0 0: f(XIN)/32 or f(XCIN)/32 0 1 0 1: f(XIN)/64 or f(XCIN)/64 0 1 1 0: f(XIN)/128 or f(XCIN)/128 0 1 1 1: f(XIN)/256 or f(XCIN)/256 1 0 0 0: f(XIN)/512 or f(XCIN)/512 1 0 0 1: f(XIN)/1024 or f(XCIN)/1024 1 0 1 0: f(XCIN) 1011 to 1111: Not available	1	○	○
5			1	○	○
6			0	○	○
7			0	○	○

Fig. 2.3.9 Structure of Timer Y, Z count source selection register

Interrupt source selection register

Interrupt source selection register
(INTSEL: address 0039_{16})

b	Name	Functions	At reset	R	W
0	INT_0/Timer Z interrupt source selection bit (*1)	0: INT_0 interrupt 1: Timer Z interrupt	0	○	○
1	Serial I/O2/Timer Z interrupt source selection bit (*1)	0: Serial I/O2 interrupt 1: Timer Z interrupt	0	○	○
2	Nothing is arranged for these bits. Do not write “1” to these bits. When these bits are read out, the contents are “0”.		0	○	○
3			0	○	○
4	INT_4/$CNTR_2$ interrupt source selection bit	0: INT_4 interrupt 1: $CNTR_2$ interrupt	0	○	○
5	Nothing is arranged for this bit. Do not write “1” to this bit. When this bit is read out, the contents are “0”.		0	○	○
6	$CNTR_1$/Serial I/O3 receive interrupt source selection bit	0: $CNTR_1$ interrupt 1: Serial I/O3 receive interrupt	0	○	○
7	AD converter/Serial I/O3 transmit interrupt source selection bit	0: A-D converter interrupt 1: Serial I/O3 transmit interrupt	0	○	○

*1: Do not write “1” to these bits simultaneously.

Fig. 2.3.10 Structure of Interrupt source selection register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1
(IREQ1 : address 003C16)

b	Name	Functions	At reset	R	W
0	INT0/Timer Z interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	INT1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	Serial I/O1 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	Serial I/O1 transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	Timer X interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	Timer Y interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Timer 2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻

✻: "0" can be set by software, but "1" cannot be set.

Fig. 2.3.11 Structure of Interrupt request register 1

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2
(IREQ2 : address 003D16)

b	Name	Functions	At reset	R	W
0	CNTR0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	CNTR1/Serial I/O3 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	Serial I/O2/Timer Z interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	INT2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	INT3 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	INT4/CNTR2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	AD converter/Serial I/O3 transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	×

✻: "0" can be set by software, but "1" cannot be set.

Fig. 2.3.12 Structure of Interrupt request register 2

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1
(ICON1 : address 003E16)

b	Name	Functions	At reset	R	W
0	INT0/Timer Z interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Serial I/O1 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Serial I/O1 transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Timer X interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Timer Y interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.3.13 Structure of Interrupt control register 1

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 2
(ICON2 : address 003F16)

b	Name	Functions	At reset	R	W
0	CNTR0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	CNTR1/ Serial I/O3 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Serial I/O2/ Timer Z interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	INT2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT3 interrupt enable bit	0 : Interrupt disabled	0	○	○
5	INT4/CNTR2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	AD converter/Serial I/O3 transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to “0”.		0	○	○

Fig. 2.3.14 Structure of Interrupt control register 2

2.3.3 Timer application examples

(1) Basic functions and uses

[Function 1] Control of Event interval (Timer X, Timer Y, Timer Z, Timer 1, Timer 2)

When a certain time, by setting a count value to each timer, has passed, the timer interrupt request occurs.

<Use>

- •Generation of an output signal timing
- •Generation of a wait time

[Function 2] Control of Cyclic operation (Timer X, Timer Y, Timer Z, Timer 1, Timer 2)

The value of the timer latch is automatically written to the corresponding timer each time the timer underflows, and each timer interrupt request occurs in cycles.

<Use>

- •Generation of cyclic interrupts
- •Clock function (measurement of 250 ms); see Application example 1
- •Control of a main routine cycle

[Function 3] Output of Rectangular waveform (Timer X, Timer Y, Timer Z)

The output level of the CNTR pin is inverted each time the timer underflows (in the pulse output mode).

<Use>

- •Piezoelectric buzzer output; see Application example 2
- •Generation of the remote control carrier waveforms

[Function 4] Count of External pulses (Timer X, Timer Y, Timer Z)

External pulses input to the CNTR pin are counted as the timer count source (in the event counter mode).

<Use>

- •Frequency measurement; see Application example 3
- •Division of external pulses
- •Generation of interrupts due to a cycle using external pulses as the count source; count of a reel pulse

[Function 5] Measurement of External pulse width (Timer X, Timer Y, Timer Z)

The “H” or “L” level width of external pulses input to CNTR pin is measured (in the pulse width measurement mode).

<Use>

- •Measurement of external pulse frequency (measurement of pulse width of FG pulse* for a motor); see Application example 4
- •Measurement of external pulse duty (when the frequency is fixed)

FG pulse*: Pulse used for detecting the motor speed to control the motor speed.

[Function 6] Output of Arbitrary waveform (Timer Z)

The value which is set to the output level latch is output from the CNTR pin each time the timer underflows. (programmable waveform generating mode)

[Function 7] One-shot pulse output by external trigger (Timer Z)

The value of timer latch is set to timer by trigger signal which is input from the INT pin, and timer is counted down. When trigger signal is input, “H” or “L” is output from the CNTR pin at the same time, and “L” or “H” is output by underflow of timer. (programmable one-shot generating mode)

(2) Timer application example 1: Clock function (measurement of 250 ms)

Outline: The input clock is divided by the timer so that the clock can count up at 250 ms intervals.

Specifications: •The clock f(X_{IN}) = 4.19 MHz (2^{22} Hz) is divided by the timer.
•The clock is counted up in the process routine of the timer X interrupt which occurs at 250 ms intervals.

Figure 2.3.15 shows the timers connection and setting of division ratios; Figure 2.3.16 shows the relevant registers setting; Figure 2.3.17 shows the control procedure.

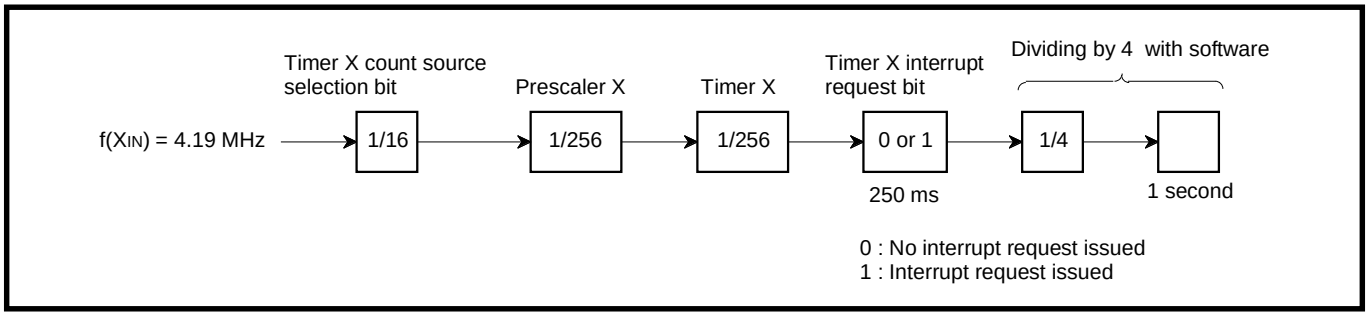


Fig. 2.3.15 Timers connection and setting of division ratios

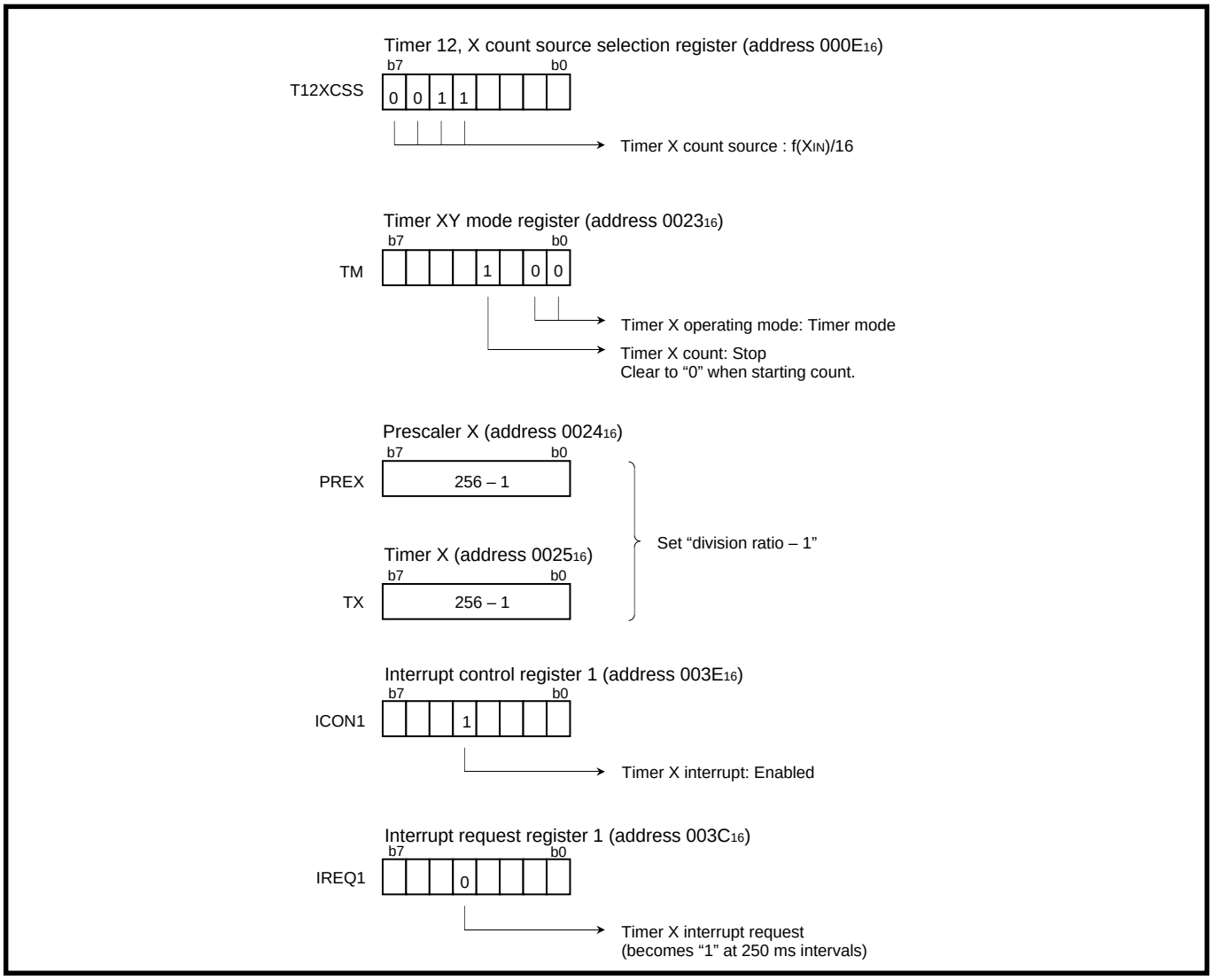


Fig. 2.3.16 Relevant registers setting

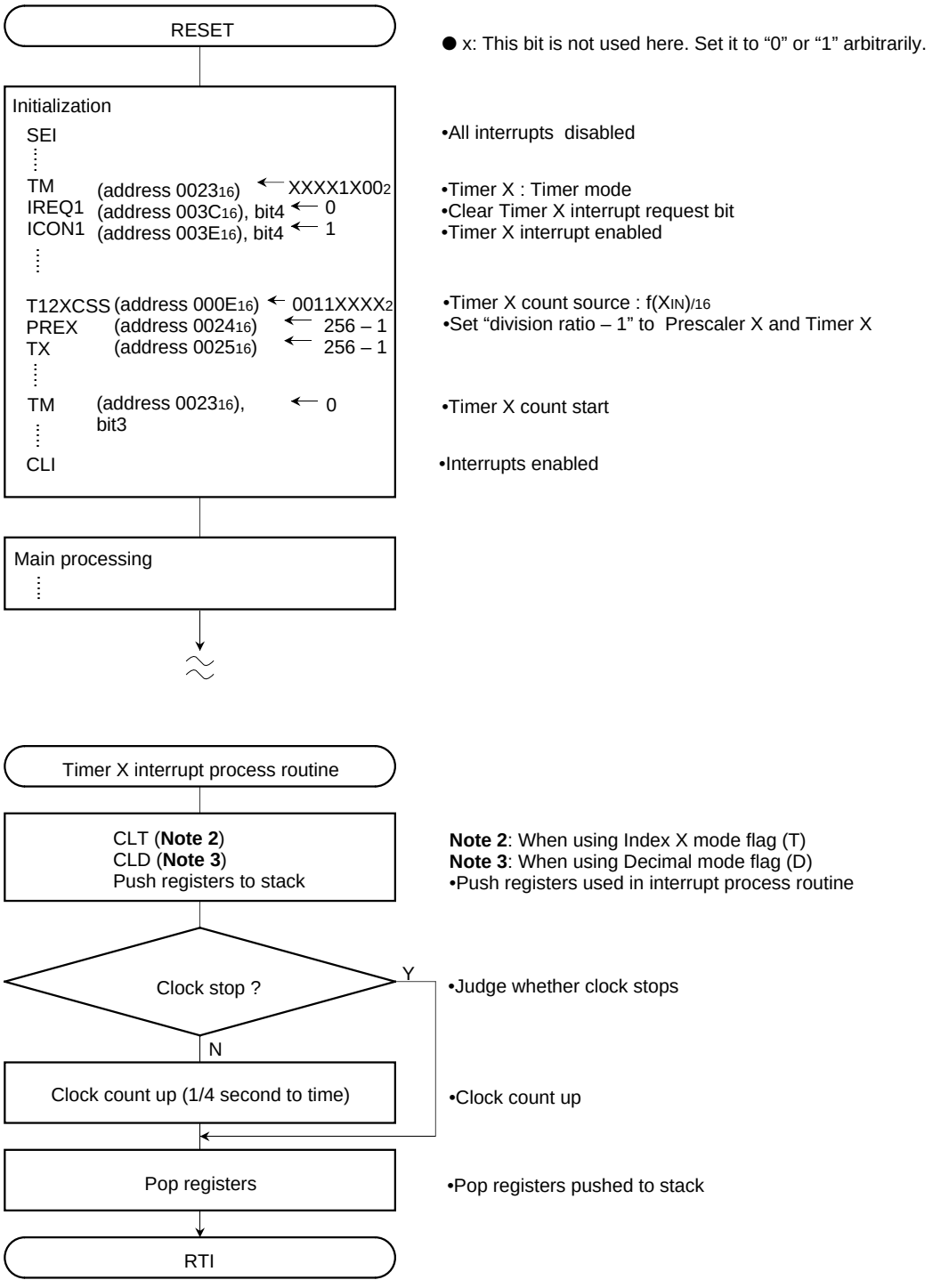


Fig. 2.3.17 Control procedure

(3) Timer application example 2: Piezoelectric buzzer output

Outline: The rectangular waveform output function of the timer is applied for a piezoelectric buzzer output.

Specifications: •The rectangular waveform, dividing the clock f(X_{IN}) = 8 MHz into about 2 kHz (2049 Hz), is output from the $P4_7/CNTR_2$ pin.
•The level of the $P4_7/CNTR_2$ pin is fixed to "H" while a piezoelectric buzzer output stops.

Figure 2.3.18 shows a peripheral circuit example, and Figure 2.3.19 shows the timers connection and setting of division ratios. Figure 2.3.20 shows the relevant registers setting, and Figure 2.3.21 shows the control procedure.

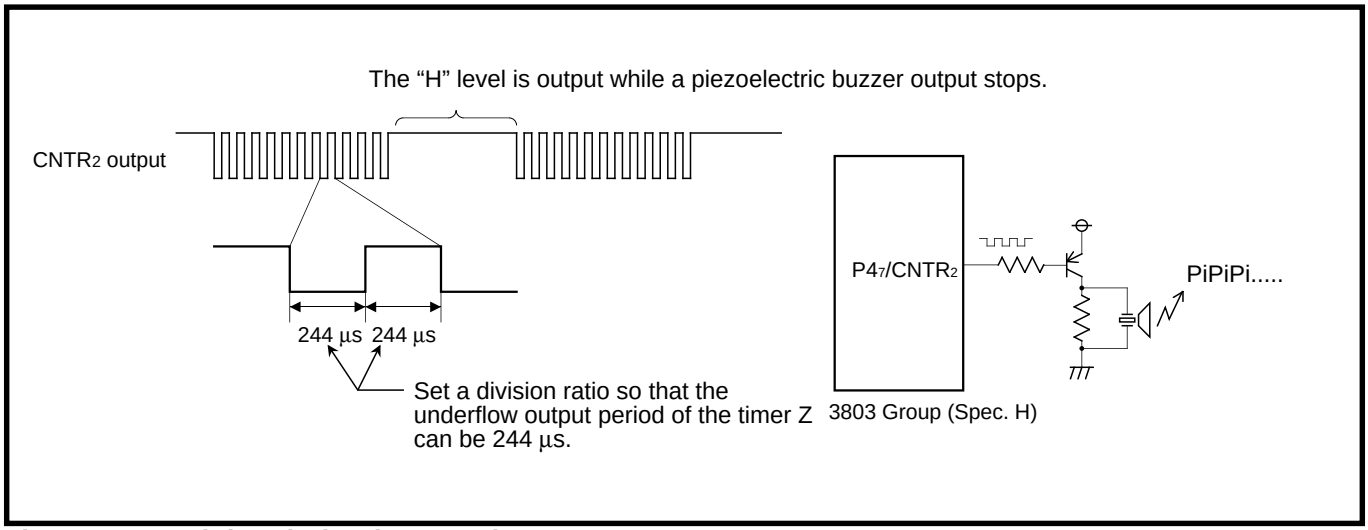


Fig. 2.3.18 Peripheral circuit example

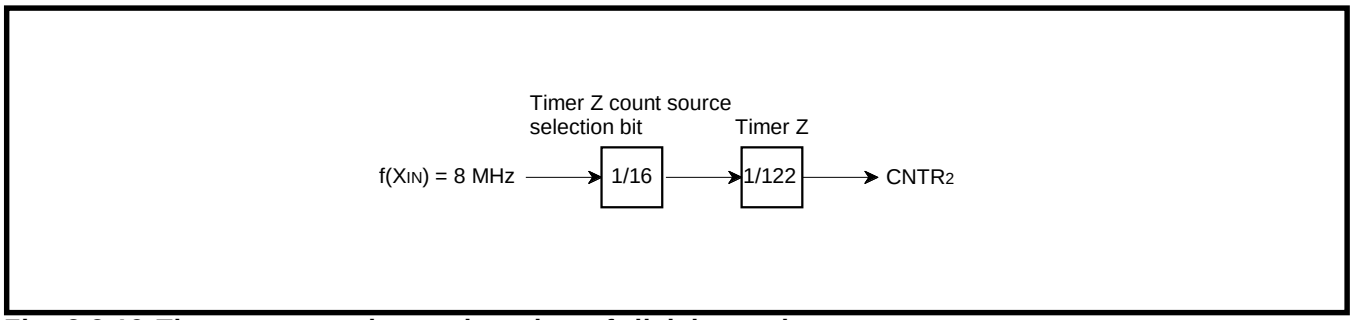


Fig. 2.3.19 Timers connection and setting of division ratios

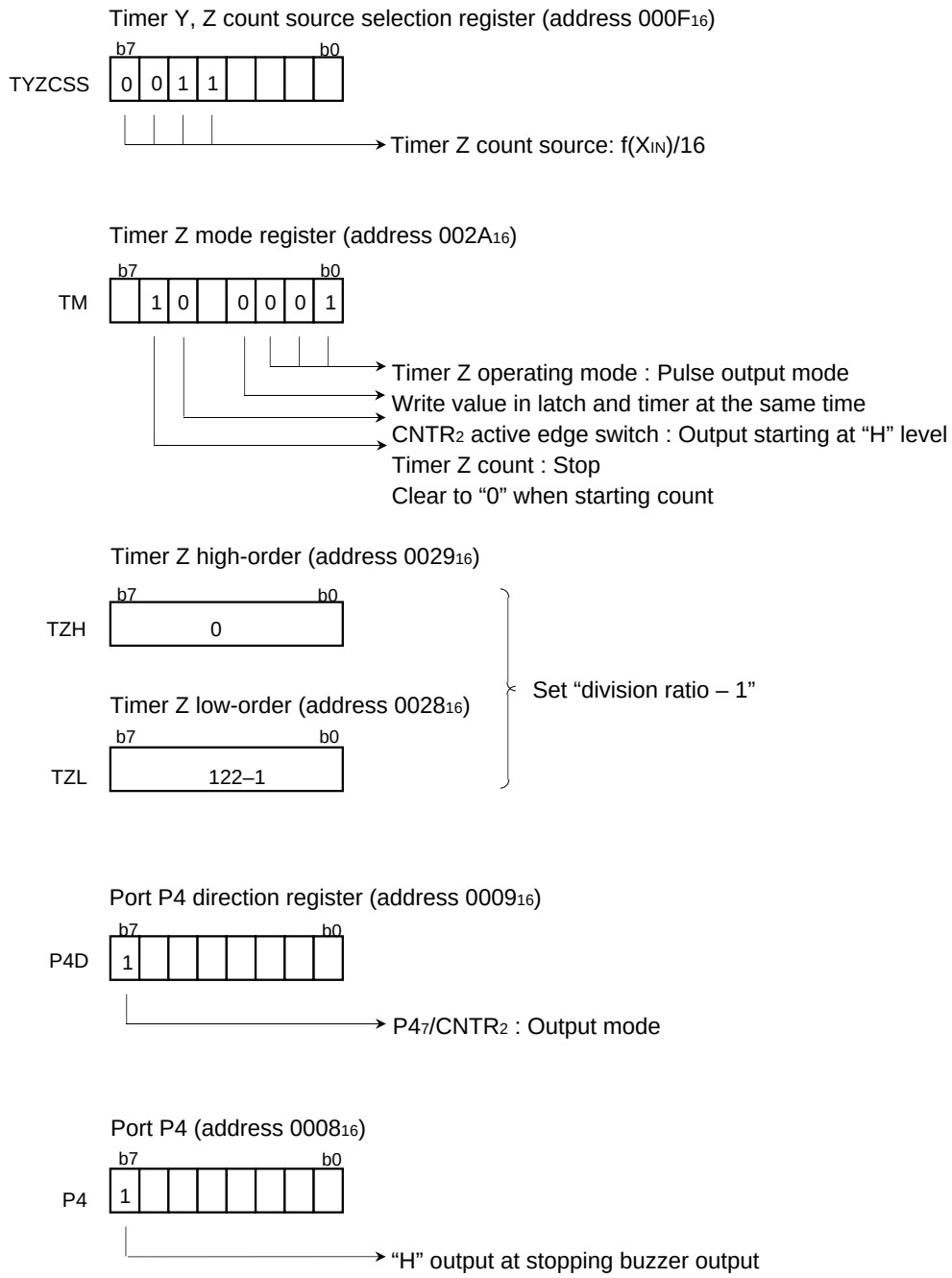


Fig. 2.3.20 Relevant registers setting

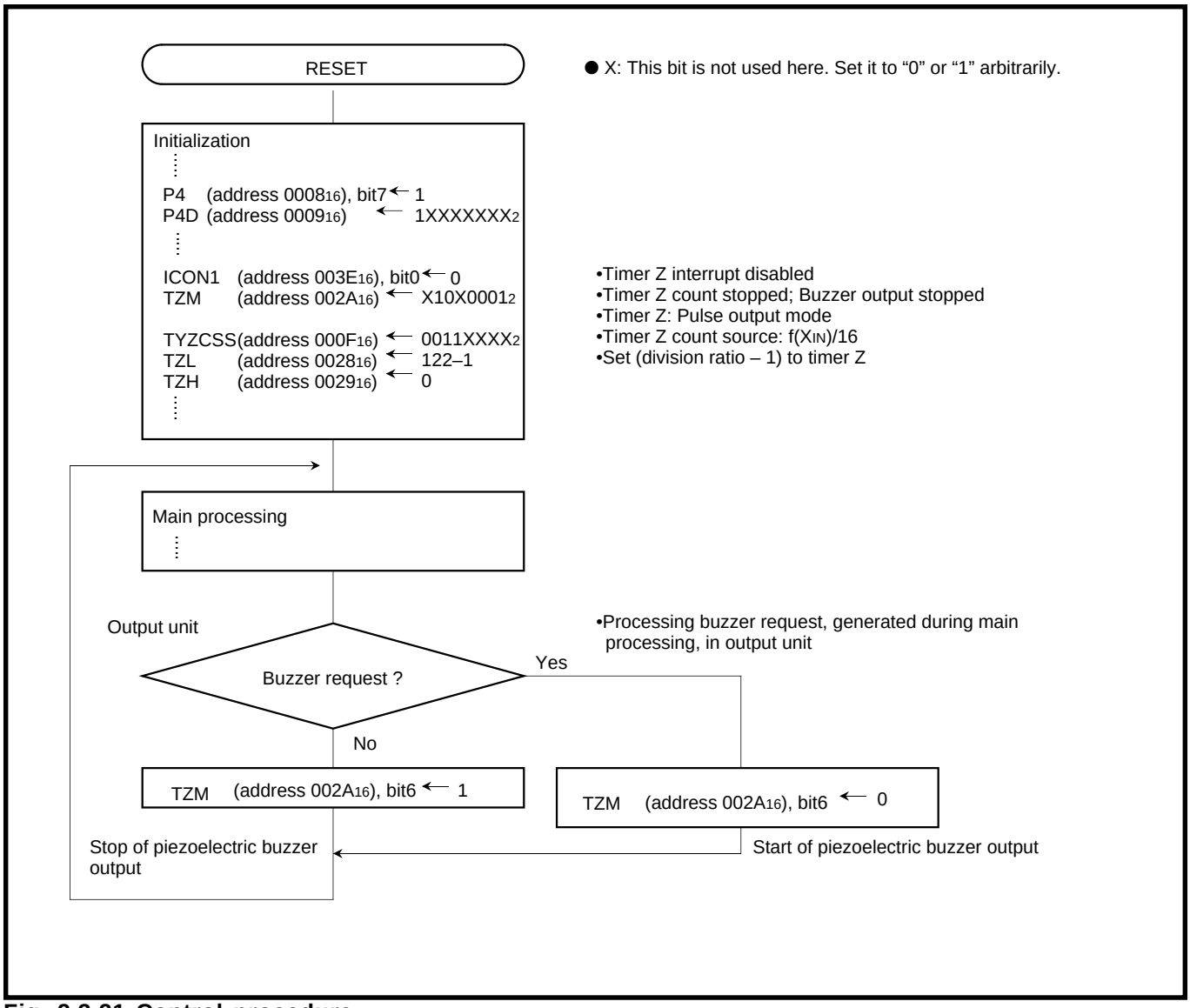


Fig. 2.3.21 Control procedure

(4) Timer application example 3: Frequency measurement

Outline: The following two values are compared to judge whether the frequency is within a valid range.
- •A value by counting pulses input to $P5_5/CNTR_1$ pin with the timer.
- •A reference value

Specifications: •The pulse is input to the $P5_5/CNTR_1$ pin and counted by the timer Y.
- •The clock f(X_{IN}) = 8 MHz is dividing by the timer 1, and the interrupt request occurs at about 2 ms intervals.
- •A count value is read out at about 2 ms intervals, the timer 1 interrupt interval. When the count value is 28 to 40, it is judged that the input pulse is valid.
- •Because the timer is a down-counter, the count value is compared with 227 to 215 **(Note)**.

Note: 227 to 215 = {255 (initial value of counter) – 28} to {255 – 40}; 28 to 40 means the number of valid count value.

Figure 2.3.22 shows the judgment method of valid/invalid of input pulses; Figure 2.3.23 shows the relevant registers setting; Figure 2.3.24 shows the control procedure.

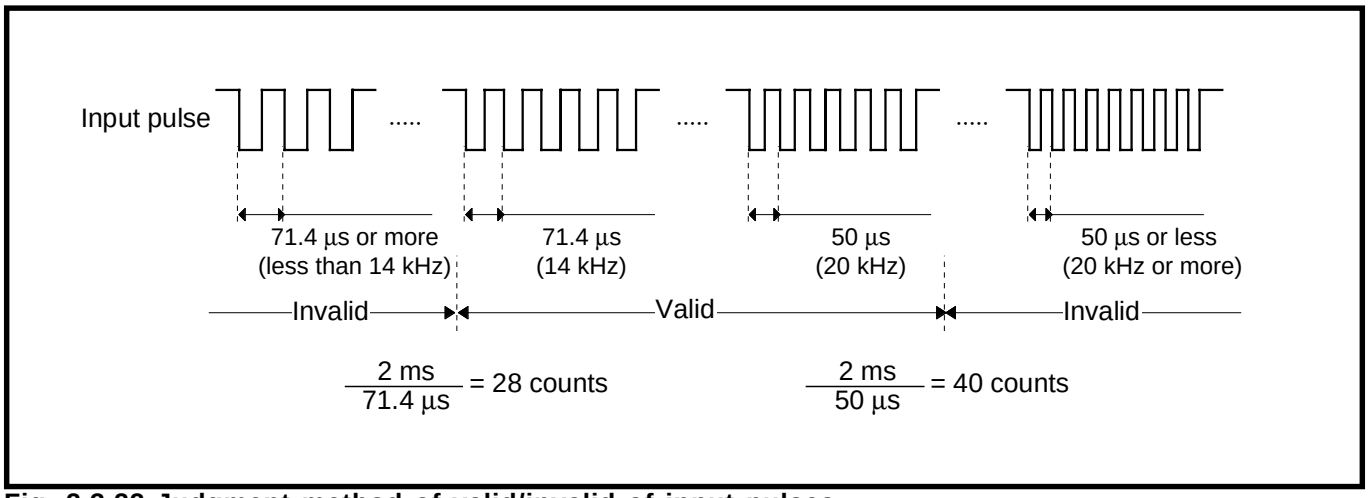


Fig. 2.3.22 Judgment method of valid/invalid of input pulses

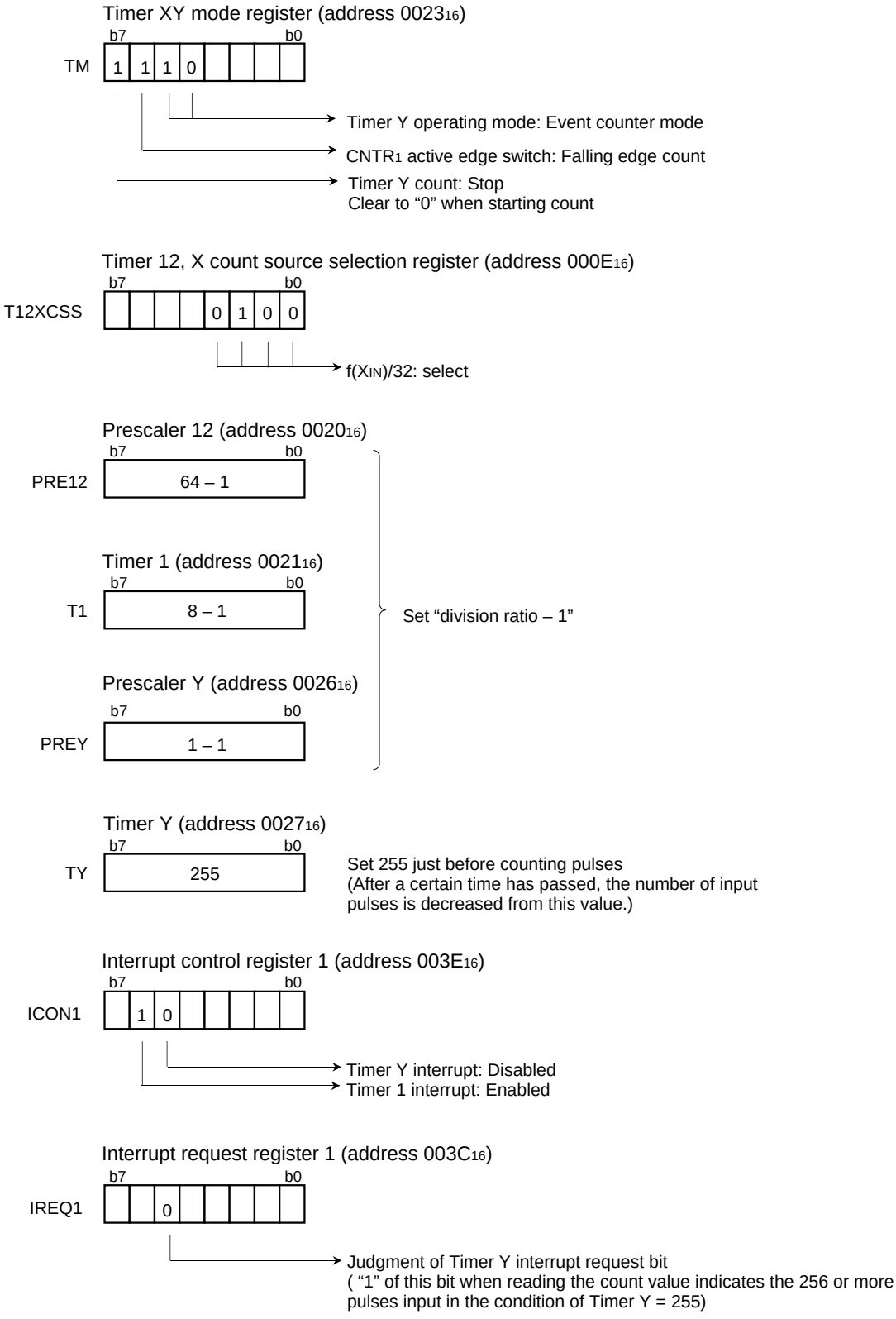


Fig. 2.3.23 Relevant registers setting

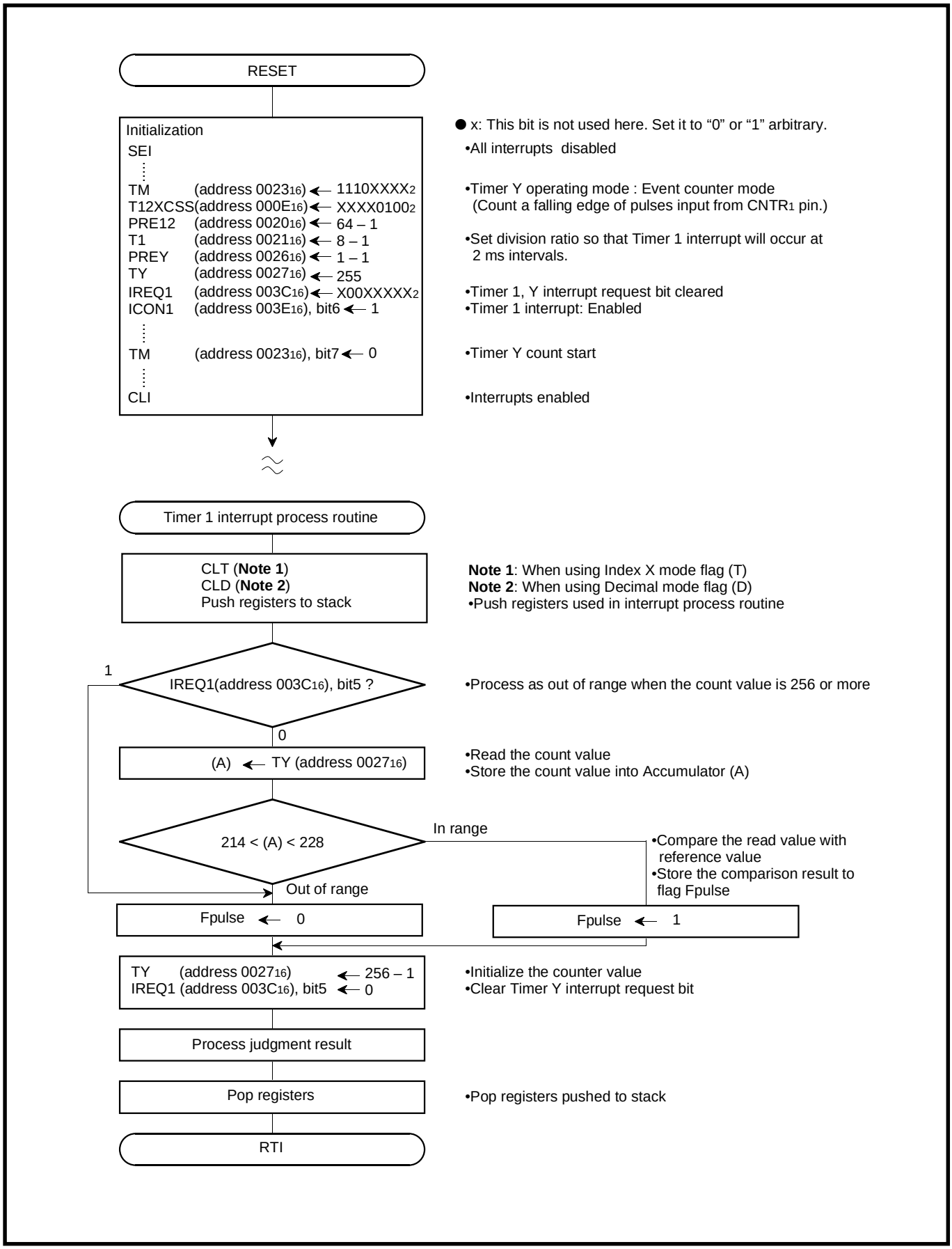


Fig. 2.3.24 Control procedure

(5) Timer application example 4: Measurement of FG pulse width for motor

Outline: The timer Z counts the “H” level width of the pulses input to the $P4_7/CNTR_2$ pin. An underflow is detected by the timer Z interrupt and an end of the input pulse “H” level is detected by the $P4_7/CNTR_2$ interrupt.

Specifications: •The timer Z counts the “H” level width of the FG pulse input to the $P4_7/CNTR_2$ pin.

<Example>

When the clock frequency is 8 MHz, the count source is 2 µs, which is obtained by dividing the clock frequency by 16. Measurement can be made up to 131.072 ms in the range of $FFFF_{16}$ to 0000_{16}.

Figure 2.3.25 shows the timers connection and setting of division ratio; Figure 2.3.26 shows the relevant registers setting; Figure 2.3.27 and Figure 2.3.28 show the control procedure.

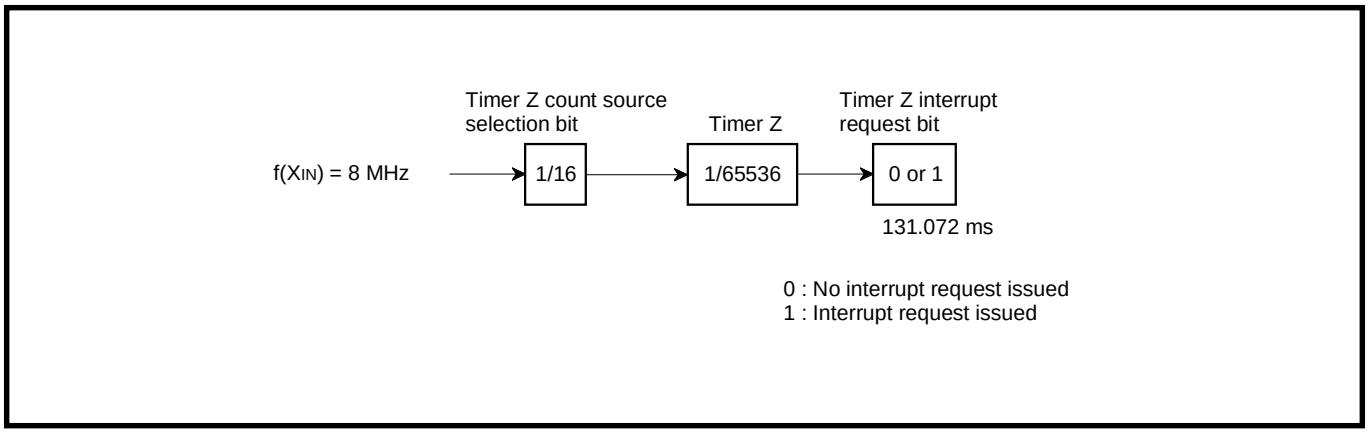


Fig. 2.3.25 Timers connection and setting of division ratios

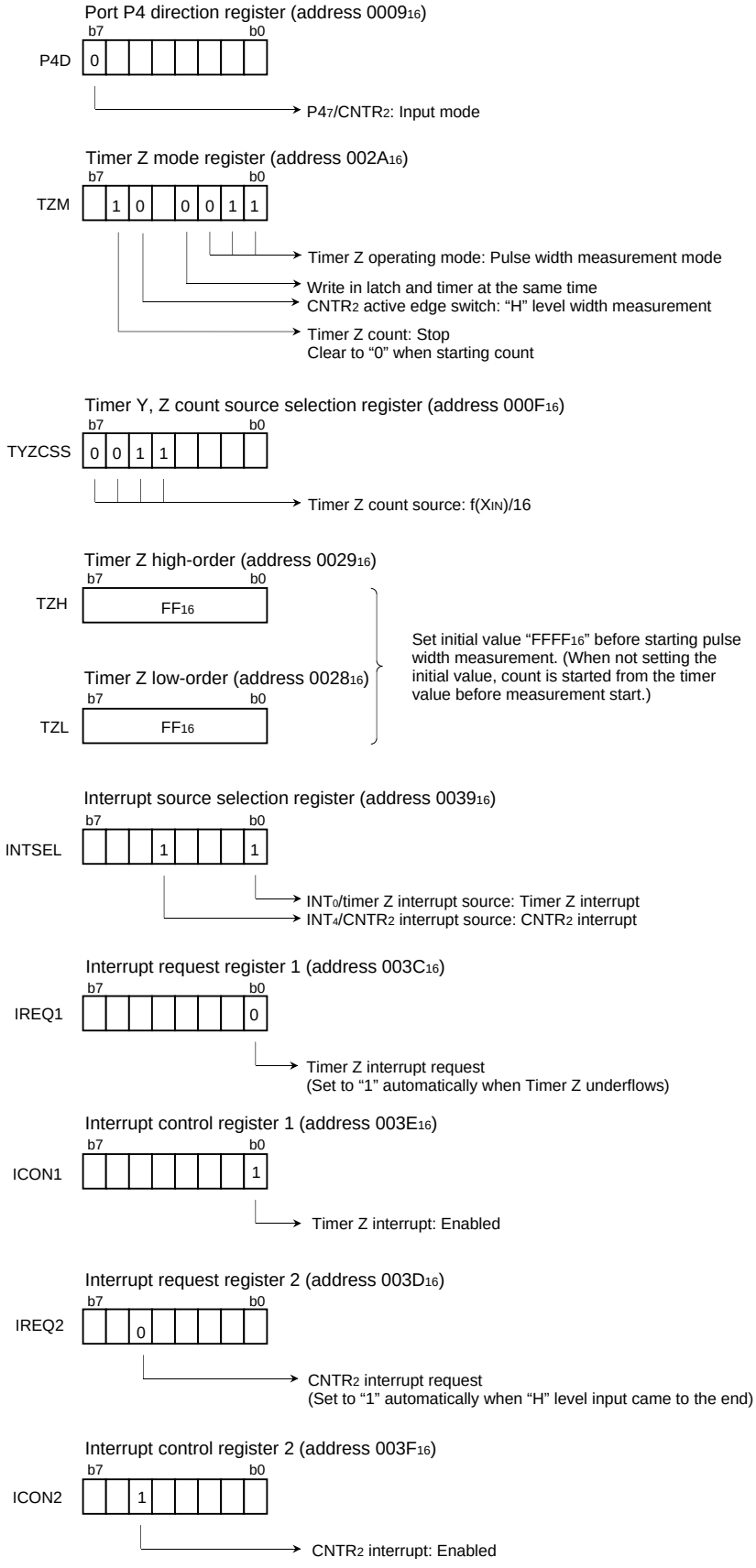
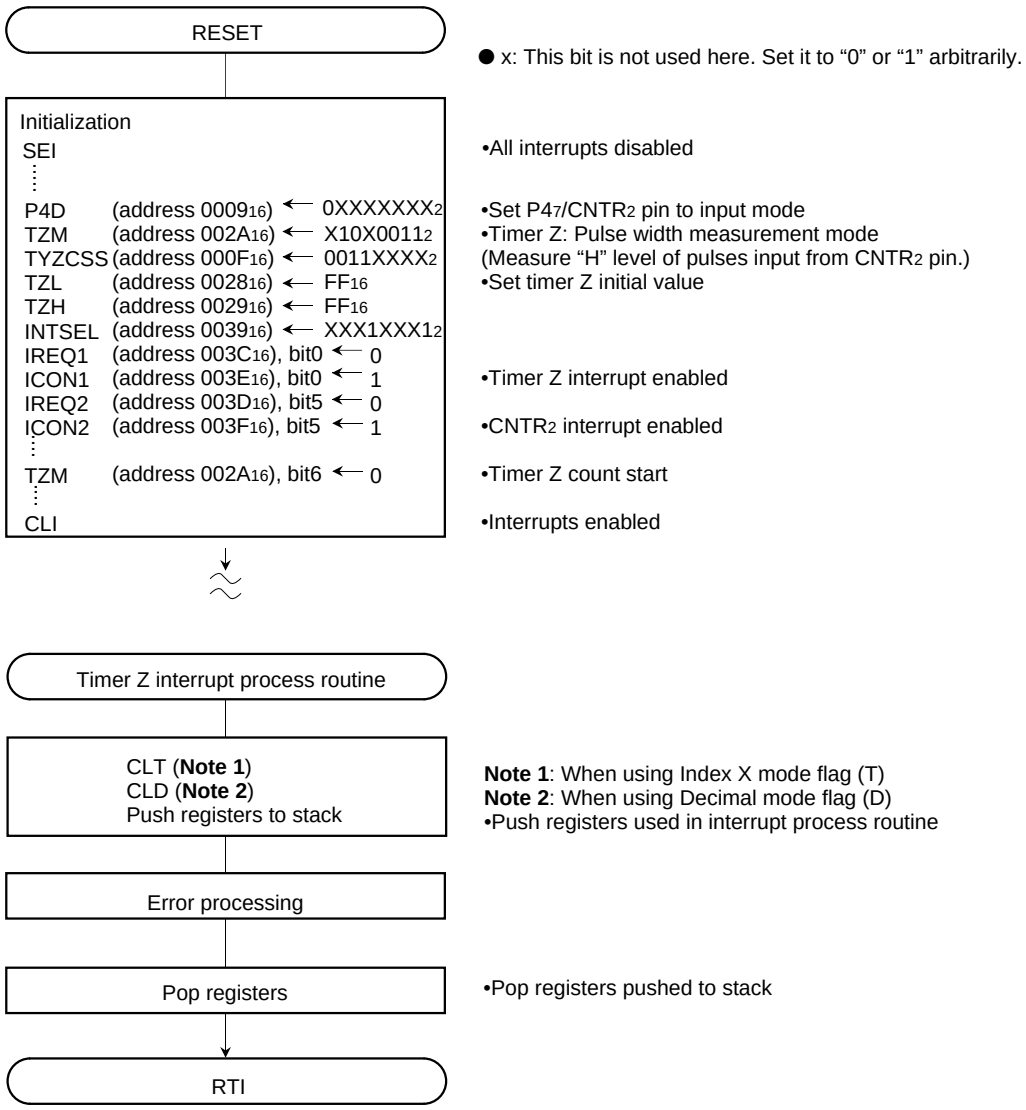
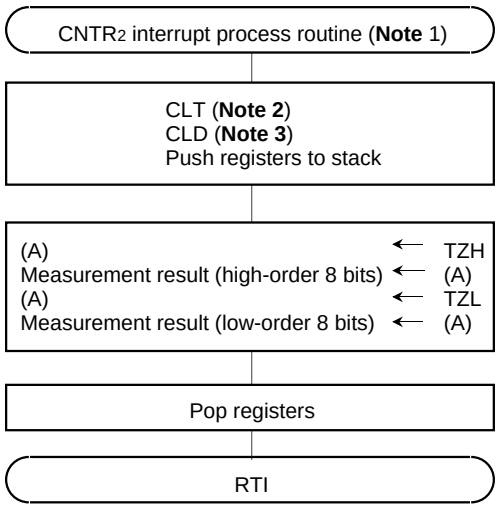


Fig. 2.3.26 Relevant registers setting



Note: Timer Z interrupt also occurs owing to factors other than measurement level. ($CNTR_2$ input =“L” in this application)
Process it by software as error processing is performed for measurement level as necessary. ($CNTR_2$ input level can be checked by reading the contents of sharing port $P4_7$ register.)

Fig. 2.3.27 Control procedure (1)



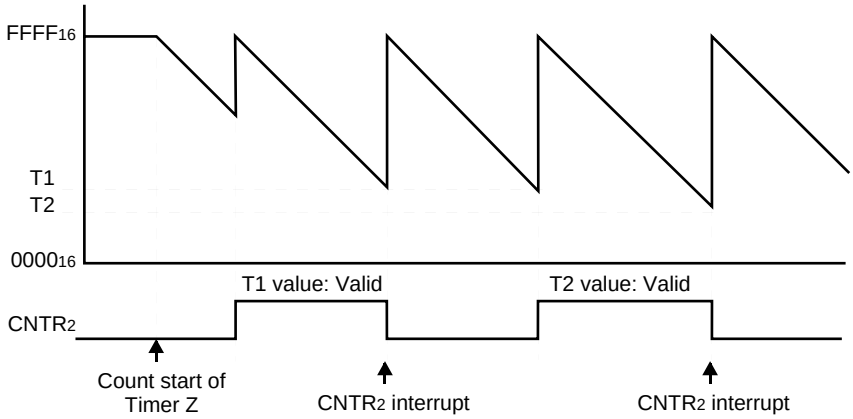
Notes **2**: When using Index X mode flag (T)
3: When using Decimal mode flag (D)
•Pushing registers used in interrupt process routine

•Count value read and storing it to RAM

•Popping registers pushed to stack

Note 1: The first value becomes invalid depending on start timing of Timer Z count shown by the following figure.
Process it by software as necessary.

[Example 1] • Start Timer Z count when $CNTR_2$ input level is "L".
($CNTR_2$ input level can be checked by reading the contents of sharing port $P4_7$ register.)



[Example 2] • Start Timer Z count when $CNTR_2$ input level is "H".
Invalidate the first $CNTR_2$ interrupt after start of Timer Z count.

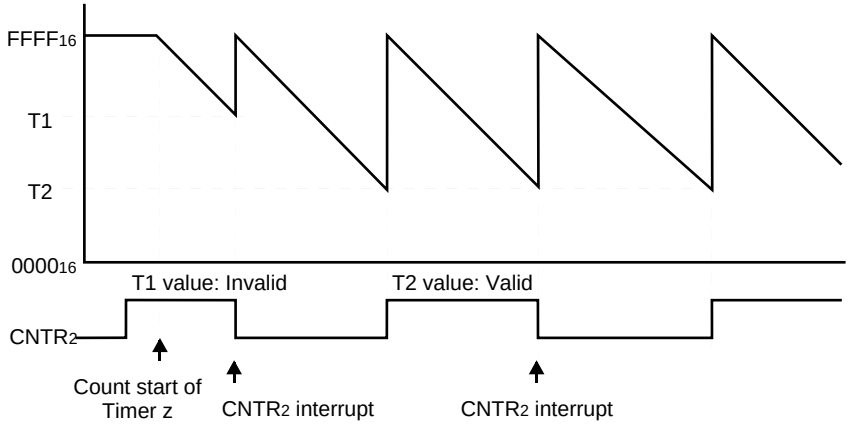


Fig. 2.3.28 Control procedure (2)

2.3.4 Notes on timer

- If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in unconsiderable amount owing to generating of thin pulses in the count input signals.
  Therefore, select the timer count source before set the value to the prescaler and the timer.

2.4 Serial I/O

This paragraph explains the registers setting method and the notes relevant to Serial I/O.

2.4.1 Memory map

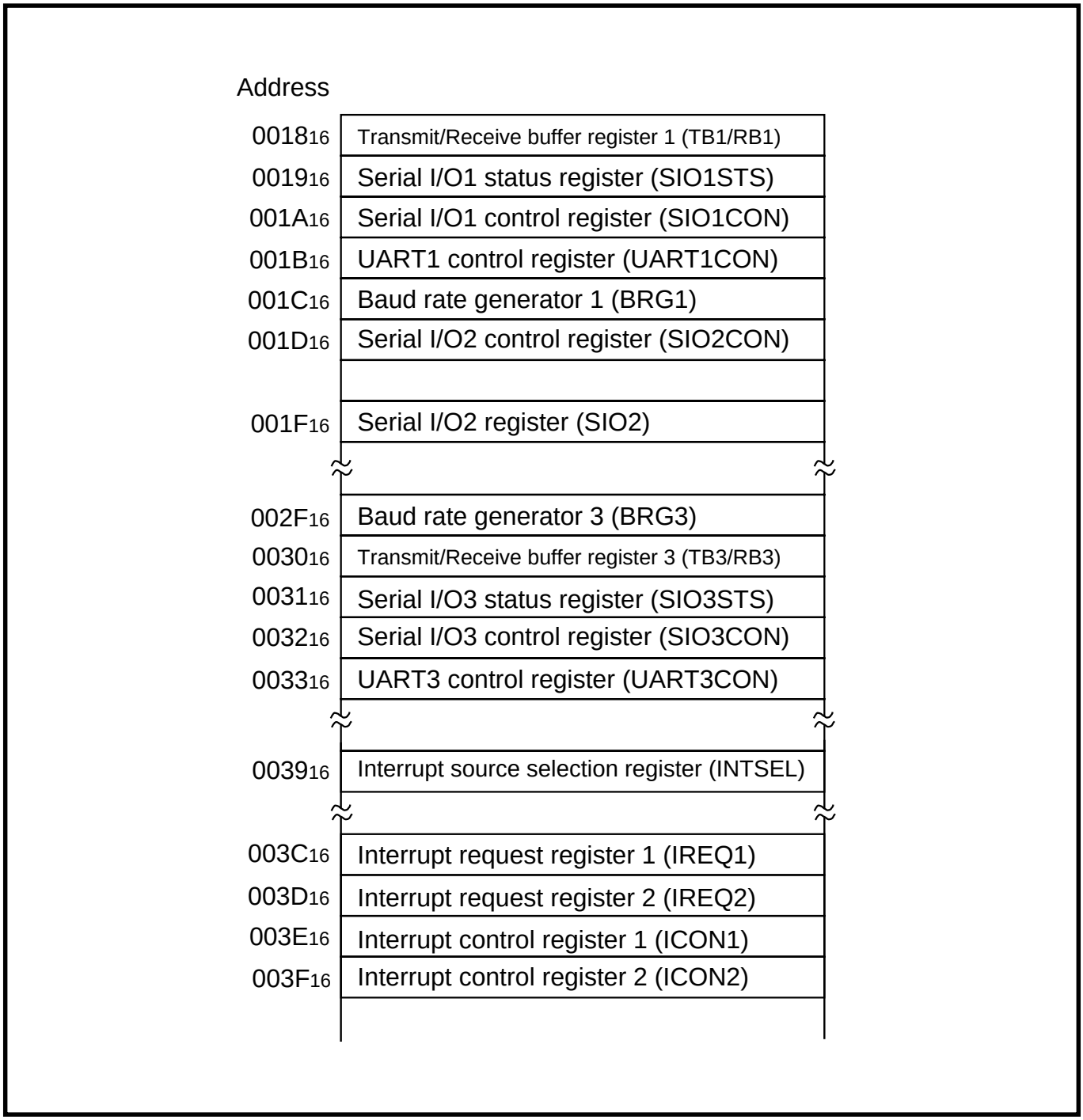
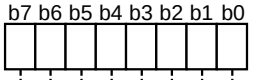


Fig. 2.4.1 Memory map of registers relevant to Serial I/O

2.4.2 Relevant registers

Transmit/Receive buffer register 1, Transmit/Receive buffer register 3



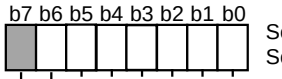
Transmit/Receive buffer register 1 (TB1/RB1: address 0018_{16})
Transmit/Receive buffer register 3 (TB3/RB3: address 0030_{16})

b	Functions	At reset	R	W
0	The transmission data is written to or the receive data is read out from this buffer register. • At write: A data is written to the transmit buffer register. • At read: The contents of the receive buffer register are read out.	Undefined	O	O
1		Undefined	O	O
2		Undefined	O	O
3		Undefined	O	O
4		Undefined	O	O
5		Undefined	O	O
6		Undefined	O	O
7		Undefined	O	O

Note: The contents of transmit buffer register cannot be read out.
The data cannot be written to the receive buffer register.

Fig. 2.4.2 Structure of Transmit/Receive buffer register 1 and Transmit/Receive buffer register 3

Serial I/O1 status register, Serial I/O3 status register



Serial I/O1 status register (SIO1STS: address 0019_{16})
Serial I/O3 status register (SIO3STS: address 0031_{16})

b	Name	Functions	At reset	R	W
0	Transmit buffer empty flag (TBE)	0: Buffer full 1: Buffer empty	0	O	X
1	Receive buffer full flag (RBF)	0: Buffer empty 1: Buffer full	0	O	X
2	Transmit shift register shift completion flag (TSC)	0: Transmit shift in progress 1: Transmit shift completed	0	O	X
3	Overrun error flag (OE)	0: No error 1: Overrun error	0	O	X
4	Parity error flag (PE)	0: No error 1: Parity error	0	O	X
5	Framing error flag (FE)	0: No error 1: Framing error	0	O	X
6	Summing error flag (SE)	0: (OE) U (PE) U (FE) = 0 1: (OE) U (PE) U (FE) = 1	0	O	X
7	Nothing is arranged for this bit. This bit is a write disabled bit. When this bit is read out, the contents are “1”.		1	O	X

Fig. 2.4.3 Structure of Serial I/O1 status register and Serial I/O3 status register

Serial I/O1 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O1 control register
(SIO1CON: address 001A16)

b	Name	Functions	At reset	R	W
0	BRG count source selection bit (CSS)	0: f(XIN) 1: f(XIN)/4	0	○	○
1	Serial I/O1 synchronous clock selection bit (SCS)	When clock synchronous serial I/O is selected, 0: BRG output divided by 4 1: External clock input When UART is selected, 0: BRG output divided by 16 1: External clock input divided by16	0	○	○
2	$\overline{SRDY1}$ output enable bit (SRDY)	0: I/O port (P47) 1: $\overline{SRDY1}$ output pin	0	○	○
3	Transmit interrupt source selection bit (TIC)	0: Transmit buffer empty 1: Transmit shift operation completion	0	○	○
4	Transmit enable bit (TE)	0: Transmit disabled 1: Transmit enabled	0	○	○
5	Receive enable bit (RE)	0: Receive disabled 1: Receive enabled	0	○	○
6	Serial I/O1 mode selection bit (SIOM)	0: UART 1: Clock synchronous serial I/O	0	○	○
7	Serial I/O1 enable bit (SIOE)	0: Serial I/O1 disabled (P44 to P47: normal I/O pins) 1: Serial I/O1 enabled (P44 to P47: Serial I/O pins)	0	○	○

Fig. 2.4.4 Structure of Serial I/O1 control register

Serial I/O3 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O3 control register
(SIO3CON: address 0032_{16})

b	Name	Functions	At reset	R	W
0	BRG count source selection bit (CSS)	0: f(X_{IN}) 1: f(X_{IN})/4	0	○	○
1	Serial I/O3 synchronous clock selection bit (SCS)	When clock synchronous serial I/O is selected, 0: BRG output divided by 4 1: External clock input When UART is selected, 0: BRG output divided by 16 1: External clock input divided by16	0	○	○
2	$\overline{S_{RDY3}}$ output enable bit (SRDY)	0: I/O port ($P3_7$) 1: $\overline{S_{RDY3}}$ output pin	0	○	○
3	Transmit interrupt source selection bit (TIC)	0: Transmit buffer empty 1: Transmit shift operation completion	0	○	○
4	Transmit enable bit (TE)	0: Transmit disabled 1: Transmit enabled	0	○	○
5	Receive enable bit (RE)	0: Receive disabled 1: Receive enabled	0	○	○
6	Serial I/O3 mode selection bit (SIOM)	0: UART 1: Clock synchronous serial I/O	0	○	○
7	Serial I/O3 enable bit (SIOE)	0: Serial I/O3 disabled ($P3_4$ to $P3_7$: normal I/O pins) 1: Serial I/O3 enabled ($P3_4$ to $P3_7$: Serial I/O pins)	0	○	○

Fig. 2.4.5 Structure of Serial I/O3 control register

UART1 control register

b7 b6 b5 b4 b3 b2 b1 b0

UART1 control register
(UART1CON: address 001B16)

b	Name	Functions	At reset	R	W
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	○	○
1	Parity enable bit (PARE)	0: Parity checking disabled 1: Parity checking enabled	0	○	○
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	○	○
3	Stop bit length selection bit (STPS)	0: 1 stop bit 1: 2 stop bits	0	○	○
4	P45/TxD1 P-channel output disable bit (POFF)	0: CMOS output (in output mode) 1: N-channel open-drain output (in output mode)	0	○	○
5	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “1”.		1	○	×
6			1	○	×
7			1	○	×

Fig. 2.4.6 Structure of UART1 control register

UART3 control register

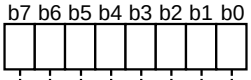
b7 b6 b5 b4 b3 b2 b1 b0

UART3 control register
(UART3CON: address 003316)

b	Name	Functions	At reset	R	W
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	○	○
1	Parity enable bit (PARE)	0: Parity checking disabled 1: Parity checking enabled	0	○	○
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	○	○
3	Stop bit length selection bit (STPS)	0: 1 stop bit 1: 2 stop bits	0	○	○
4	P35/TxD3 P-channel output disable bit (POFF)	0: CMOS output (in output mode) 1: N-channel open-drain output (in output mode)	0	○	○
5	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “1”.		1	○	×
6			1	○	×
7			1	○	×

Fig. 2.4.7 Structure of UART3 control register

Baud rate generator i (i = 1, 3)



Baud rate generator i
(BRGi (i=1, 3): address 001C16, 002F16)

b	Functions	At reset	R	W
0	Set a count value of baud rate generator.	Undefined	○	○
1		Undefined	○	○
2		Undefined	○	○
3		Undefined	○	○
4		Undefined	○	○
5		Undefined	○	○
6		Undefined	○	○
7		Undefined	○	○

Note: Write to this register while transmit/receive operation is stopped.

Fig. 2.4.8 Structure of Baud rate generator 1 and Baud rate generator 3

Serial I/O2 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O2 control register
(SIO2CON: address 001D16)

b	Name	Functions	At reset	R	W
0	Internal synchronous clock selection bits	b2b1b0 0 0 0: f(XIN)/8 0 0 1: f(XIN)/16 0 1 0: f(XIN)/32 0 1 1: f(XIN)/64 1 1 0: f(XIN)/128 1 1 1: f(XIN)/256	0	○	○
1			0	○	○
2			0	○	○
3	Serial I/O2 port selection bit	0: I/O port (P51, P52) 1: SOUT2, SCLK2 signal output	0	○	○
4	$\overline{S_{RDY2}}$ output enable bit	0: I/O port (P53) 1: $\overline{S_{RDY2}}$ signal output	0	○	○
5	Transfer direction selection bit	0: LSB first 1: MSB first	0	○	○
6	Serial I/O2 synchronous clock selection bit	0: External clock 1: Internal clock	0	○	○
7	P51/SOUT2 P-channel output disable bit	0: CMOS output (in output mode) 1: N-channel open-drain output (in output mode)	0	○	○

Fig. 2.4.9 Structure of Serial I/O2 control register

Serial I/O2 register

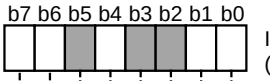
b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O2 register
(SIO2: address 001F16)

b	Name	Functions	At reset	R	W
0	This register becomes shift register. At transmit: Set transmit data to this register. At receive: Received data is stored to this register.		Undefined	○	○
1			Undefined	○	○
2			Undefined	○	○
3			Undefined	○	○
4			Undefined	○	○
5			Undefined	○	○
6			Undefined	○	○
7			Undefined	○	○

Fig. 2.4.10 Structure of Serial I/O2 register

Interrupt source selection register



Interrupt source selection register
(INTSEL: address 0039_{16})

b	Name	Functions	At reset	R	W
0	INT_0/Timer Z interrupt source selection bit (*1)	0: INT_0 interrupt 1: Timer Z interrupt	0	○	○
1	Serial I/O2/Timer Z interrupt source selection bit (*1)	0: Serial I/O2 interrupt 1: Timer Z interrupt	0	○	○
2	Nothing is arranged for these bits. Do not write “1” to these bits. When these bits are read out, the contents are “0”.		0	○	○
3			0	○	○
4	INT_4/$CNTR_2$ interrupt source selection bit	0: INT_4 interrupt 1: $CNTR_2$ interrupt	0	○	○
5	Nothing is arranged for this bit. Do not write “1” to this bit. When this bit is read out, the contents are “0”.		0	○	○
6	$CNTR_1$/Serial I/O3 receive interrupt source selection bit	0: $CNTR_1$ interrupt 1: Serial I/O3 receive interrupt	0	○	○
7	AD converter/Serial I/O3 transmit interrupt source selection bit	0: A-D converter interrupt 1: Serial I/O3 transmit interrupt	0	○	○

*1: Do not write “1” to these bits simultaneously.

Fig. 2.4.11 Structure of Interrupt source selection register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1
(IREQ1 : address 003C16)

b	Name	Functions	At reset	R	W
0	INT0/Timer Z interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	INT1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	Serial I/O1 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	Serial I/O1 transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	Timer X interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	Timer Y interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Timer 2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻

✻: "0" can be set by software, but "1" cannot be set.

Fig. 2.4.12 Structure of Interrupt request register 1

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2
(IREQ2 : address 003D16)

b	Name	Functions	At reset	R	W
0	CNTR0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	CNTR1/Serial I/O3 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	Serial I/O2/Timer Z interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	INT2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	INT3 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	INT4/CNTR2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	AD converter/Serial I/O3 transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	×

✻: "0" can be set by software, but "1" cannot be set.

Fig. 2.4.13 Structure of Interrupt request register 2

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1
(ICON1 : address 003E16)

b	Name	Functions	At reset	R	W
0	INT0/Timer Z interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Serial I/O1 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Serial I/O1 transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Timer X interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Timer Y interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.4.14 Structure of Interrupt control register 1

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0
0

Interrupt control register 2
(ICON2 : address 003F16)

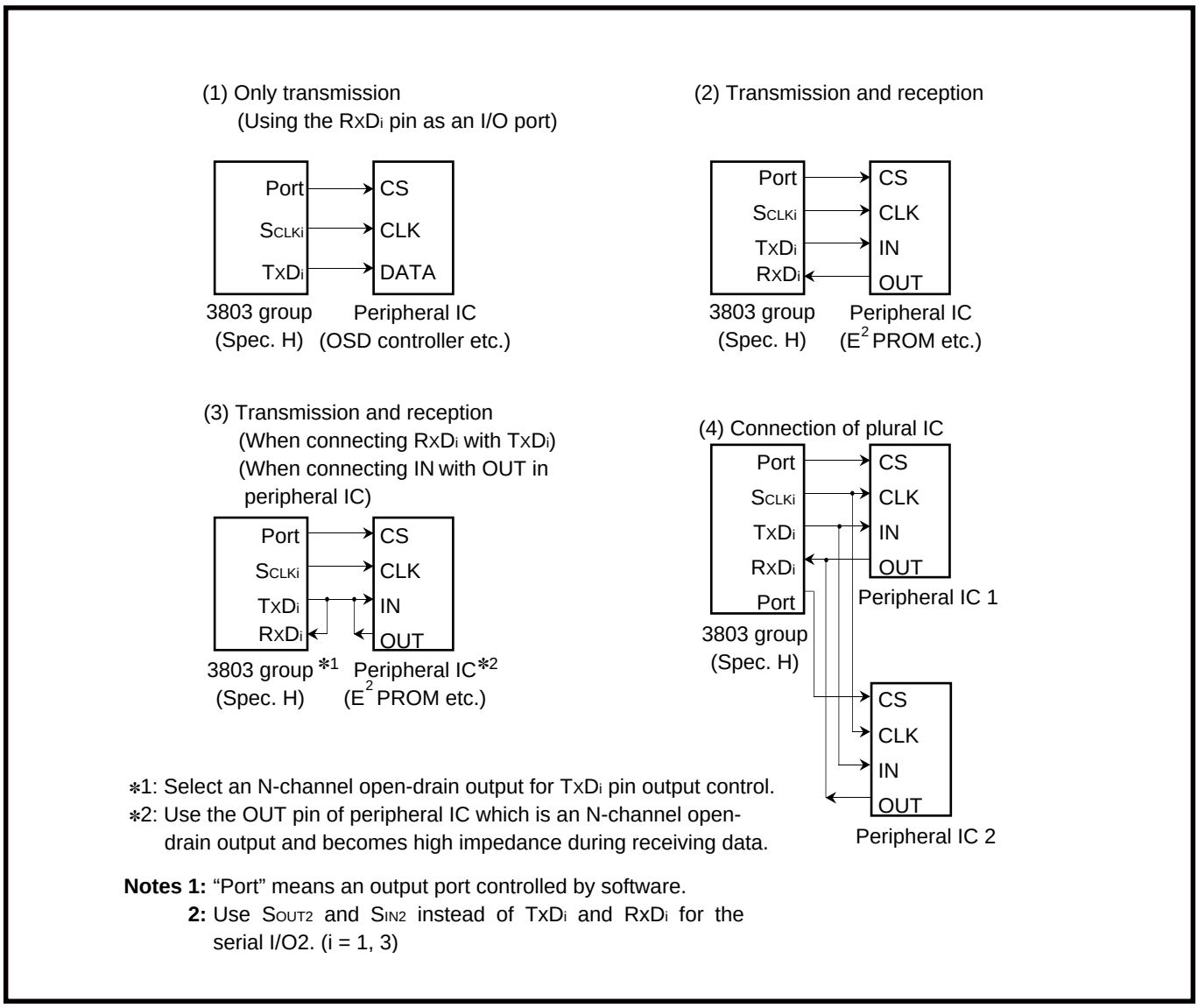
b	Name	Functions	At reset	R	W
0	CNTR0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	CNTR1/ Serial I/O3 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Serial I/O2/ Timer Z interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	INT2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT3 interrupt enable bit	0 : Interrupt disabled	0	○	○
5	INT4/CNTR2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	AD converter/Serial I/O3 transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to “0”.		0	○	○

Fig. 2.4.15 Structure of Interrupt control register 2

2.4.3 Serial I/O connection examples

(1) Control of peripheral IC equipped with CS pin

Figure 2.4.16 shows connection examples of a peripheral IC equipped with the CS pin. There are connection examples using a clock synchronous serial I/O mode.



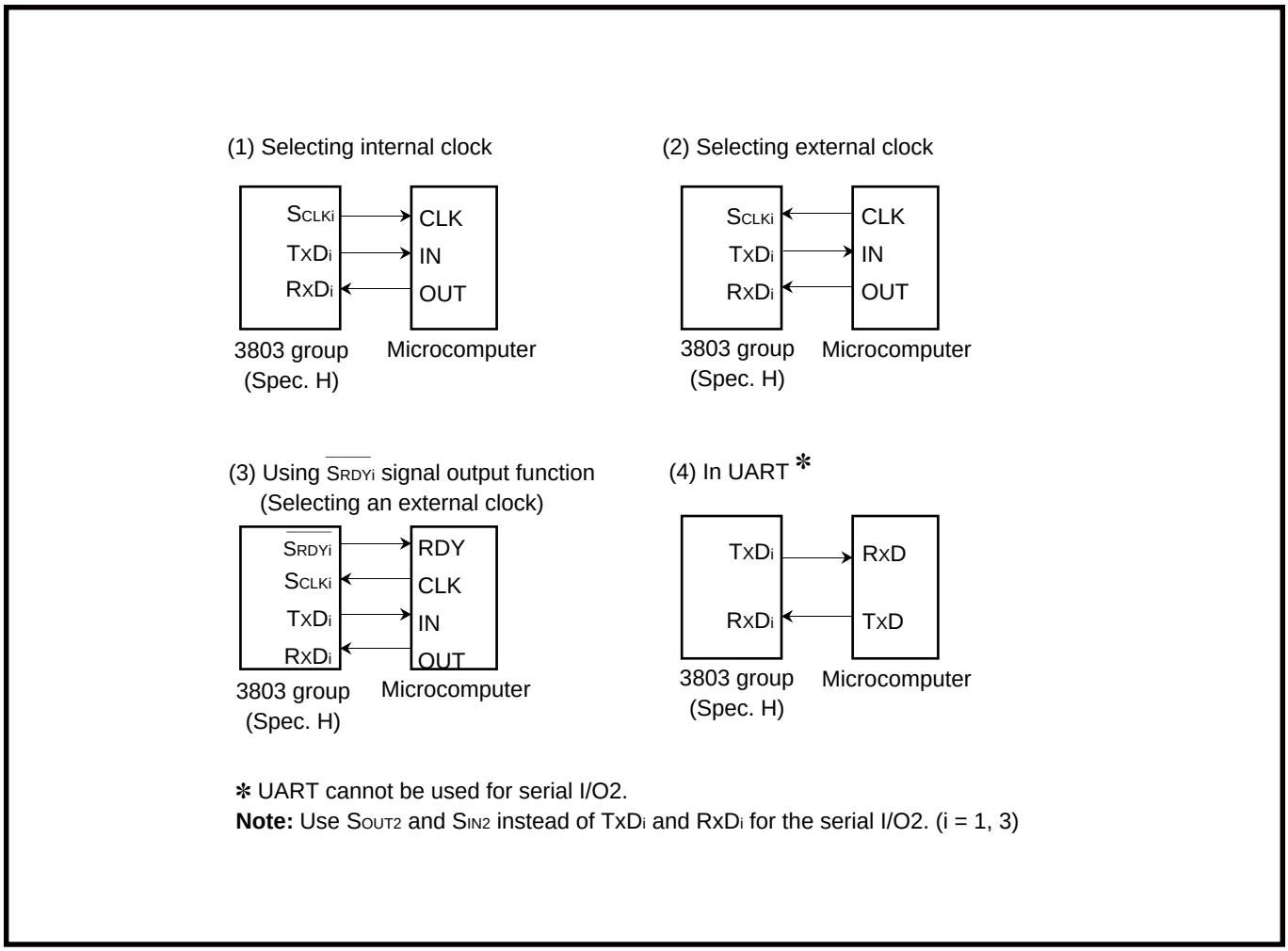
∗1: Select an N-channel open-drain output for TxDi pin output control.
∗2: Use the OUT pin of peripheral IC which is an N-channel open-drain output and becomes high impedance during receiving data.

Notes 1: "Port" means an output port controlled by software.
2: Use SOUT2 and SIN2 instead of TxDi and RxDi for the serial I/O2. (i = 1, 3)

Fig. 2.4.16 Serial I/O connection examples (1)

(2) Connection with microcomputer

Figure 2.4.17 shows connection examples with another microcomputer.



* UART cannot be used for serial I/O2.

Note: Use S_{OUT2} and S_{IN2} instead of TxD_i and RxD_i for the serial I/O2. (i = 1, 3)

Fig. 2.4.17 Serial I/O connection examples (2)

2.4.4 Setting of serial I/O transfer data format

A clock synchronous or clock asynchronous (UART) can be selected as a data format of serial I/O1 and serial I/O3.
Serial I/O2 operates in a clock synchronous.
Figure 2.4.18 shows the serial I/O transfer data format.

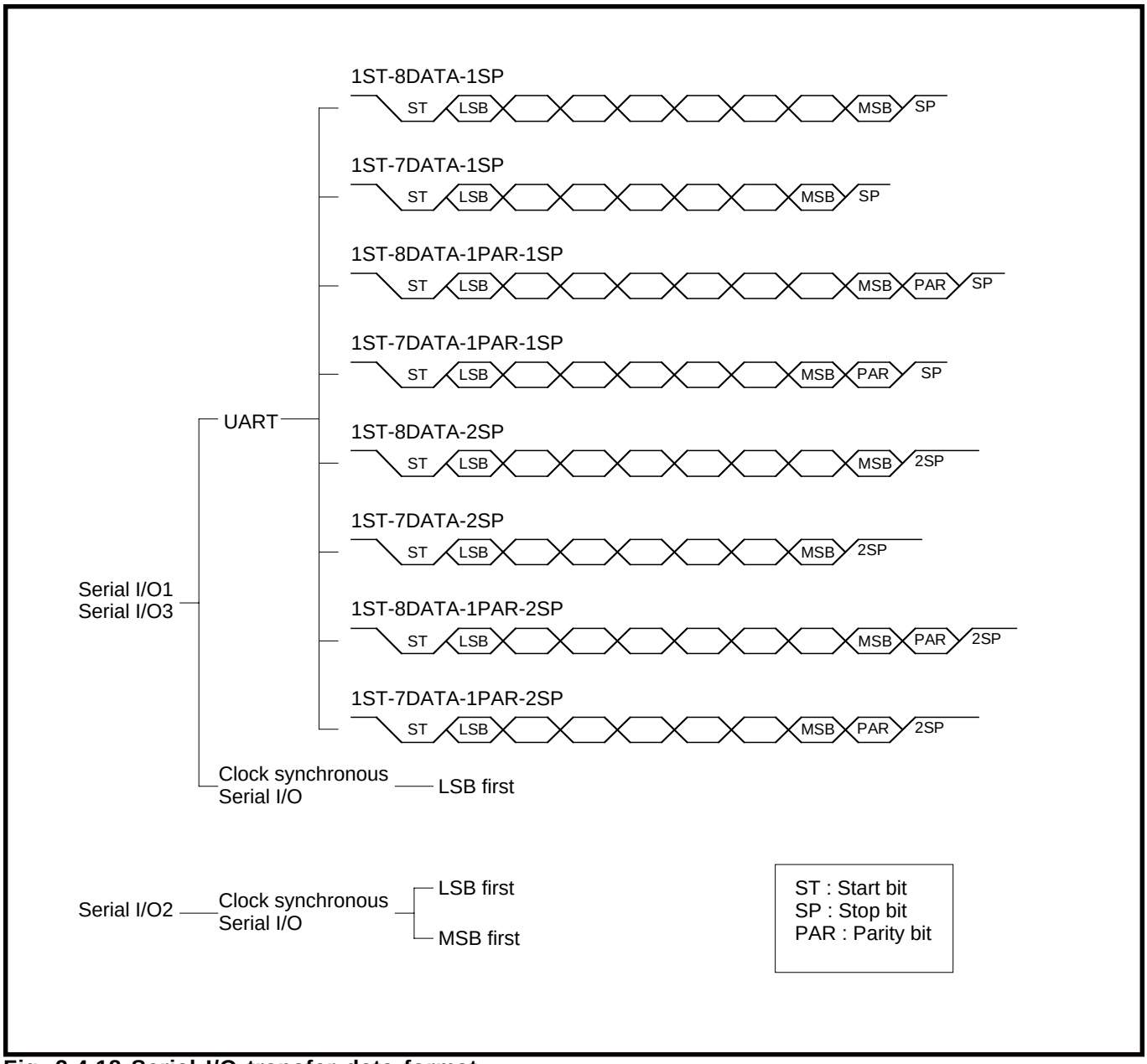


Fig. 2.4.18 Serial I/O transfer data format

2.4.5 Serial I/O1, serial I/O3 operation: stop and initialize

Serial I/O1 and serial I/O3 perform the same operation. In the following explanations when names of serial I/O1 and serial I/O3 are different, serial I/O1s' are showed first and then serial I/O3s' in the marked ( ).

(1) Clock synchronous serial I/O mode

■Stop/initialize transmit operation when only transmitting

When using an internal clock, set the transmit enable bit and serial I/O1 enable bit (serial I/O3 enable bit) to “0”.
When using an external clock, set the transmit enable bit to “0”.

By setting the transmit enable bit to “0”, the transmit operations listed below will be stopped or initialized. However, when using an internal clock, the clock is output in 8 pulses, even if the transmit enable bit is set to “0” during transmit operations.

- Stop supply of shift clock to transmit shift register
- Initialize clock control circuit for transmit
- Transmit buffer empty flag = “0”
- Transmit shift register shift complete flag = “0”
- $P4_5/TxD_1$ pin: input/output port $P4_5$ ($P3_5/TxD_3$ pin: input/output port $P3_5$)

By setting the serial I/O1 enable bit (serial I/O3 enable bit) to “0”, pins $P4_4/RxD_1$, $P4_5/TxD_1$, $P4_6/S_{CLK1}$, and $P4_7/\overline{S_{RDY1}}$ ($P3_4/RxD_3$, $P3_5/TxD_3$, $P3_6/S_{CLK3}$, $P3_7/\overline{S_{RDY3}}$ pins) all become I/O ports. As a result, the internal clock cannot be output externally.

■Stop/initialize receive operation when only receiving

When using an internal clock, set the receive enable bit and serial I/O1 enable bit (serial I/O3 enable bit) to “0”.
When using an external clock, set the receive enable bit or serial I/O1 enable bit (serial I/O3 enable bit) to “0”.

By setting the receive enable bit to “0”, the receive operations listed below will be stopped or initialized. However, when using an internal clock, the clock is output in 8 pulses, even if the receive enable bit is set to “0” during receive operations.

- Stop supply of shift clock to receive shift register
- Initialize clock control circuit for receive
- Error flags (over-run, parity, framing, and summing error flags) = “0”
- Receive buffer full flag = “0”
- $P4_4/RxD_1$ pin: input/output port $P4_4$ ($P3_4/RxD_3$ pin: input/output port $P3_4$)

By setting the serial I/O1 enable bit (serial I/O3 enable bit) to “0”, the receive operations listed below will be stopped or initialized. As a result, the internal clock cannot be output externally.

- Stop supply of shift clock to receive shift register
- Initialize clock control circuit for receive
- Error flags (over-run, parity, framing, and summing error flags) = “0”
- Receive buffer full flag = “0”
- $P4_4/RxD_1$, $P4_5/TxD_1$, $P4_6/S_{CLK1}$, $P4_7/\overline{S_{RDY1}}$ pins: I/O ports $P4_4$, $P4_5$, $P4_6$, $P4_7$ ($P3_4/RxD_3$, $P3_5/TxD_3$, $P3_6/S_{CLK3}$, $P3_7/\overline{S_{RDY3}}$ pins: I/O ports $P3_4$, $P3_5$, $P3_6$, $P3_7$)

■Stop/initialize receive/transmit operation when both receiving and transmitting

Set the transmit enable bit and receive enable bit to “0” simultaneously.
When using an internal clock, also set the serial I/O1 enable bit (serial I/O3 enable bit) to “0”.

(2) UART Mode

■Stop/initialize transmit operation

Set the transmit enable bit to “0”.

■Stop/initialize receive operation

Set the receive enable bit to “0”.

2.4.6 Serial I/O pin function and selection method

(1) Serial I/O1, serial I/O3

Table 2.4.1 shows the pin function in the clock synchronous serial I/O mode, Table 2.4.2 shows the pin function in the UART mode.

Table 2.4.1 Pin function in clock synchronous serial I/O mode

Pin name (Serial I/O1)	Pin name (Serial I/O3)	Function	Serial I/O1 control register (address 1A16) Serial I/O3 control register (address 3216)								Corresponding direction register
			b7 (Note 1)	b6	b5	b4	b3	b2	b1	b0	
			SIOE	SIOM	RE	TE	TIC	SRDY	SCS	CSS	
P44/RxD1	P34/RxD3	RxD1, RxD3	1	1	1	1	×	×	×	×	×
		P44, P34	1	1	0	×	×	×	×	×	0/1
P45/TxD1	P35/TxD3	TxD1, TxD3	1	1	×	1	×	×	×	×	×
		P45, P35	1	1	×	0	×	×	×	×	0/1
P46/SCLK1	P36/SCLK3	SCLK1 (External clock input)	1	1	×	1	×	×	1	×	×
		SCLK1 (Internal clock output)	1	1	×	1	×	×	0	×	×
P47/SRDY1 (Note 2) /CNTR2	P37/SRDY3	SRDY1, SRDY3	1	1	1	1	×	1	×	×	×
		P47, P37	1	1	×	×	×	0	×	×	0/1

Note 1: When SIOE is set to "0", all pins become I/O ports regardless of set value of b6–b0.
Note 2: In the pulse output mode, the programmable waveform generating mode, or the programmable one-shot generating mode of the timer Z, this pin functions as the timer Z function output pin regardless of b7-b0 setting.
×: This is not used for the pin's function setting.

Table 2.4.2 Pin function in UART mode

Pin name (Serial I/O1)	Pin name (Serial I/O3)	Function	Serial I/O1 control register (address 1A16)								Corresponding direction register
			b7 (Note 1)	b6	b5	b4	b3	b2	b1	b0	
			SIOE	SIOM	RE	TE	TIC	SRDY	SCS	CSS	
P44/RxD1	P34/RxD3	RxD	1	0	1	×	×	×	×	×	×
		P44	1	0	0	×	×	×	×	×	0/1
P45/TxD1	P35/TxD3	TxD	1	0	×	1	×	×	×	×	×
		P45	1	0	×	0	×	×	×	×	0/1
P46/SCLK1	P36/SCLK3	SCLK1 (External clock input)	1	0	×	×	×	×	1	×	×
		P46	1	0	×	×	×	×	0	×	0/1
P47/SRDY1 (Note 2) /CNTR2	P37/SRDY3	P47	1	0	×	×	×	×	×	×	0/1

Note 1: When SIOE is set to "0", all pins become I/O ports regardless of set value of b6–b0.
Note 2: In the pulse output mode, the programmable waveform generating mode, or the programmable one-shot generating mode of the timer Z, this pin functions as the timer Z function output pin regardless of b7-b0 setting.
×: This is not used for the pin's function setting.

(2) Serial I/O2

Table 2.4.3 shows the pin function in the clock synchronous serial I/O mode.

Table 2.4.3 Pin function in clock synchronous serial I/O mode

Pin name	Function		Serial I/O2 control register (address 1D16)								Corresponding direction register
			b7	b6	b5	b4	b3	b2	b1	b0	
P50/SIN2	SIN2 (Note 1)		×	×	×	×	1	×	×	×	0
	P50		×	×	×	×	×	×	×	×	0/1
P51/SOUT2	SOUT2	CMOS output	0	×	×	×	1	×	×	×	×
		N-channel open-drain output	1	×	×	×	1	×	×	×	×
	P51		(Note 3)	×	×	×	0	×	×	×	0/1
P52/SCLK2	SCLK2 (External clock input) (Note 2)		×	0	×	×	1	×	×	×	×
	SCLK2 (Internal clock output)		×	1	×	×	1	×	×	×	×
	P52		×	×	×	×	0	×	×	×	0/1
P53/SRDY2	SRDY2		×	×	×	1	×	×	×	×	×
	P53		×	×	×	0	×	×	×	×	0/1

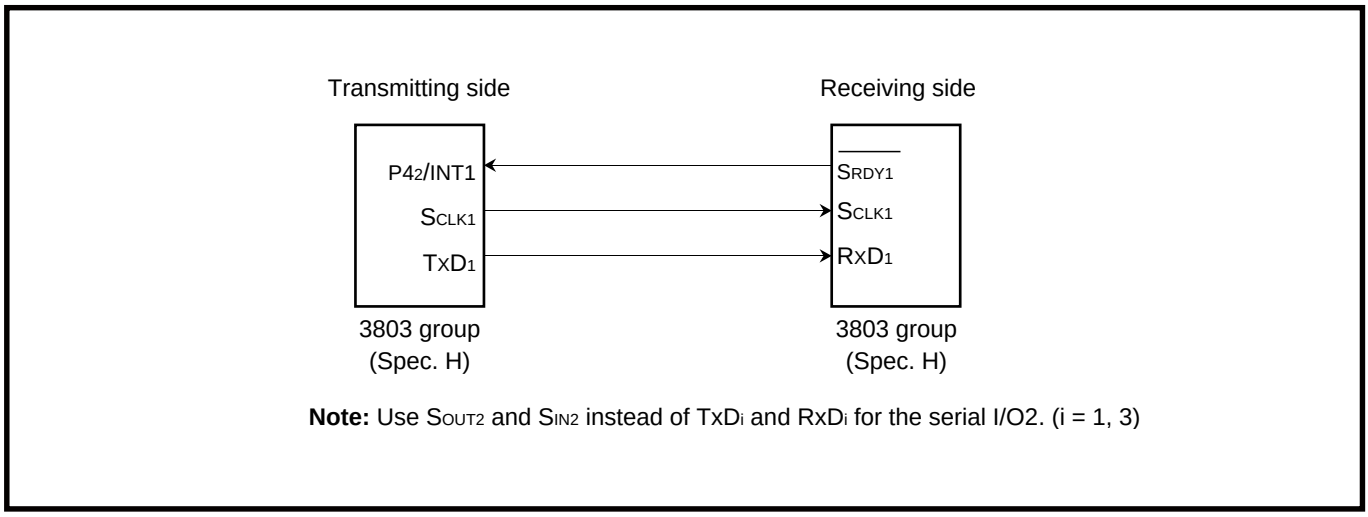
Notes 1: Although this pin functions as SIN2 when b3 is set to "0", set "1" to b3.
Notes 2: Although this pin functions as SCLK2 when b3 and the corresponding direction register are set to "0", set "1" to b3.
Notes 3: When the corresponding direction register bit is "1", the b7 setting is valid.
×: This is not used for the pin's function setting.

2.4.7 Serial I/O application examples

(1) Communication using clock synchronous serial I/O (transmit/receive)

Outline : 2-byte data is transmitted and received, using the clock synchronous serial I/O. The $\overline{SRDY1}$ signal is used for communication control.

Figure 2.4.19 shows a connection diagram, and Figure 2.4.20 shows a timing chart.
Figure 2.4.21 shows a registers setting relevant to the transmitting side, and Figure 2.4.22 shows registers setting relevant to the receiving side.



Note: Use S_{OUT2} and S_{IN2} instead of TxD_i and RxD_i for the serial I/O2. (i = 1, 3)

Fig. 2.4.19 Connection diagram

Specifications :
- Serial I/O is used (clock synchronous serial I/O is selected.)
- Synchronous clock frequency : 125 kHz (f(X_{IN}) = 4 MHz is divided by 32)
- $\overline{SRDY1}$ (receivable signal) is used.
- The receiving side outputs $\overline{SRDY1}$ signal at intervals of 2 ms (generated by timer), and 2-byte data is transferred from the transmitting side to the receiving side.

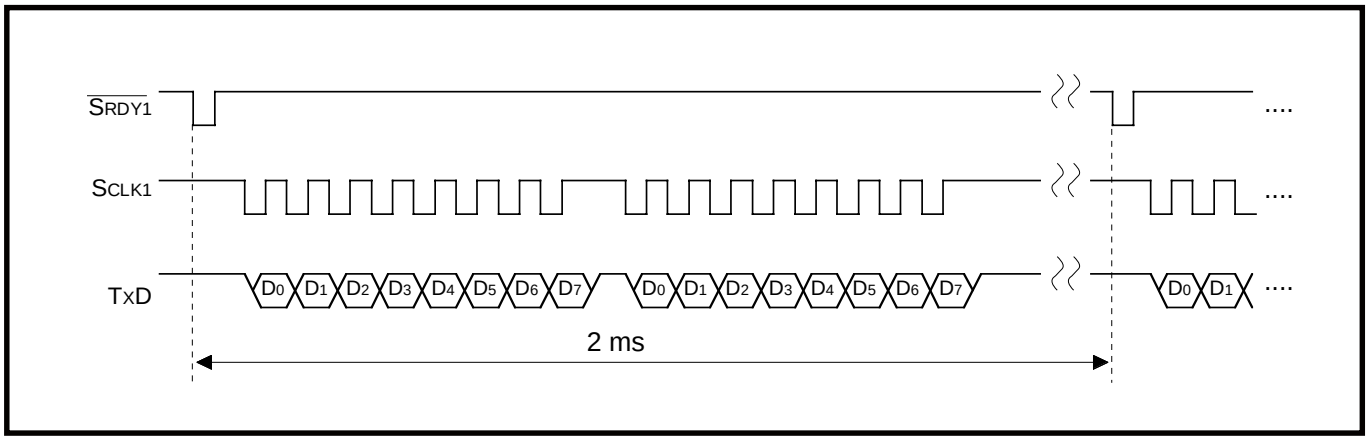


Fig. 2.4.20 Timing chart (using clock synchronous serial I/O)

Transmitting side

Port P4 direction register (Address : 0009_{16})

P4D

b7							b0
					0		

→ Port $P4_2/INT_1$: Input mode

Serial I/O1 status register (Address : 0019_{16})

SIO1STS

b7							b0

→ Transmit buffer empty flag
- Confirm that the data has been transferred from Transmit buffer register to Transmit shift register.
- When this flag is "1", it is possible to write the next transmission data in to Transmit buffer register.

→ Transmit shift register shift completion flag
Confirm completion of transmitting 1-byte data with this flag.
"1" : Transmit shift completed

Serial I/O1 control register (Address : $001A_{16}$)

SIO1CON

b7							b0
1	1	0	1			0	0

→ BRG count source : f(X_{IN})
→ Serial I/O1 synchronous clock : BRG/4
→ Transmit enabled
→ Receive disabled
→ Clock synchronous serial I/O
→ Serial I/O1 enabled

UART1 control register (Address : $001B_{16}$)

UART1CON

b7							b0
			0				

→ $P4_5/TxD_1$ pin : CMOS output

Baud rate generator 1 (Address : $001C_{16}$)

BRG1

b7							b0
8 – 1							

Set "division ratio – 1"

Interrupt edge selection register (Address : $003A_{16}$)

INTEDGE

b7							b0
						0	

→ INT_1 falling edge active

Fig. 2.4.21 Registers setting relevant to transmitting side

Receiving side

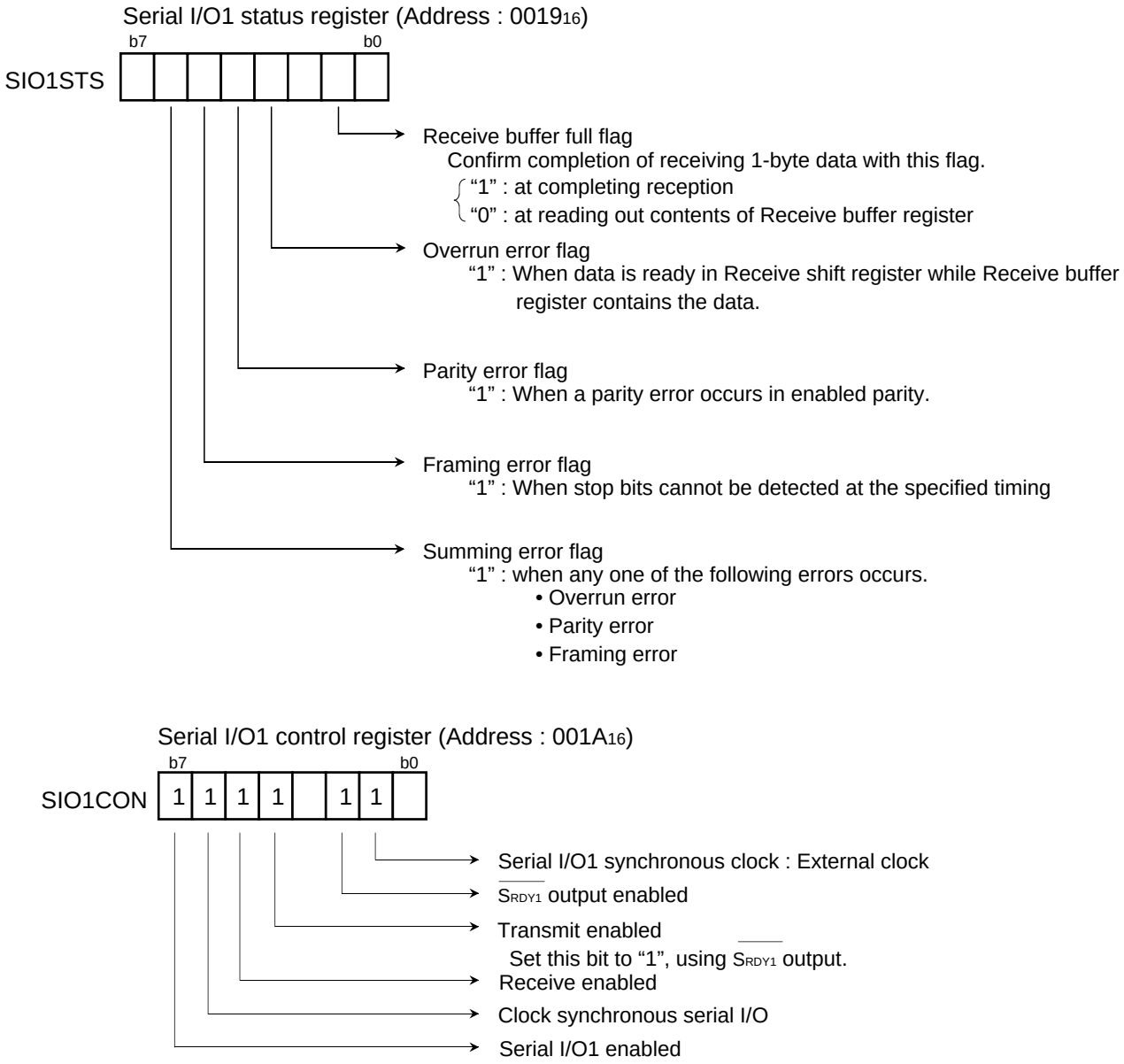


Fig. 2.4.22 Registers setting relevant to receiving side

Figure 2.4.23 shows a control procedure of the transmitting side, and Figure 2.4.24 shows a control procedure of the receiving side.

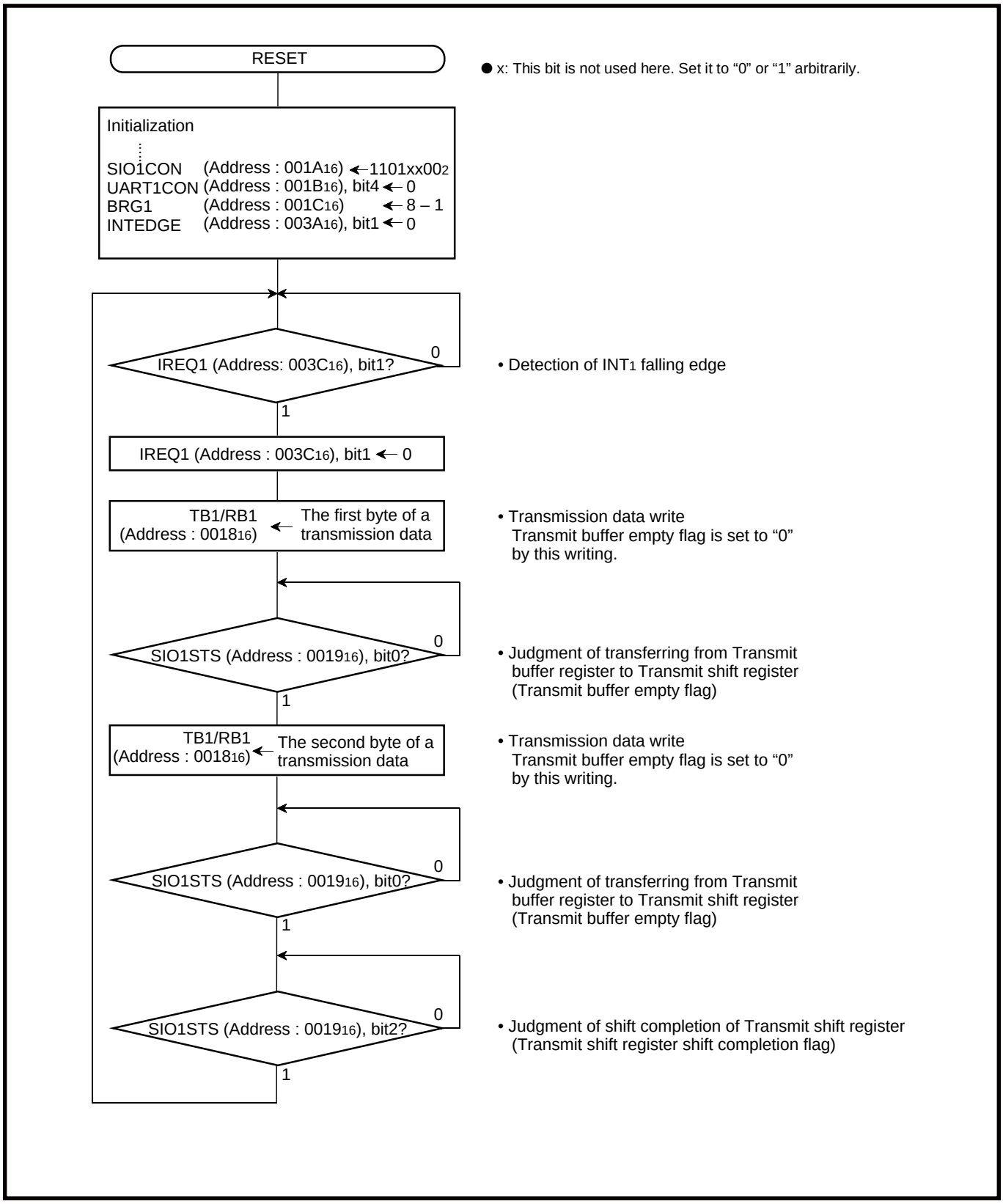


Fig. 2.4.23 Control procedure of transmitting side

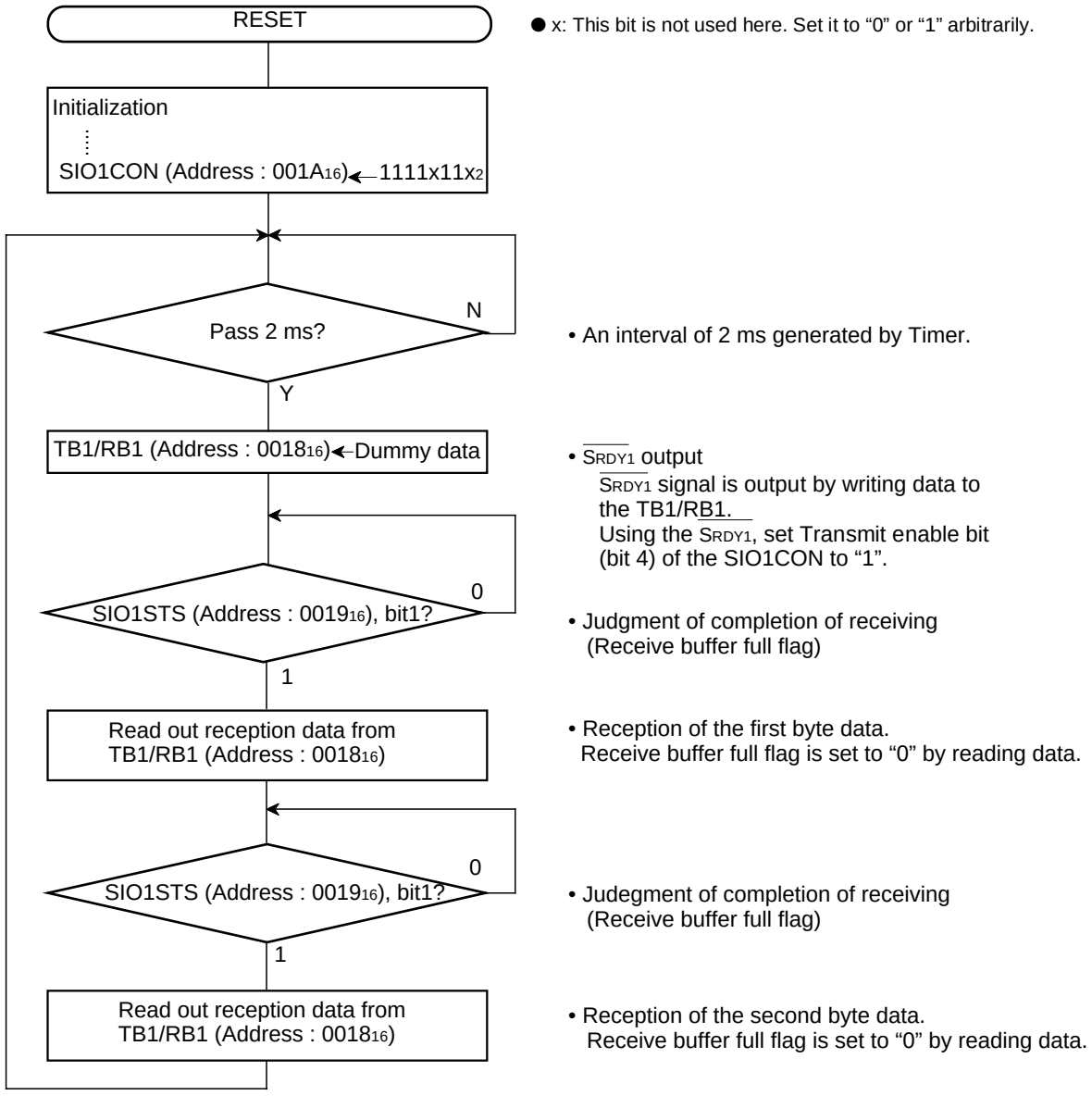
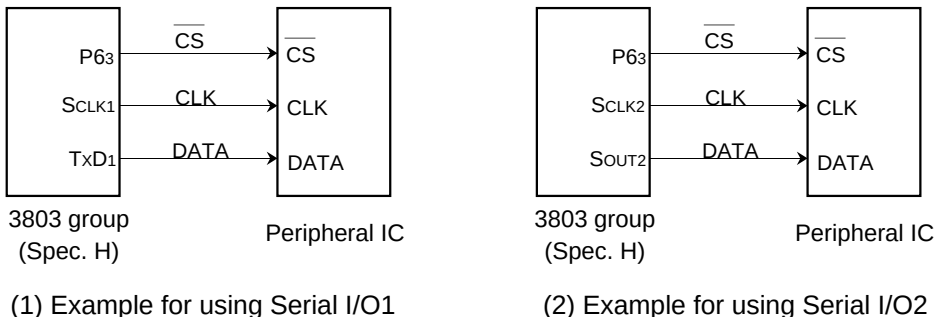


Fig. 2.4.24 Control procedure of receiving side

(2) Output of serial data (control of peripheral IC)

Outline : 4-byte data is transmitted and received, using the clock synchronous serial I/O. The $\overline{CS}$ signal is output to a peripheral IC through port $P6_3$.

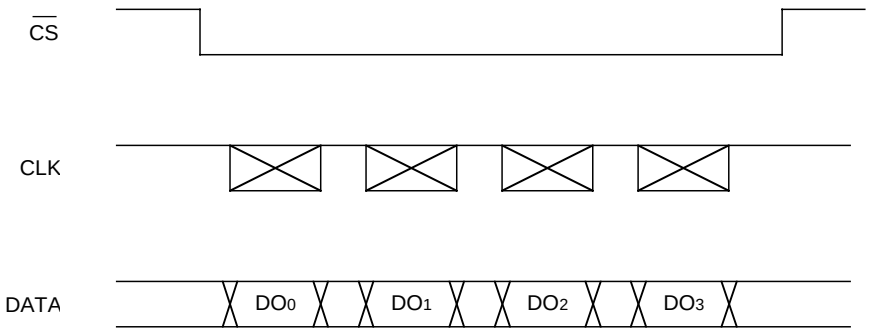
Figure 2.4.25 shows connection diagrams of example for using serial I/O1 and example for using serial I/O2 with the same specification, and Figure 2.4.26 shows a timing chart.



(1) Example for using Serial I/O1 (2) Example for using Serial I/O2

Fig. 2.4.25 Connection diagrams

Specifications :
- Serial I/O is used (clock synchronous serial I/O is selected.)
- Synchronous clock frequency : 125 kHz ($f(X_{IN})$ = 4 MHz is divided by 32)
- Transfer direction : LSB first
- The Serial I/O interrupt is not used.
- Port $P6_3$ is connected to the $\overline{CS}$ pin ("L" active) of the peripheral IC for transmission control; the output level of port $P6_3$ is controlled by software.



Note: When using serial I/O2, the S_{OUT2} pin becomes the high-impedance state after transfer is completed.

Fig. 2.4.26 Timing chart (serial I/O1)

Figure 2.4.27 shows registers setting relevant to serial I/O1, and Figure 2.4.28 shows a setting of serial I/O1 transmission data.

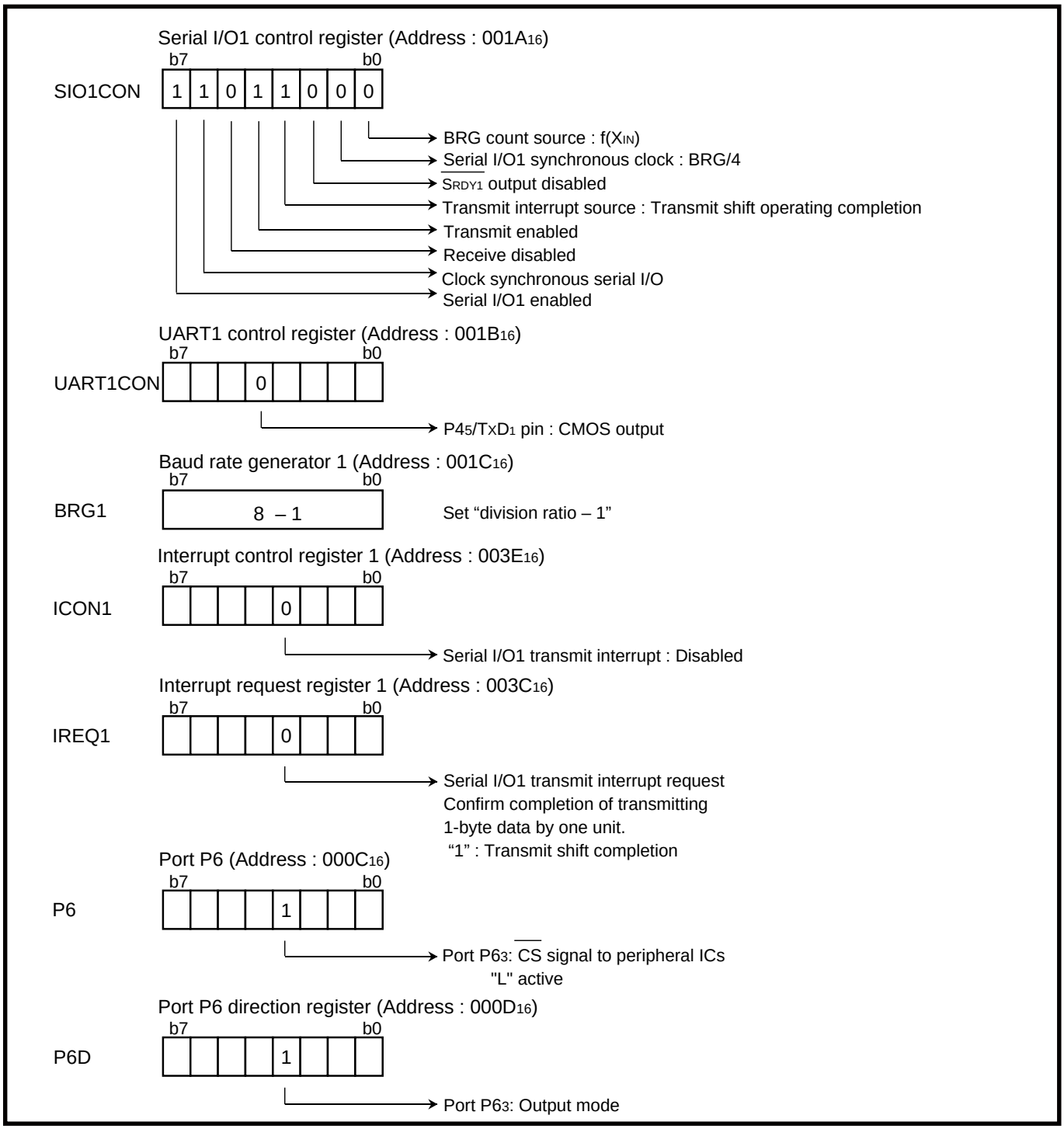


Fig. 2.4.27 Registers setting relevant to serial I/O1

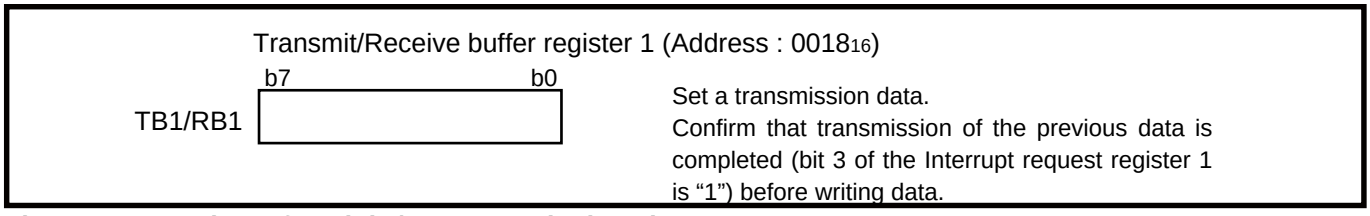


Fig. 2.4.28 Setting of serial I/O1 transmission data

When the registers are set as shown in Fig. 2.4.27, serial I/O1 can transmit 1-byte data by writing data to the transmit buffer register.
Thus, after setting the $\overline{CS}$ signal to "L", write the transmission data to the transmit buffer register by each 1 byte, and return the $\overline{CS}$ signal to "H" when the target number of bytes has been transmitted. Figure 2.4.29 shows a control procedure of serial I/O1.

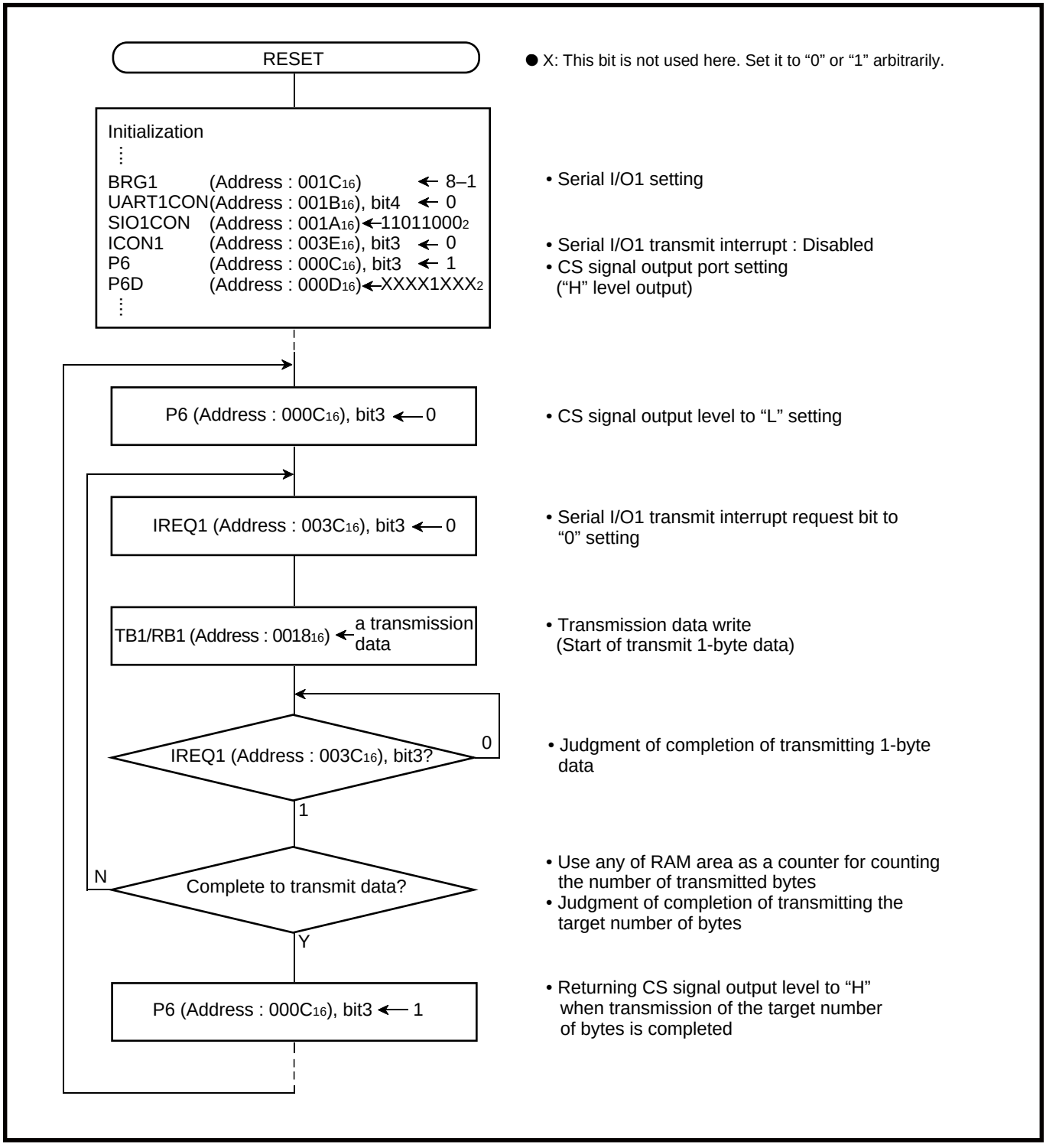


Fig. 2.4.29 Control procedure of serial I/O1

Figure 2.4.30 shows registers setting relevant to serial I/O2, and Figure 2.4.31 shows a setting of serial I/O2 transmission data.

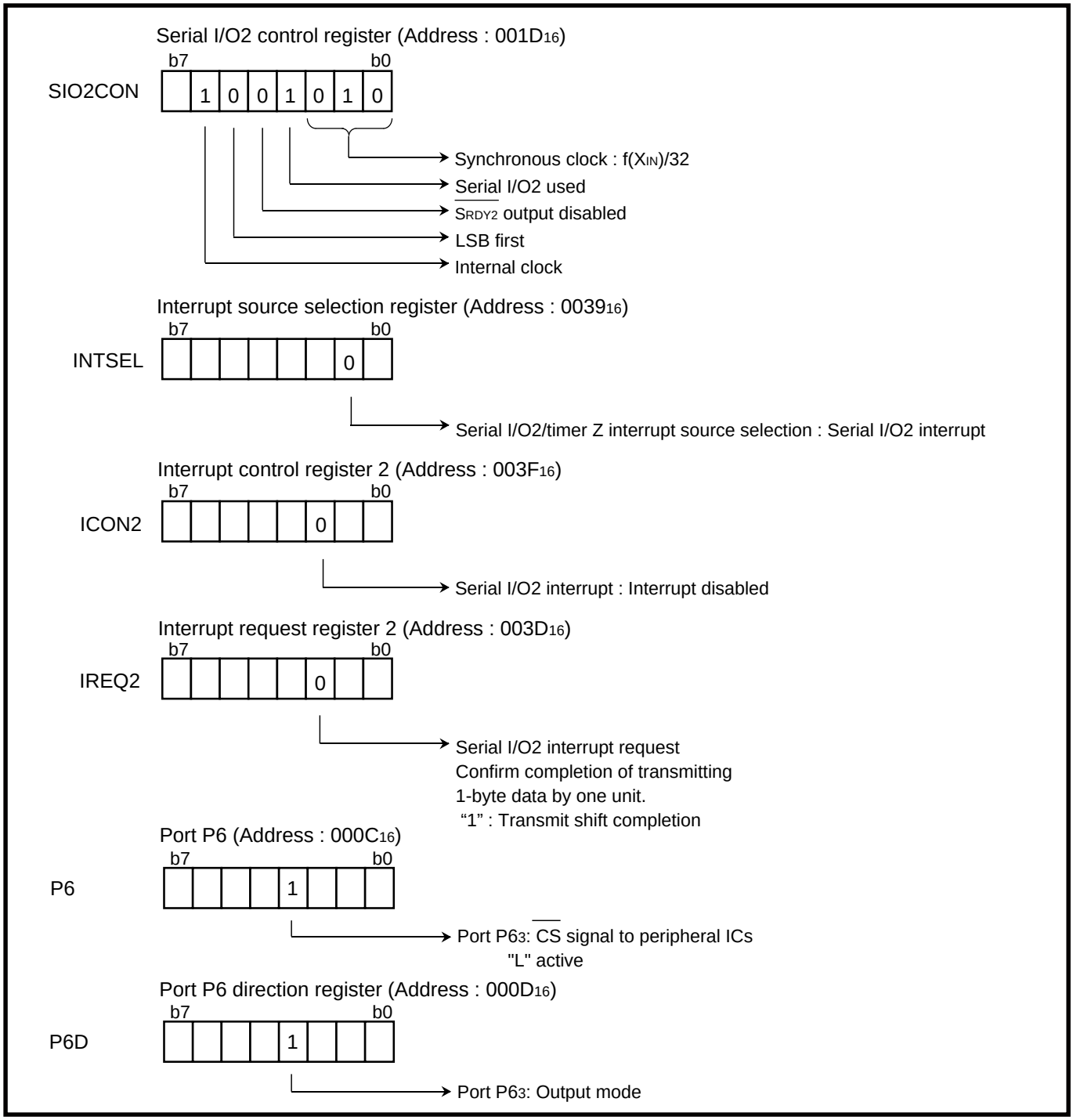


Fig. 2.4.30 Registers setting relevant to serial I/O2

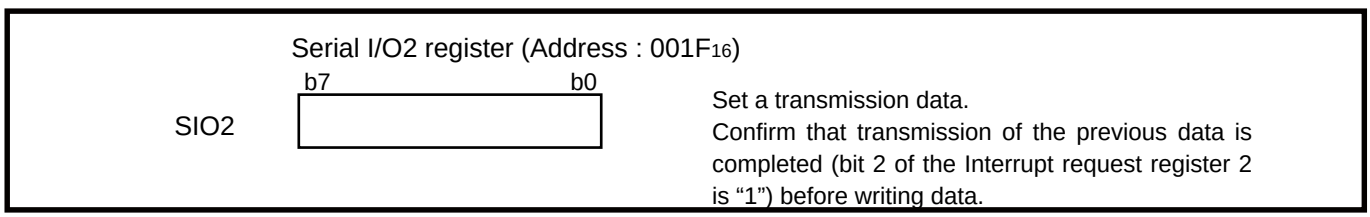


Fig. 2.4.31 Setting of serial I/O2 transmission data

When the registers are set as shown in Fig. 2.4.30, serial I/O2 can transmit 1-byte data by writing data to the serial I/O2 register.
Thus, after setting the CS signal to “L”, write the transmission data to the serial I/O2 register by each 1 byte, and return the CS signal to “H” when the target number of bytes has been transmitted.
Figure 2.4.32 shows a control procedure of serial I/O2.

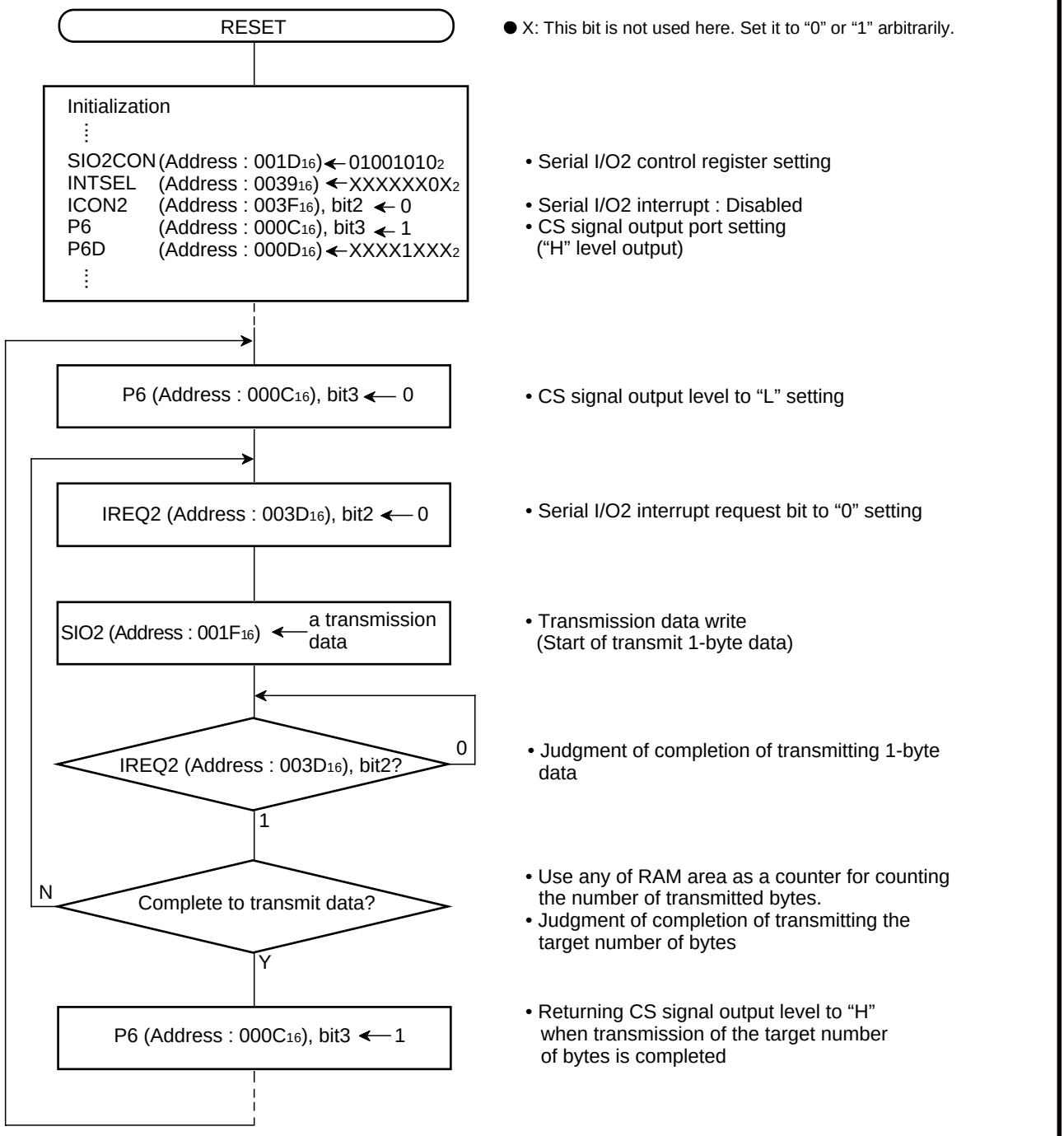


Fig. 2.4.32 Control procedure of serial I/O2

(3) Cyclic transmission or reception of block data (data of specified number of bytes) between two microcomputers

Outline : When the clock synchronous serial I/O is used for communication, synchronization of the clock and the data between the transmitting and receiving sides may be lost because of noise included in the synchronous clock. It is necessary to correct that constantly, using "heading adjustment".

This "heading adjustment" is carried out by using the interval between blocks in this example. This example is described for serial I/O1, but this example also can apply serial I/O3.

Figure 2.4.33 shows connection diagram.

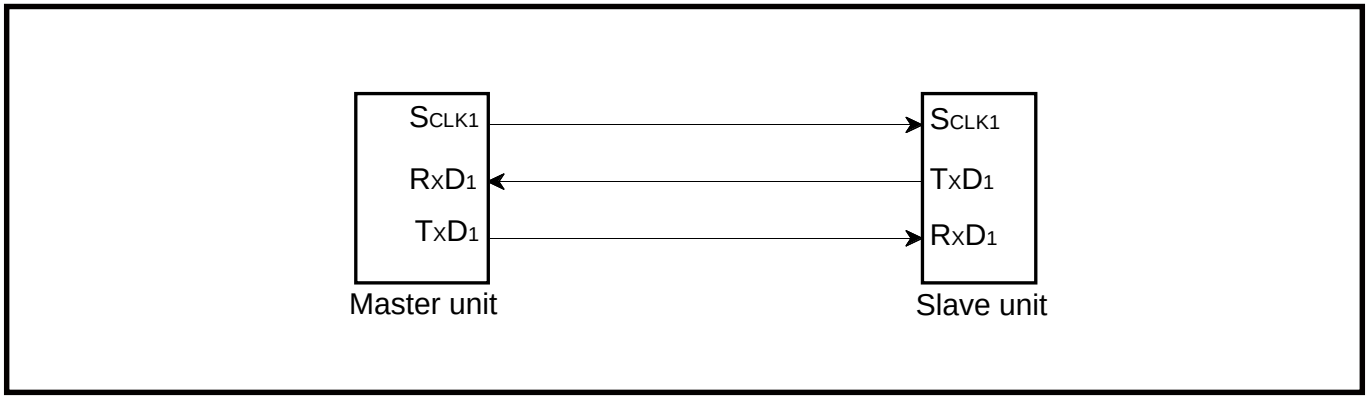


Fig. 2.4.33 Connection diagram

Specifications :

- The serial I/O1 is used (clock synchronous serial I/O is selected).
- Synchronous clock frequency : 125 kHz ($f(X_{IN})$ = 4 MHz is divided by 32)
- Byte cycle: 500 µs
- Number of bytes for transmission or reception : 8 byte/block
- Block transfer cycle : 16 ms
- Block transfer term : 4 ms
- Interval between blocks : 12 ms
- Heading adjustment time : 8 ms

Master side control

- Data is transmitted and received by interrupt routine executed every byte cycle (500 µs)

Slave side control

- Data is transmitted and received by serial I/O1 receive interrupt routine.
- The heading adjustment is carried out by interrupt routine executed every 1 ms.

Limitations of specifications :

- Reading of the reception data and writing of the next transmission data must be completed within the time obtained from "byte cycle – time for transferring 1-byte data" (in this example, the time taken from generating of the serial I/O1 receive interrupt request to input of the next synchronous clock is 436 µs).
- "Heading adjustment time < interval between blocks" must be satisfied.

The communication is performed according to the timing shown in Figure 2.4.34. In the slave unit, when a synchronous clock is not input within a certain time (heading adjustment time), the next clock input is processed as the beginning (heading) of a block.
When a clock is input again after one block (8 byte) is received, the clock is ignored.
Figure 2.4.35 shows relevant registers setting.

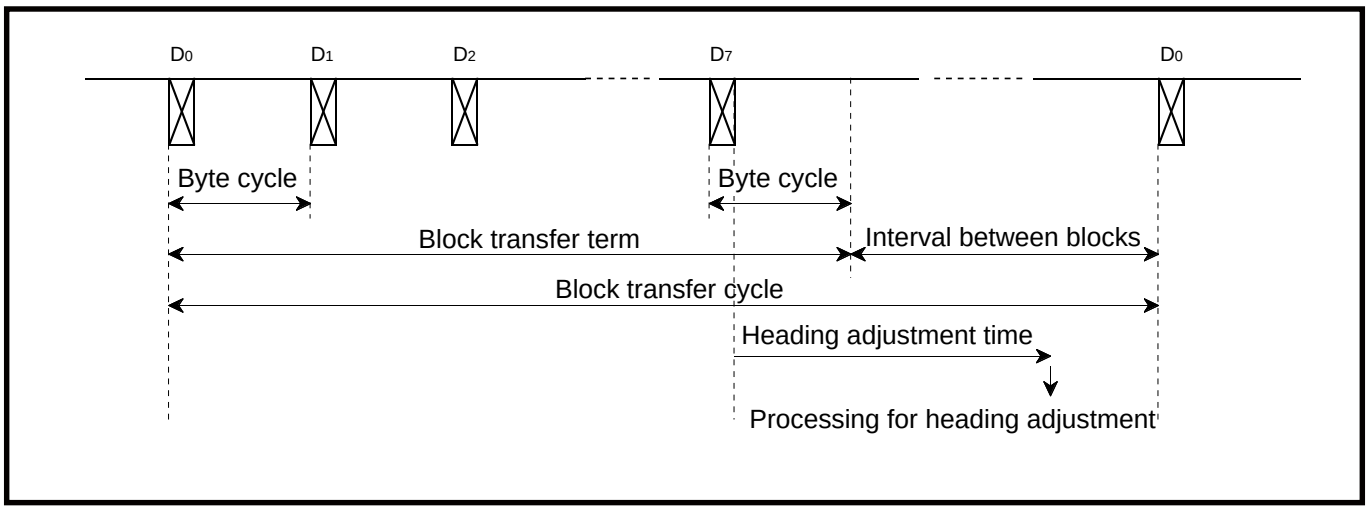


Fig. 2.4.34 Timing chart

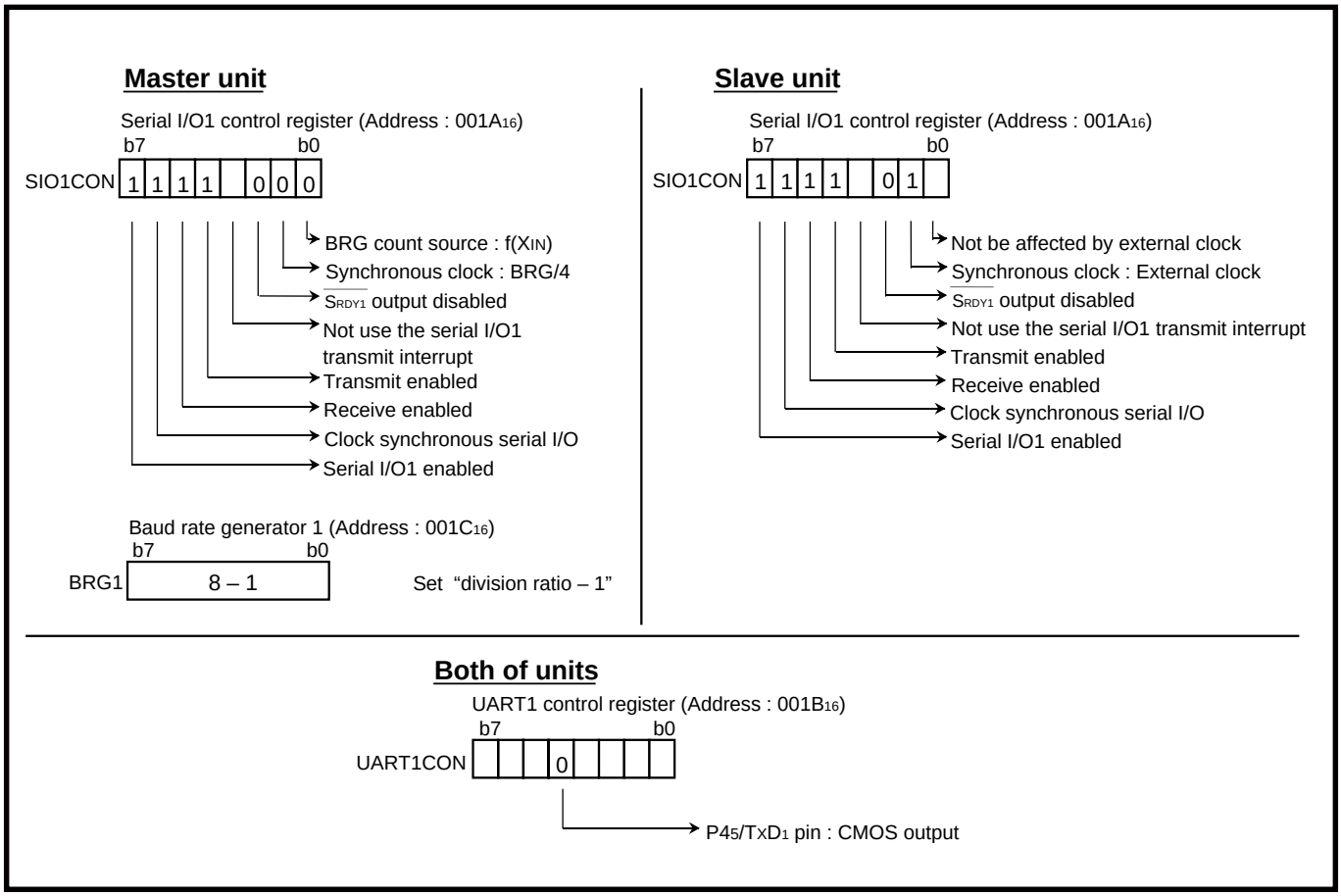


Fig. 2.4.35 Relevant registers setting

Control procedure :

● Control in the master unit

The master unit starts transmission or reception by writing transmission data to the transmit buffer register in the interrupt routine executed every 500 µs. In this interrupt routine, read the reception data before the next transmission data is written to the transmit buffer register. Additionally, transmission and reception of one block (8 bytes) is controlled and the block interval is generated. Figure 2.4.36 shows the control procedure of the master unit.

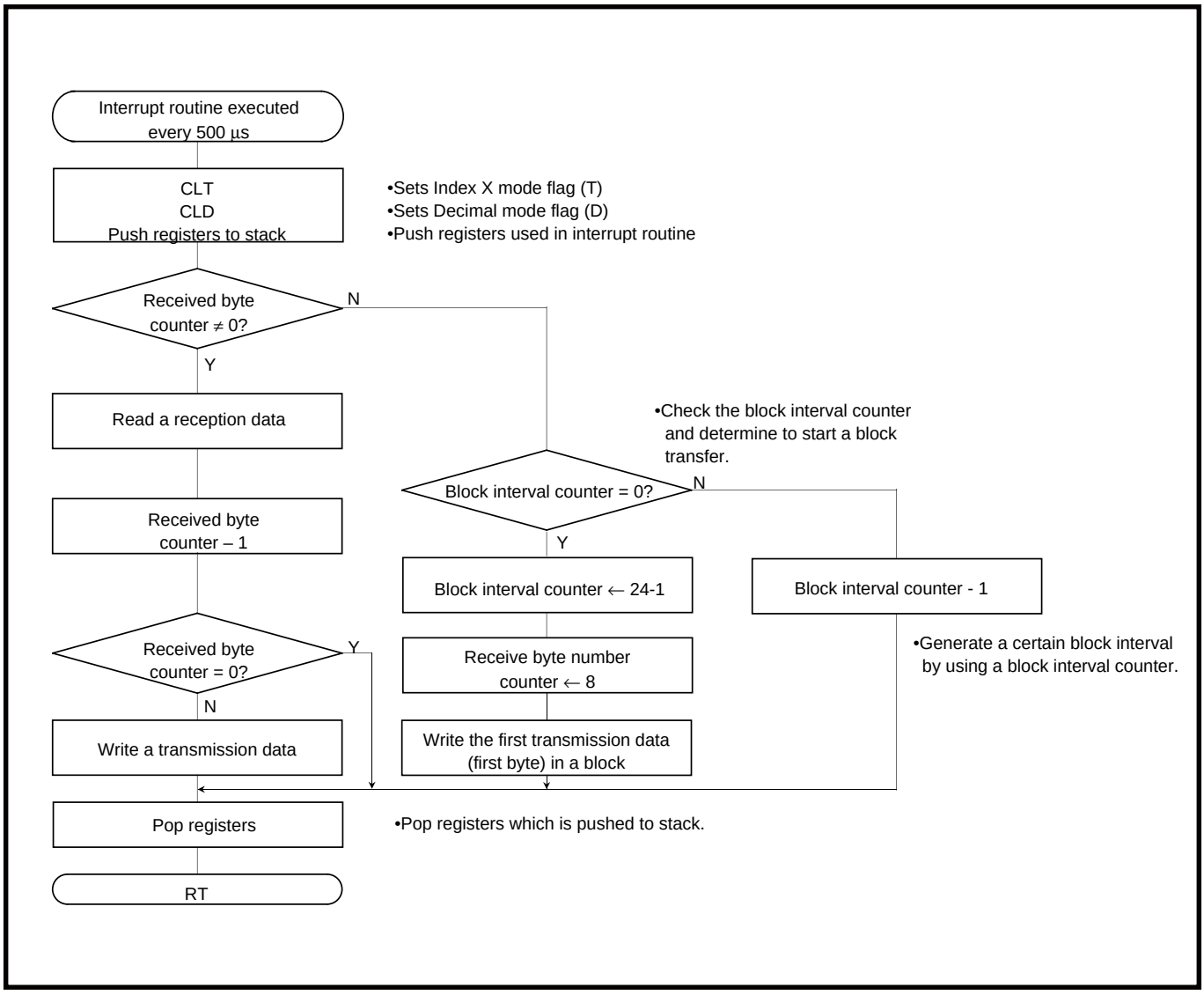


Fig. 2.4.36 Control procedure of master unit

● Control in the slave unit

After setting the relevant registers as shown in Figure 2.4.35, the slave unit becomes the state where a synchronous clock can be received at any time, and the serial I/O1 receive interrupt occurs each time an 8-bit synchronous clock is received.

In the serial I/O1 receive interrupt processing routine, the data to be transmitted next is written to the transmit buffer register after the received data is read out.

However, if no serial I/O1 receive interrupt occurs for a certain time (heading adjustment time or more), the following processing will be performed in the interrupt routine executed every 1 ms.

1. Serial I/O1 is initialized.
2. The first 1-byte data of the transmission data in the block is written into the transmit buffer register.
3. Since the data to be received next is processed as the first 1 byte of the received data in the block, the receive byte counter is initialized.

Figure 2.4.37 shows a control procedure of the slave unit.

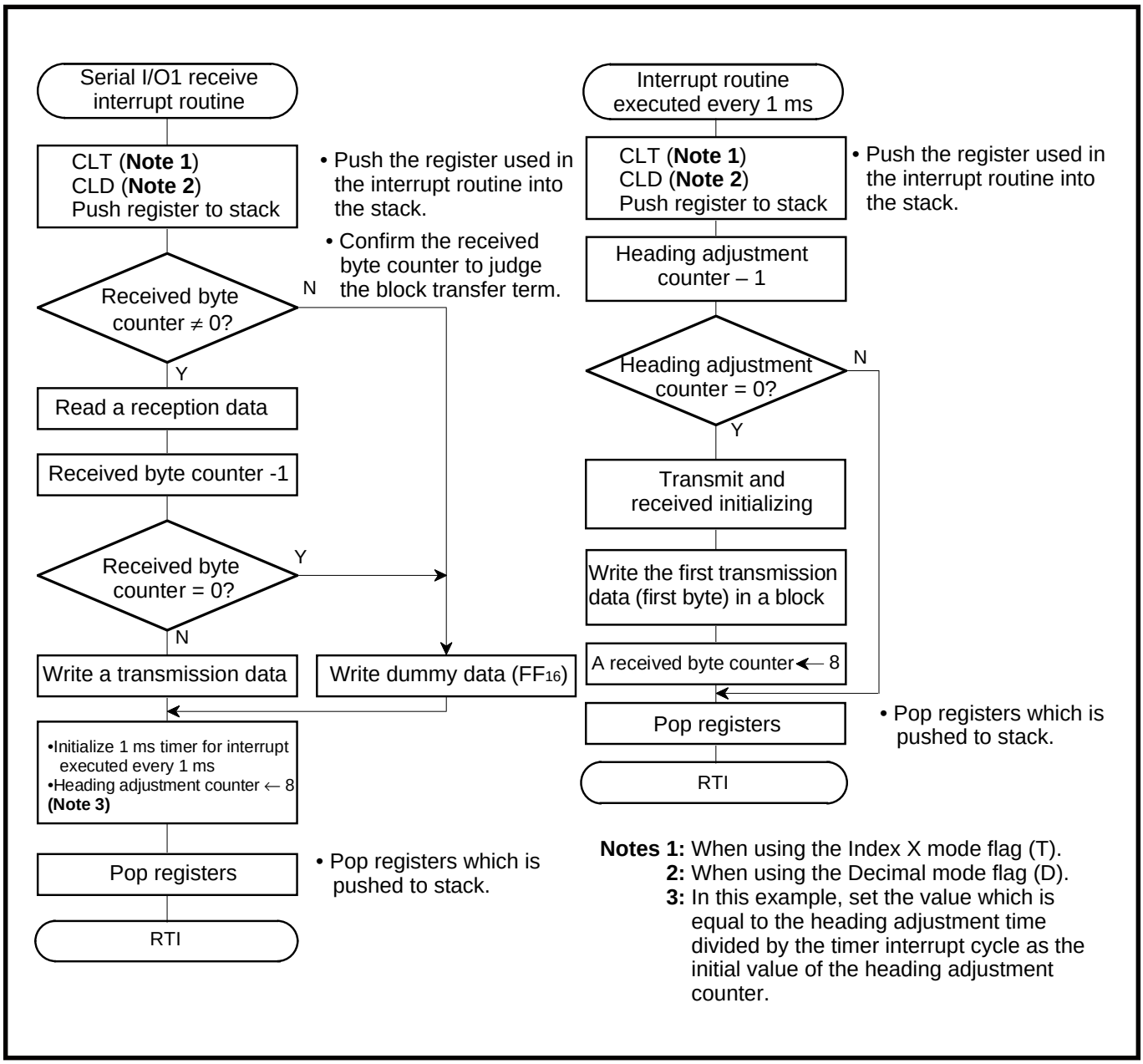


Fig. 2.4.37 Control procedure of slave unit

(4) Communication (transmit/receive) using asynchronous serial I/O (UART)

Outline : 2-byte data is transmitted and received, using the asynchronous serial I/O. Port $P4_0$ is used for communication control.

Figure 2.4.38 shows a connection diagram, and Figure 2.4.39 shows a timing chart.

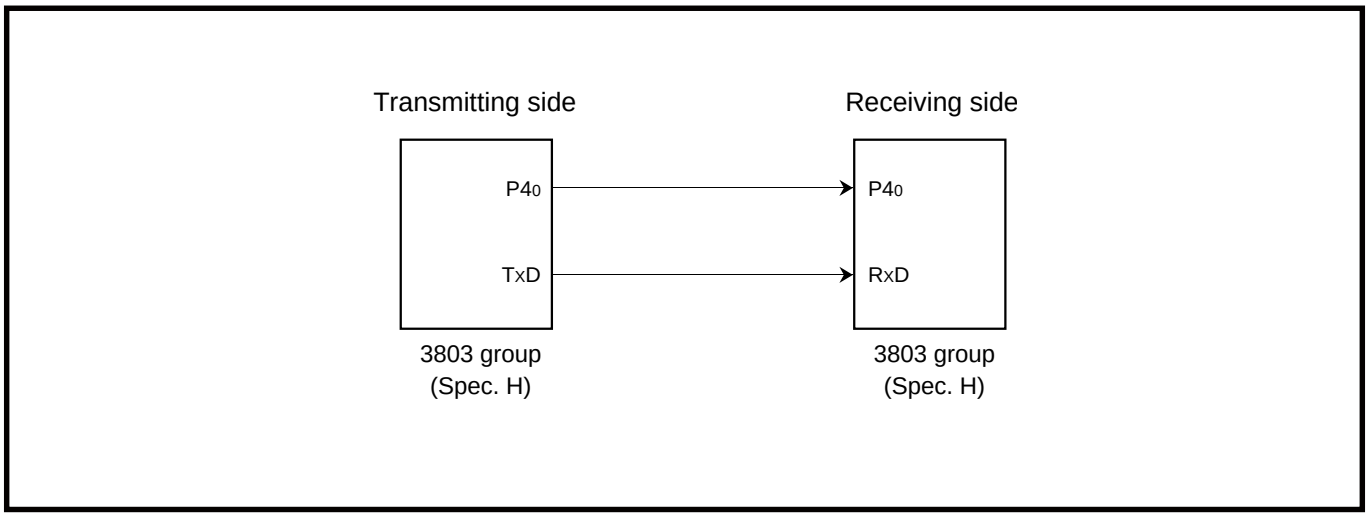


Fig. 2.4.38 Connection diagram (Communication using UART)

Specifications :
- Serial I/O1 is used (UART is selected).
- Transfer bit rate : 9600 bps ($f(X_{IN})$ = 4.9152 MHz is divided by 512)
- Communication control using port $P4_0$
  (The output level of port $P4_0$ is controlled by software.)
- 2-byte data is transferred from the transmitting side to the receiving side at intervals of 10 ms generated by the timer.

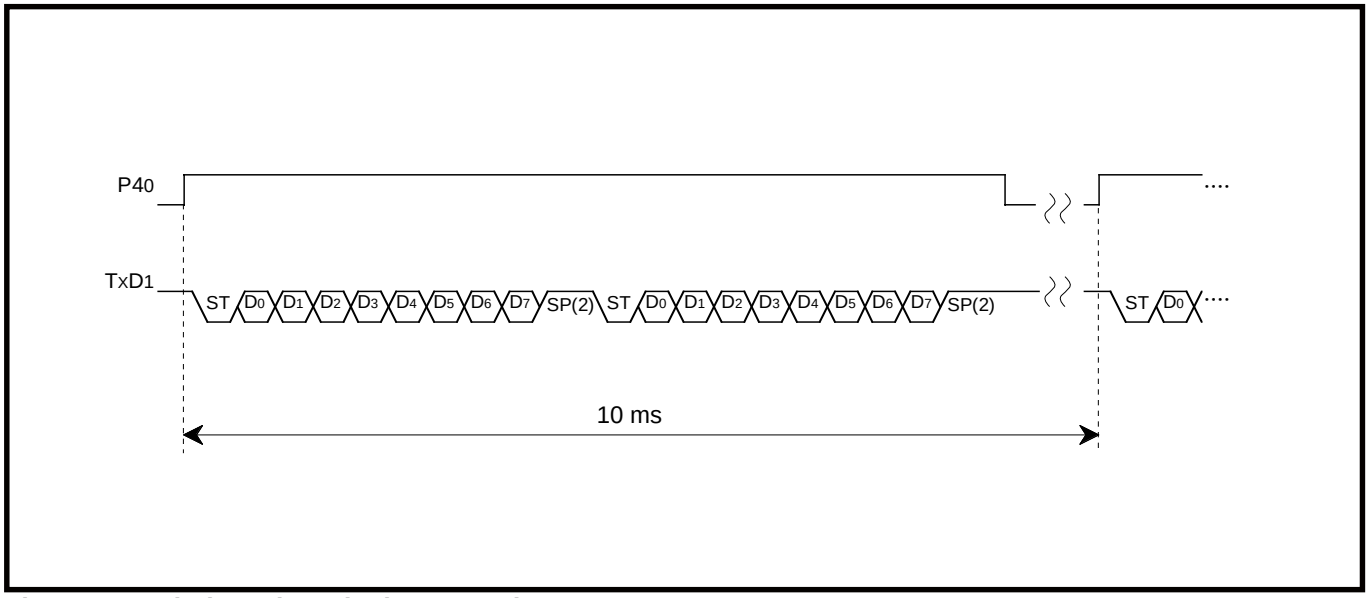


Fig. 2.4.39 Timing chart (using UART)

Table 2.4.4 shows setting examples of the baud rate generator (BRG) values and transfer bit rate values; Figure 2.4.40 shows registers setting relevant to the transmitting side; Figure 2.4.41 shows registers setting relevant to the receiving side.

Table 2.4.4 Setting examples of Baud rate generator (BRG) values and transfer bit rate values

BRG count source **(Note 1)**	BRG setting value	Transfer bit rate (bps) **(Note 2)**	
		at f(XIN) = 4.9152 MHz	at f(XIN) = 16 MHz
f(XIN)/4	255(FF_{16})	300	976.5625
f(XIN)/4	127($7F_{16}$)	600	1953.125
f(XIN)/4	63($3F_{16}$)	1200	3906.25
f(XIN)/4	31($1F_{16}$)	2400	7812.5
f(XIN)/4	15($0F_{16}$)	4800	15625
f(XIN)/4	7(07_{16})	9600	31250
f(XIN)/4	3(03_{16})	19200	62500
f(XIN)/4	1(01_{16})	38400	125000
f(XIN)	3(03_{16})	76800	250000
f(XIN)	1(01_{16})	153600	500000
f(XIN)	0(00_{16})	307200	1000000

Notes 1: Select the BRG count source with bit 0 of the serial I/O1 control register (Address : $1A_{16}$).

2: Equation of transfer bit rate:

$$\text{Transfer bit rate (bps)} = \frac{f(X_{IN})}{(\text{BRG setting value} + 1) \times 16 \times m^{*}}$$

*m: When bit 0 of the serial I/O1 control register (Address : $1A_{16}$) is set to “0,” a value of m is 1.
When bit 0 of the serial I/O1 control register (Address : $1A_{16}$) is set to “1,” a value of m is 4.

Transmitting side

Serial I/O1 status register (Address : 0019_{16})

SIO1STS

b7							b0

- b0 → Transmit buffer empty flag
  - • Confirm that the data has been transferred from Transmit buffer register to Transmit shift register.
  - • When this flag is "1", it is possible to write the next transmission data in to Transmit buffer register.
- b1 → Transmit shift register shift completion flag
  - Confirm completion of transmitting 1-byte data with this flag.
  - "1" : Transmit shift completed

Serial I/O1 control register (Address : $001A_{16}$)

SIO1CON

b7							b0
1	0	0	1		0	0	1

- b0 → BRG count source : f(X_{IN})/4
- b1 → Synchronous clock : BRG/16
- b2 → $\overline{S_{RDY1}}$ output disabled
- b3 → Transmit enabled
- b4 → Receive disabled
- b5 → Asynchronous serial I/O(UART)
- b7 → Serial I/O1 enabled

UART1 control register (Address : $001B_{16}$)

UART1CON

b7							b0
			0	1		0	0

- b0 → Character length : 8 bits
- b1 → Parity checking disabled
- b2 → Stop bit length : 2 stop bits
- b3 → $P4_5/TxD_1$ pin : CMOS output

Baud rate generator 1 (Address : $001C_{16}$)

BRG1

b7							b0
8 – 1							

$$\text{Set } \frac{f(X_{IN})}{\text{Transfer bit rate} \times 16 \times m \ *} - 1$$

✻ When bit 0 of Serial I/O1 control register (Address : $001A_{16}$) is set to "0," a value of m is 1.
When bit 0 of Serial I/O1 control register (Address : $001A_{16}$) is set to "1," a value of m is 4.

Port P4 (Address : 0008_{16})

P4

b7							b0
							0

- b0 → Port $P4_0$: Communication control: "H" active

Port P4 direction register (Address : 0009_{16})

P4D

b7							b0
							1

- b0 → Port $P4_0$: Communication control: Output mode

Fig. 2.4.40 Registers setting relevant to transmitting side

Receiving side

Serial I/O1 status register (Address : 0019_{16})

SIO1STS (b7 … b0)

- Receive buffer full flag
  Confirm completion of receiving 1-byte data with this flag.
  - "1" : at completing reception
  - "0" : at reading out contents of Receive buffer register
- Overrun error flag
  "1" : When data is ready in Receive shift register while Receive buffer register contains the data.
- Parity error flag
  "1" : When a parity error occurs in enabled parity.
- Framing error flag
  "1" : When stop bits cannot be detected at the specified timing
- Summing error flag
  "1" : when any one of the following errors occurs.
  - Overrun error
  - Parity error
  - Framing error

Serial I/O1 control register (Address : $001A_{16}$)

SIO1CON (b7 … b0) = 1 0 1 0 _ 0 0 1

- BRG count source : $f(X_{IN})/4$
- Synchronous clock : BRG/16
- $\overline{S_{RDY1}}$ output disabled
- Transmit disabled
- Receive enabled
- Asynchronous serial I/O(UART)
- Serial I/O1 enabled

UART1 control register (Address : $001B_{16}$)

UART1CON (b7 … b0) = _ _ _ _ 1 _ 0 0

- Character length : 8 bits
- Parity checking disabled
- Stop bit length : 2 stop bits

Baud rate generator 1 (Address : $001C_{16}$)

BRG1 (b7 … b0) = 8 – 1

$$\text{Set } \frac{f(X_{IN})}{\text{Transfer bit rate} \times 16 \times m \ *} - 1$$

* When bit 0 of Serial I/O1 control register (Address : $001A_{16}$) is set to "0," a value of m is 1.
When bit 0 of Serial I/O1 control register (Address : $001A_{16}$) is set to "1," a value of m is 4.

Port P4 direction register (Address : 0009_{16})

P4D (b7 … b0) = _ _ _ _ _ _ _ 0

- Port $P4_0$: Communication control: Input mode

Fig. 2.4.41 Registers setting relevant to receiving side

Figure 2.4.42 shows a control procedure of the transmitting side, and Figure 2.4.43 shows a control procedure of the receiving side.

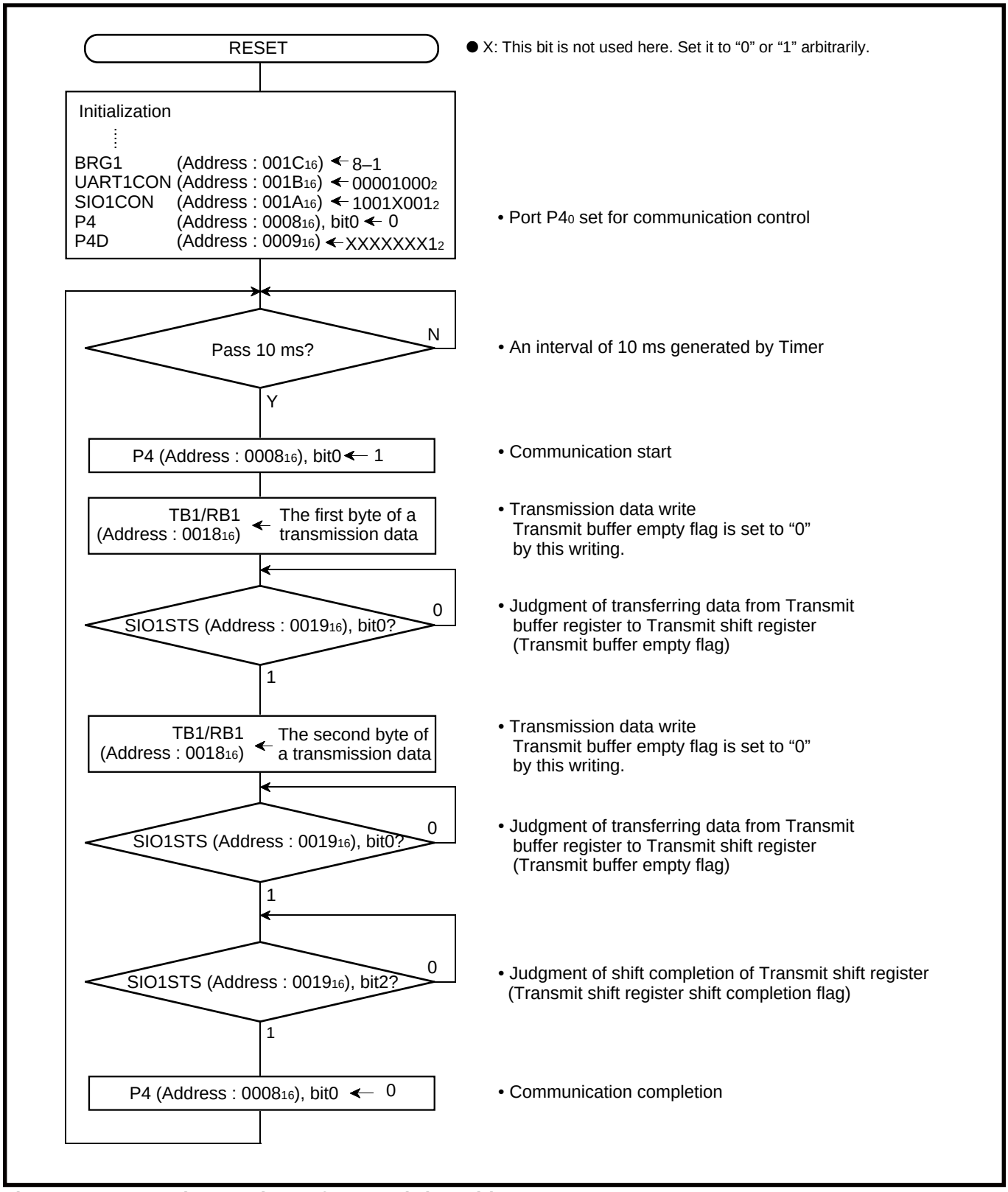


Fig. 2.4.42 Control procedure of transmitting side

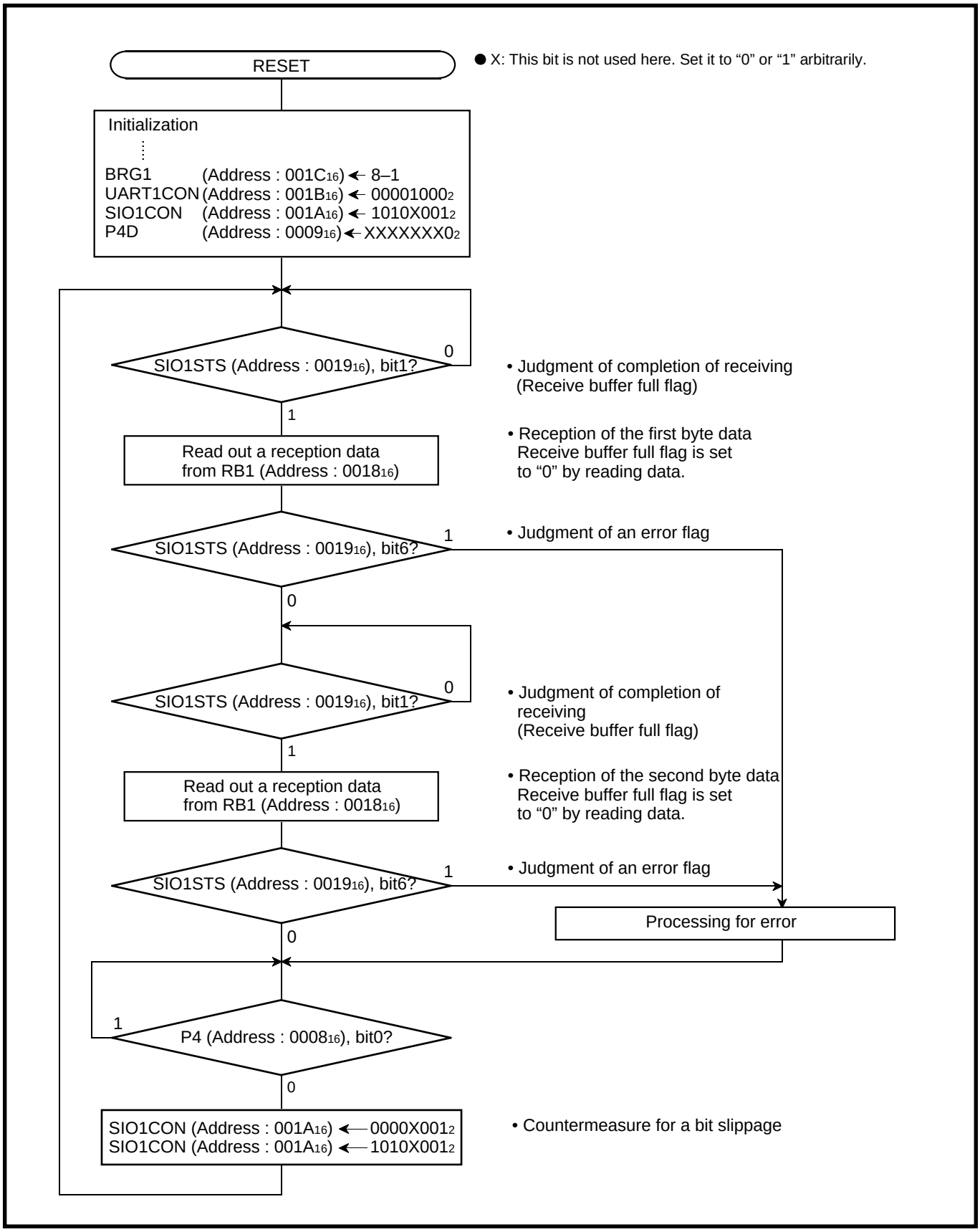


Fig. 2.4.43 Control procedure of receiving side

2.4.8 Notes on serial I/O

(1) Notes when selecting clock synchronous serial I/O

① **Stop of transmission operation**
As for serial I/Oi (i = 1, 3) that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the serial I/Oi enable bit and the transmit enable bit to “0” (serial I/Oi and transmit disabled).

● **Reason**
Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/Oi enable bit is cleared to “0” (serial I/Oi disabled), the internal transmission is running (in this case, since pins TxDi, RxDi, SCLKi, and $\overline{\text{SRDY}i}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/Oi enable bit is set to “1” at this time, the data during internally shifting is output to the TxDi pin and an operation failure occurs.

② **Stop of receive operation**
As for serial I/Oi (i = 1, 3) that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the receive enable bit to “0” (receive disabled), or clear the serial I/Oi enable bit to “0” (serial I/Oi disabled).

③ **Stop of transmit/receive operation**
As for serial I/Oi (i = 1, 3) that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear both the transmit enable bit and receive enable bit to “0” simultaneously (transmit and receive disabled) in the clock synchronous serial I/O mode.
(When data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

● **Reason**
In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.
In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to “0” (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/Oi enable bit to “0” (serial I/Oi disabled) (refer to ① in (1)).

(2) Notes when selecting clock asynchronous serial I/O

① **Stop of transmission operation**
Clear the transmit enable bit to “0” (transmit disabled). Transmission operation does not stop by setting the serial I/Oi enable bit (i = 1, 3) to “0”.

● **Reason**
This is the same as ① in (1).

② **Stop of receive operation**
Clear the receive enable bit to “0” (receive disabled).

③ **Stop of transmit/receive operation**

Only transmission operation is stopped.

Clear the transmit enable bit to “0” (transmit disabled). Transmission operation does not stop by setting the serial I/Oi enable bit (i = 1, 3) to “0”.

● **Reason**

This is the same as ① in (1).

Only receive operation is stopped.

Clear the receive enable bit to “0” (receive disabled).

(3) $\overline{\text{SRDY}}$ output of reception side

When signals are output from the $\overline{\text{SRDYi}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDYi}}$ output enable bit, and the transmit enable bit to “1” (transmit enabled).

(4) Setting serial I/Oi (i = 1, 3) control register again

Set the serial I/Oi control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to “0.”

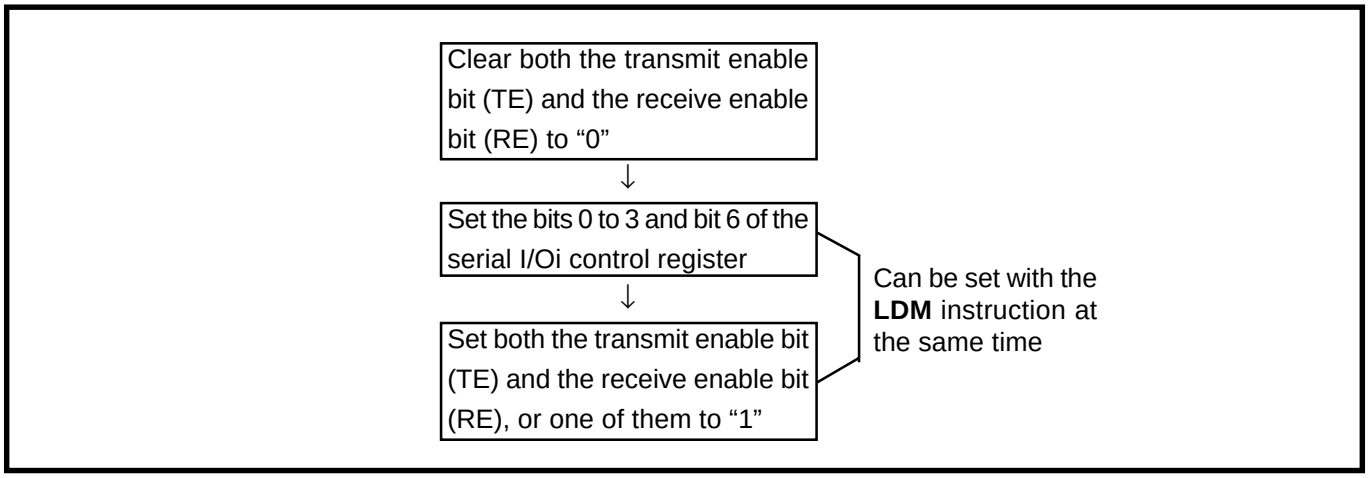


Fig. 2.4.44 Sequence of setting serial I/Oi (i = 1, 3) control register again

(5) Data transmission control with referring to transmit shift register completion flag

After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

(6) Transmission control when external clock is selected

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to “1” at “H” of the $\text{SCLK}i$ (i = 1, 3) input level. Also, write the transmit data to the transmit buffer register at “H” of the $\text{SCLK}i$ input level.

(7) Transmit interrupt request when transmit enable bit is set

When the transmit interrupt is used, take the following sequence.

① Set the serial I/O transmit interrupt enable bit to “0” (disabled).
② Set the tranasmit enable bit to “1”.
③ Set the serial I/O transmit interrupt request bit to “0” after 1 or more instruction has executed.
④ Set the serial I/O transmit interrupt enable bit to “1” (enabled).

● **Reason**

When the transmission enable bit is set to “1”, the transmit buffer empty flag and transmit shift register completion flag are set to “1”.

The transmission interrupt request bit is set and the interrupt request occurs even when selecting timing that either of the following flags is set to “1” as timing where the transmission interrupt occurs.

- Transmit buffer empty flag is set to “1”
- Transmit shift register completion flag is set to “1”

(8) Writing to baud rate generator

Write data to the baud rate generator i (BRGi) (i = 1, 3) while the transmission/reception operation is stopped.

2.5 PWM

This paragraph explains the registers setting method and the notes relevant to the PWM.

2.5.1 Memory map

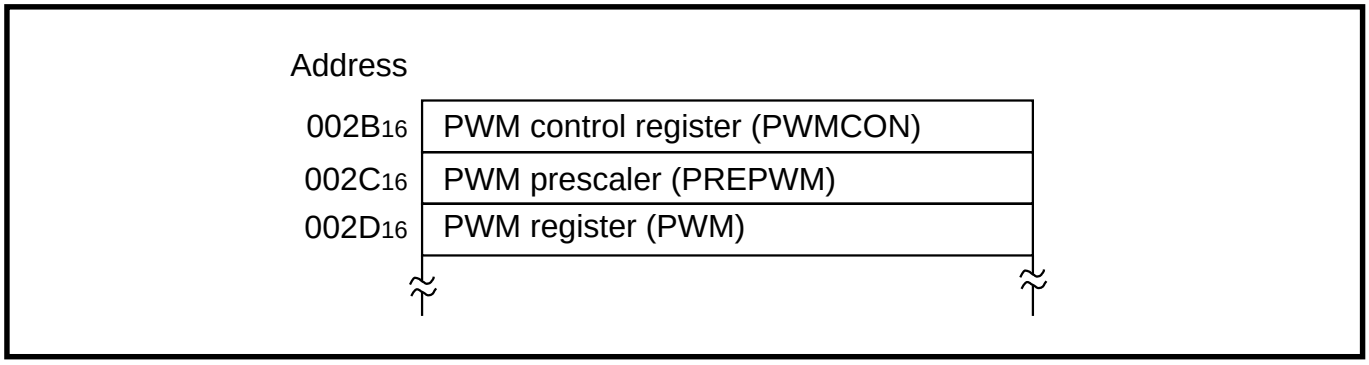


Fig. 2.5.1 Memory map of registers relevant to PWM

2.5.2 Relevant registers

PWM control register

b7 b6 b5 b4 b3 b2 b1 b0

PWM control register (PWMCON: address 002B16)

b	Name	Functions	At reset	R	W
0	PWM function enable bit	0 : PWM disabled 1 : PWM enabled	0	○	○
1	Count source selection bit	0 : f(XIN) 1 : f(XIN)/2	0	○	○
2	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “0”.		0	○	×
3			0	○	×
4			0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 2.5.2 Structure of PWM control register

PWM prescaler

b7 b6 b5 b4 b3 b2 b1 b0

PWM prescaler
(PREPWM: address 002C16)

b	Functions	At reset	R	W
0	•Set the PWM period. •The value set in this register is written to both PWM prescaler pre-latch and PWM prescaler latch at the same time. • When data is written to this register during PWM output, the pulse corresponding to changed value is output at the next period. • When this register is read out, the count value of the PWM prescaler latch is read out.	Undefined	○	○
1		Undefined	○	○
2		Undefined	○	○
3		Undefined	○	○
4		Undefined	○	○
5		Undefined	○	○
6		Undefined	○	○
7		Undefined	○	○

Fig. 2.5.3 Structure of PWM prescaler

PWM register

b7 b6 b5 b4 b3 b2 b1 b0

PWM register
(PWM: address 002D16)

b	Functions	At reset	R	W
0	• Set the PWM “H” level output interval. • The value set in this register is written to both PWM register pre-latch and PWM register latch at the same time. • When data is written to this register during PWM output, the pulse corresponding to changed value is output at the next period. • When this register is read out, the contents of the PWM register latch is read out.	Undefined	○	○
1		Undefined	○	○
2		Undefined	○	○
3		Undefined	○	○
4		Undefined	○	○
5		Undefined	○	○
6		Undefined	○	○
7		Undefined	○	○

Fig. 2.5.4 Structure of PWM register

2.5.3 PWM output circuit application example

<Motor control>

Outline : The rotation speed of the motor is controlled by using PWM (pulse width modulation) output.

Figure 2.5.5 shows a connection diagram ; Figures 2.5.6 shows PWM output timing, and Figure 2.5.7 shows a setting of the related registers.

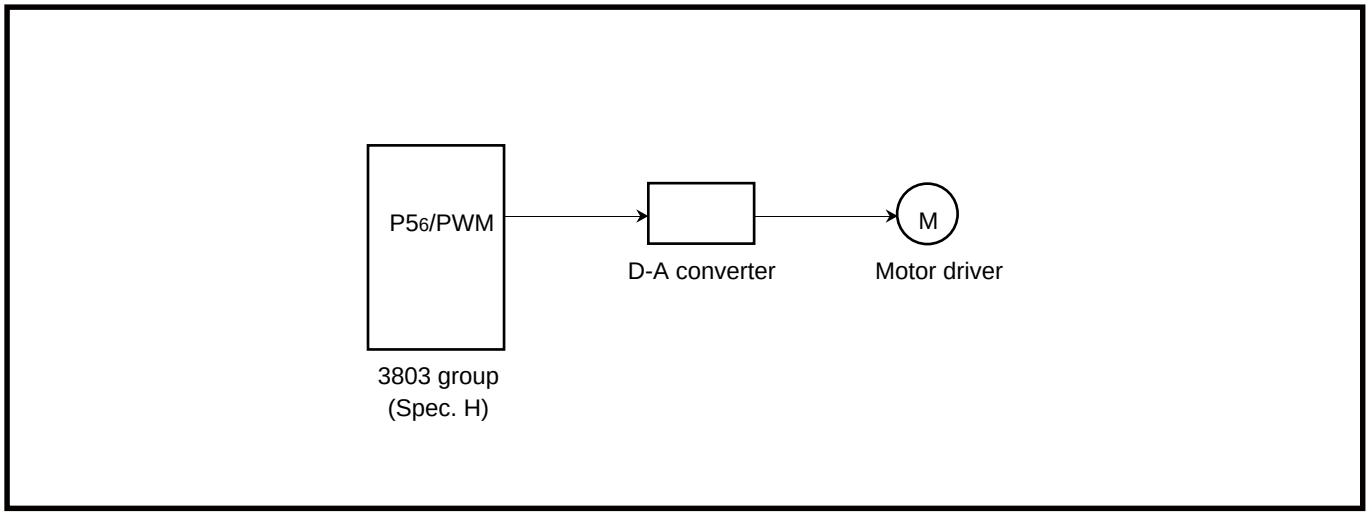


Fig. 2.5.5 Connection diagram

Specifications :
- Motor is controlled by using the PWM output function of 8-bit resolution.
- Clock f(XIN) = 5 MHz
- "T", PWM cycle : 102 μs
- "t", "H" level width of output pulse : 40 μs (Fixed speed)

✻ A motor speed can be changed by modifying the "H" level width of output pulse.

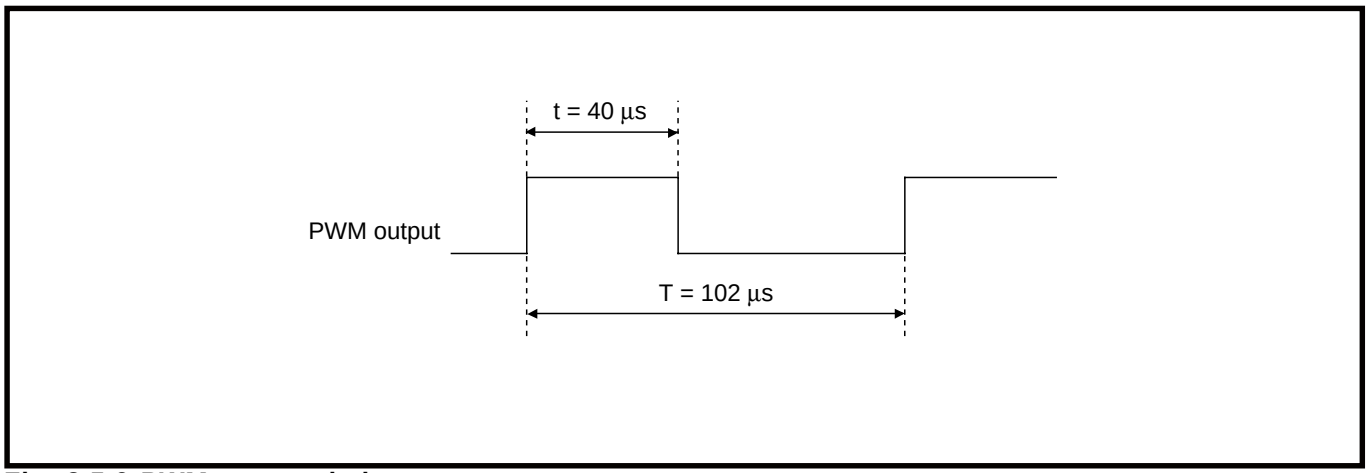


Fig. 2.5.6 PWM output timing

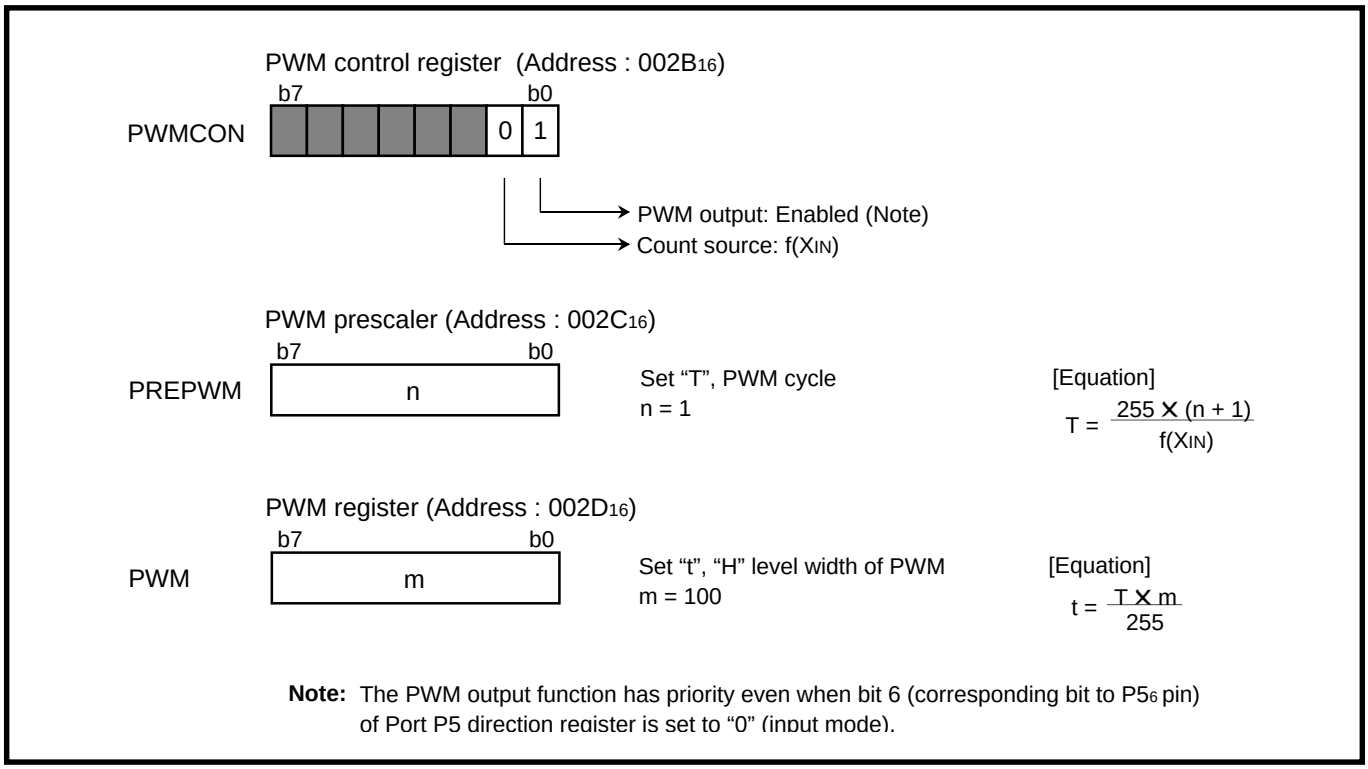


Fig. 2.5.7 Setting of relevant registers

<About PWM output>

1. Set the PWM function enable bit to "1" : The P56/PWM pin is used as the PWM pin.
   The pulse beginning with "H" level pulse is output.
2. Set the PWM function enable bit to "0" : The P56/PWM pin is used as the port P56.
   Thus, when fixing the output level, take the following procedure:
   (1) Write an output value to bit 6 of the port P5 register.
   (2) Write "01000000$_2$" to the port P5 direction register.
3. After data is set to the PWM prescaler and the PWM register, the PWM waveforms corresponding to updated data will be output from the next repetitive cycle.

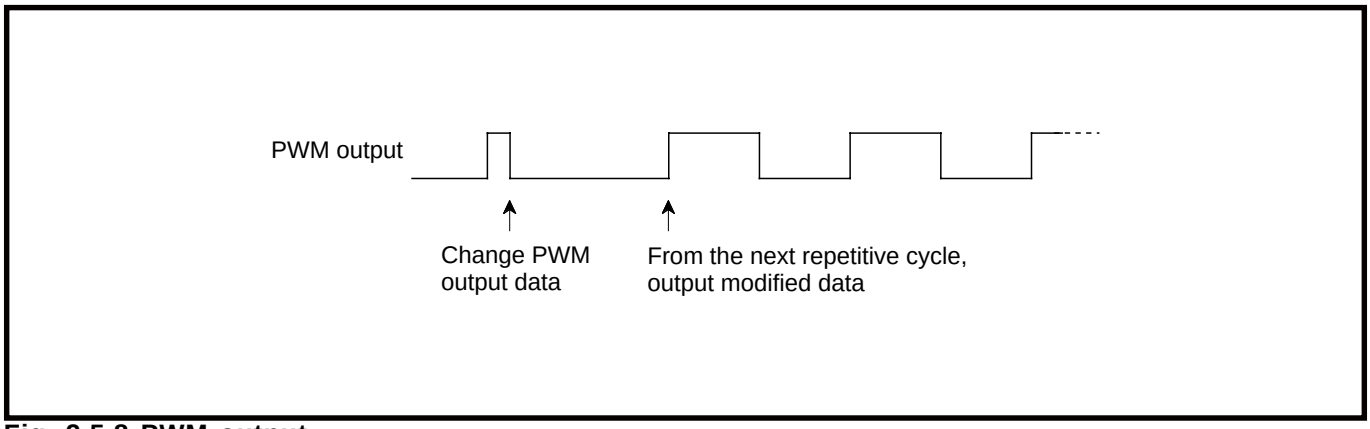


Fig. 2.5.8 PWM output

By setting the related registers as shown by Figure 2.5.7, PWM waveforms are output to the externals. This PWM output is integrated through the low pass filter, and that converted into DC signals is used for control of the motor. Figure 2.5.9 shows control procedure.

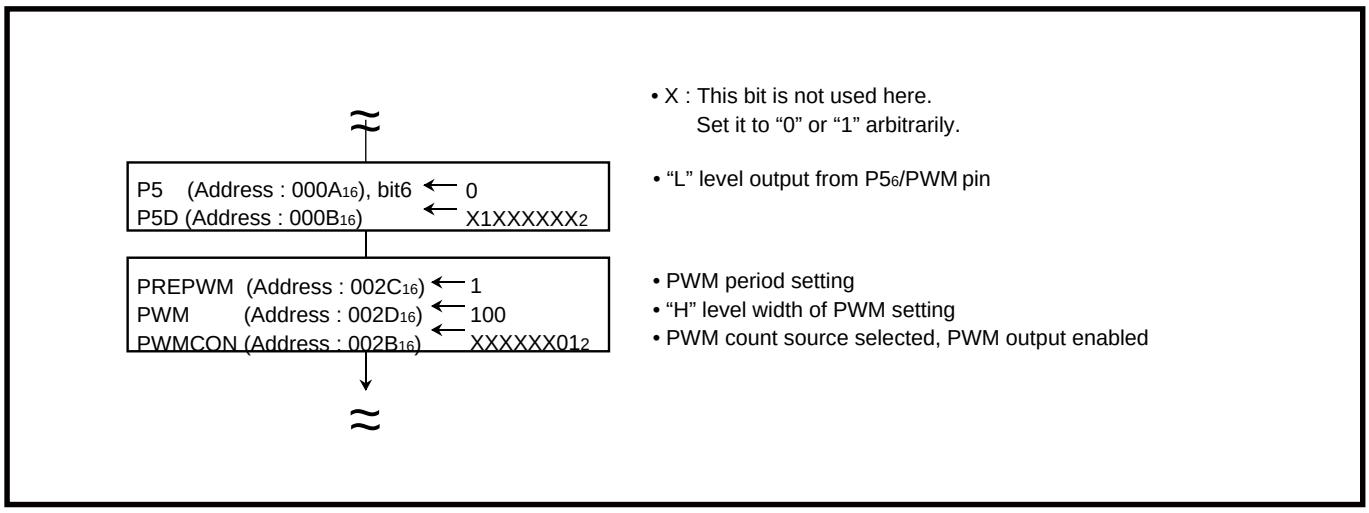


Fig. 2.5.9 Control procedure

2.5.4 Notes on PWM

The PWM starts after the PWM enable bit is set to enable and "L" level is output from the PWM pin. The length of this "L" level output is as follows:

$$\frac{n + 1}{2 \cdot f(X_{IN})} \text{ (s)} \quad \text{(Count source selection bit = 0, where n is the value set in the prescaler)}$$

$$\frac{n + 1}{f(X_{IN})} \text{ (s)} \quad \text{(Count source selection bit = 1, where n is the value set in the prescaler)}$$

2.6 A-D converter

This paragraph explains the registers setting method and the notes relevant to the A-D converter.

2.6.1 Memory map

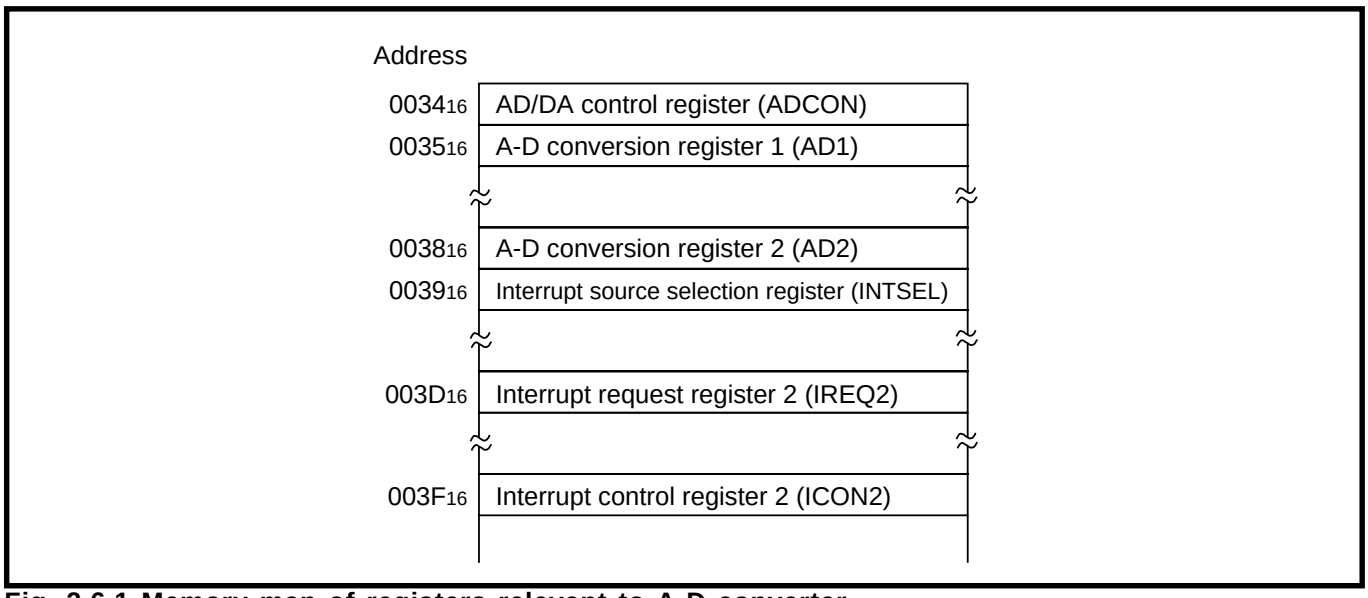


Fig. 2.6.1 Memory map of registers relevant to A-D converter

2.6.2 Relevant registers

AD/DA control register

b7 b6 b5 b4 b3 b2 b1 b0

AD/DA control register
(ADCON: address 0034₁₆)

b	Name	Functions	At reset	R	W
0	Analog input pin selection bits 1	b2 b1 b0 0 0 0: P6₀/AN₀ or P0₀/AN₈ 0 0 1: P6₁/AN₁ or P0₁/AN₉ 0 1 0: P6₂/AN₂ or P0₂/AN₁₀ 0 1 1: P6₃/AN₃ or P0₃/AN₁₁ 1 0 0: P6₄/AN₄ or P0₄/AN₁₂ 1 0 1: P6₅/AN₅ or P0₅/AN₁₃ 1 1 0: P6₆/AN₆ or P0₆/AN₁₄ 1 1 1: P6₇/AN₇ or P0₇/AN₁₅	0	○	○
1			0	○	○
2			0	○	○
3	AD conversion completion bit	0: Conversion in progress 1: Conversion completed	1	○	○
4	Analog input pin selection bit 2	0: AN₀ to AN₇ side 1: AN₈ to AN₁₅ side	0	○	○
5	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are “0”.		0	○	×
6	DA₁ output enable bit	0: DA₁ output disabled 1: DA₁ output enabled	0	○	○
7	DA₂ output enable bit	0: DA₂ output disabled 1: DA₂ output enabled	0	○	○

Fig. 2.6.2 Structure of AD/DA control register

A-D conversion register 1

b7 b6 b5 b4 b3 b2 b1 b0

A-D conversion register 1
(AD1: address 0035$_{16}$)

b	Functions	At reset	R	W
0	This is A-D conversion result stored bits. This is read exclusive register. 8-bit read: b7 … b0 = b9 b8 b7 b6 b5 b4 b3 b2 10-bit read: b7 … b0 = b7 b6 b5 b4 b3 b2 b1 b0	Undefined	○	×
1		Undefined	○	×
2		Undefined	○	×
3		Undefined	○	×
4		Undefined	○	×
5		Undefined	○	×
6		Undefined	○	×
7		Undefined	○	×

Fig. 2.6.3 Structure of A-D conversion register 1

A-D conversion register 2

b7 b6 b5 b4 b3 b2 b1 b0

A-D conversion register 2
(AD2: address 0038$_{16}$)

b	Functions		At reset	R	W
0	This is A-D conversion result stored bits. This is read exclusive register. 10-bit read: b7 … b0 = b9 b8		Undefined	○	×
1			Undefined	○	×
2	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “0”.		0	○	×
3			0	○	×
4			0	○	×
5			0	○	×
6			0	○	×
7	Conversion mode selection bit	0: 10-bit A-D mode 1: 8-bit A-D mode	0	○	○

Fig. 2.6.4 Structure of A-D conversion register 2

Interrupt source selection register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt source selection register
(INTSEL: address 0039_{16})

b	Name	Functions	At reset	R	W
0	INT_0/Timer Z interrupt source selection bit (*1)	0: INT_0 interrupt 1: Timer Z interrupt	0	○	○
1	Serial I/O2/Timer Z interrupt source selection bit (*1)	0: Serial I/O2 interrupt 1: Timer Z interrupt	0	○	○
2	Nothing is arranged for these bits. Do not write "1" to these bits. When these bits are read out, the contents are "0".		0	○	○
3			0	○	○
4	INT_4/$CNTR_2$ interrupt source selection bit	0: INT_4 interrupt 1: $CNTR_2$ interrupt	0	○	○
5	Nothing is arranged for this bit. Do not write "1" to this bit. When this bit is read out, the contents are "0".		0	○	○
6	$CNTR_1$/Serial I/O3 receive interrupt source selection bit	0: $CNTR_1$ interrupt 1: Serial I/O3 receive interrupt	0	○	○
7	AD converter/Serial I/O3 transmit interrupt source selection bit	0: A-D converter interrupt 1: Serial I/O3 transmit interrupt	0	○	○

*1: Do not write "1" to these bits simultaneously.

Fig. 2.6.5 Structure of Interrupt source selection register

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2
(IREQ2 : address 003D16)

b	Name	Functions	At reset	R	W
0	CNTR0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	CNTR1/Serial I/O3 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	Serial I/O2/Timer Z interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	INT2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	INT3 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	INT4/CNTR2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	AD converter/Serial I/O3 transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are “0”.		0	○	×

✻: “0” can be set by software, but “1” cannot be set.

Fig. 2.6.6 Structure of Interrupt request register 2

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0
0

Interrupt control register 2
(ICON2 : address 003F16)

b	Name	Functions	At reset	R	W
0	CNTR0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	CNTR1/ Serial I/O3 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Serial I/O2/ Timer Z interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	INT2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT3 interrupt enable bit	0 : Interrupt disabled	0	○	○
5	INT4/CNTR2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	AD converter/Serial I/O3 transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to “0”.		0	○	○

Fig. 2.6.7 Structure of Interrupt control register 2

2.6.3 A-D converter application examples

(1) Conversion of analog input voltage 1

Outline : The analog input voltage input from a sensor is converted to digital values.

Figure 2.6.8 shows a connection diagram, and Figure 2.6.9 shows the relevant registers setting.

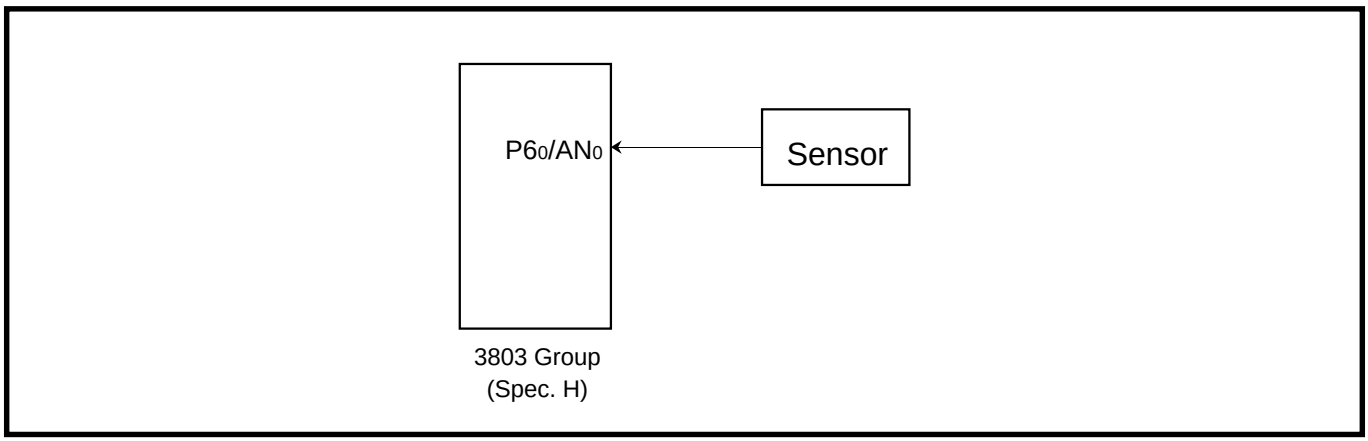


Fig. 2.6.8 Connection diagram

Specifications : •The analog input voltage input from a sensor is converted to digital values.
•P6₀/AN₀ pin is used as an analog input pin.
•10-bit A-D mode

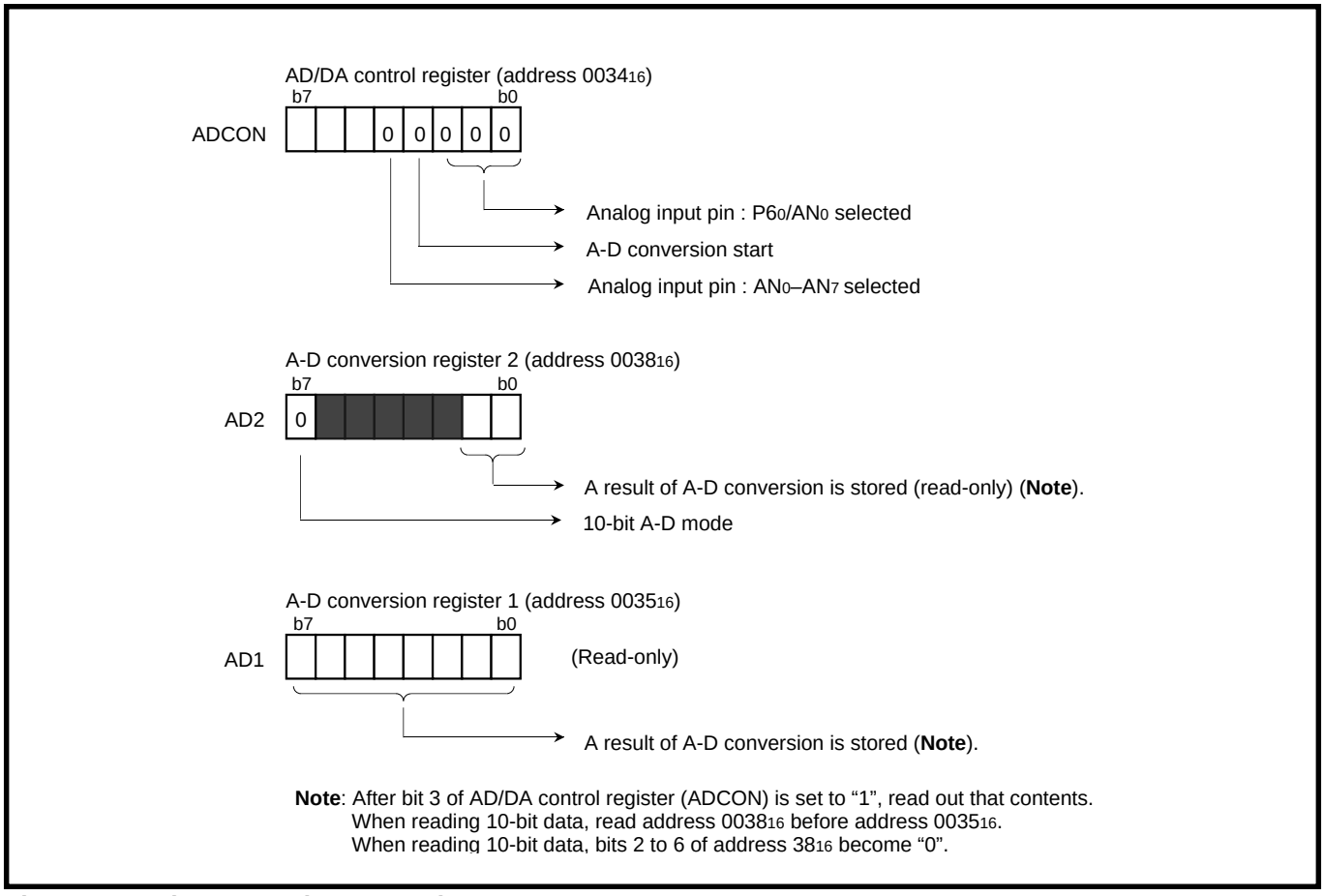


Fig. 2.6.9 Relevant registers setting

An analog input signal from a sensor is converted to the digital value according to the relevant registers setting shown by Figure 2.6.9. Figure 2.6.10 shows the control procedure for 10-bit A-D mode.

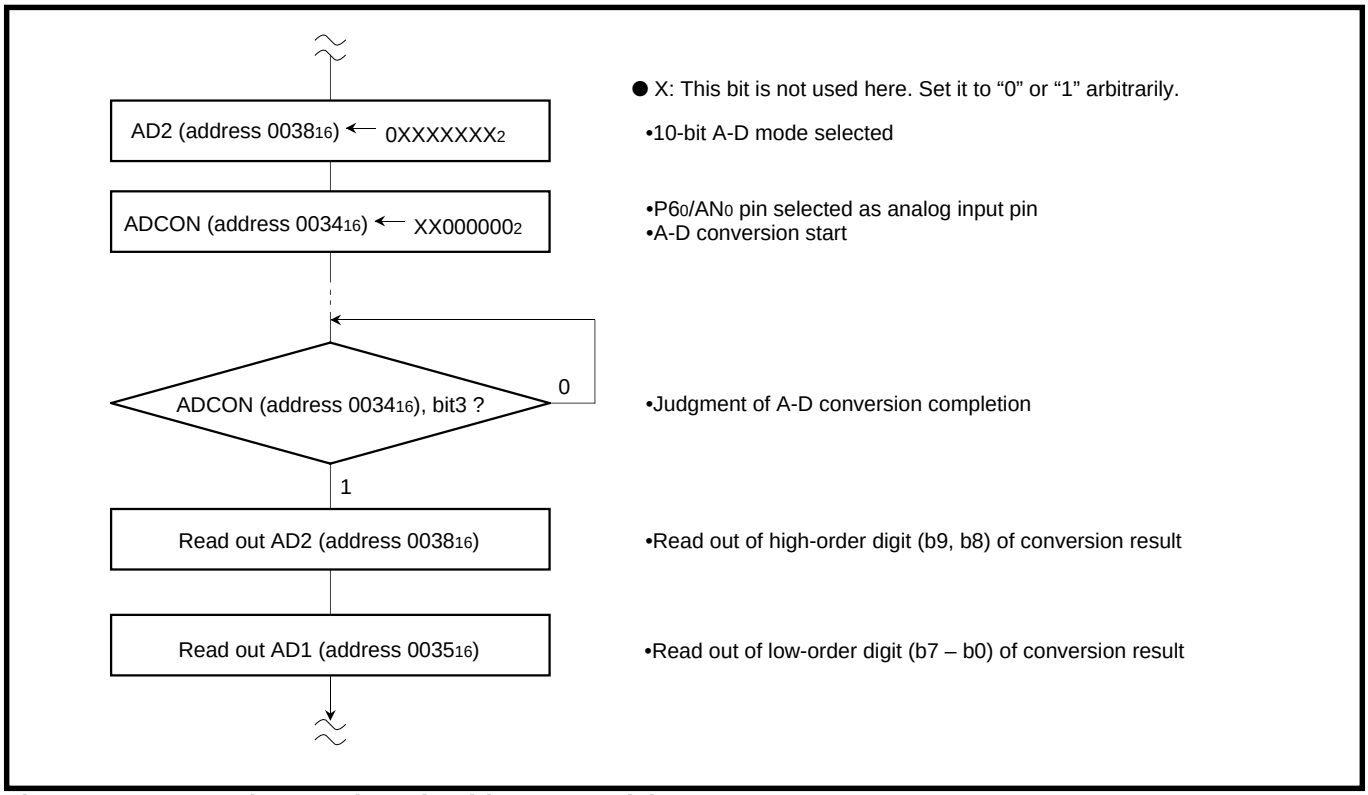


Fig. 2.6.10 Control procedure (10-bit A-D mode)

(2) Conversion of analog input voltage 2

Outline : The analog input voltage input from a sensor is converted to digital values.

Figure 2.6.11 shows a connection diagram, and Figure 2.6.12 shows the relevant registers setting.

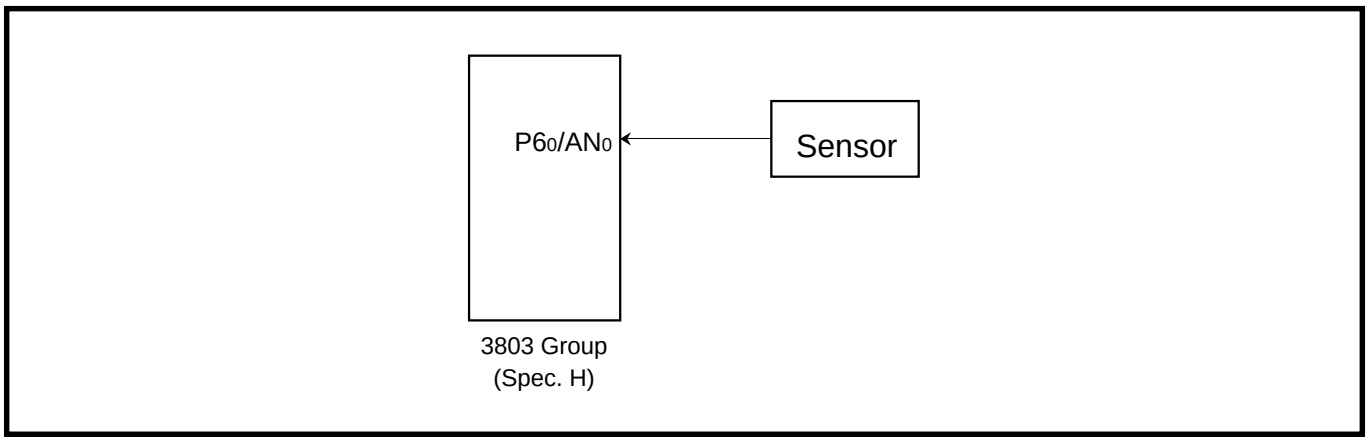


Fig. 2.6.11 Connection diagram

Specifications : •The analog input voltage input from a sensor is converted to digital values.
•P60/AN0 pin is used as an analog input pin.
•8-bit A-D mode

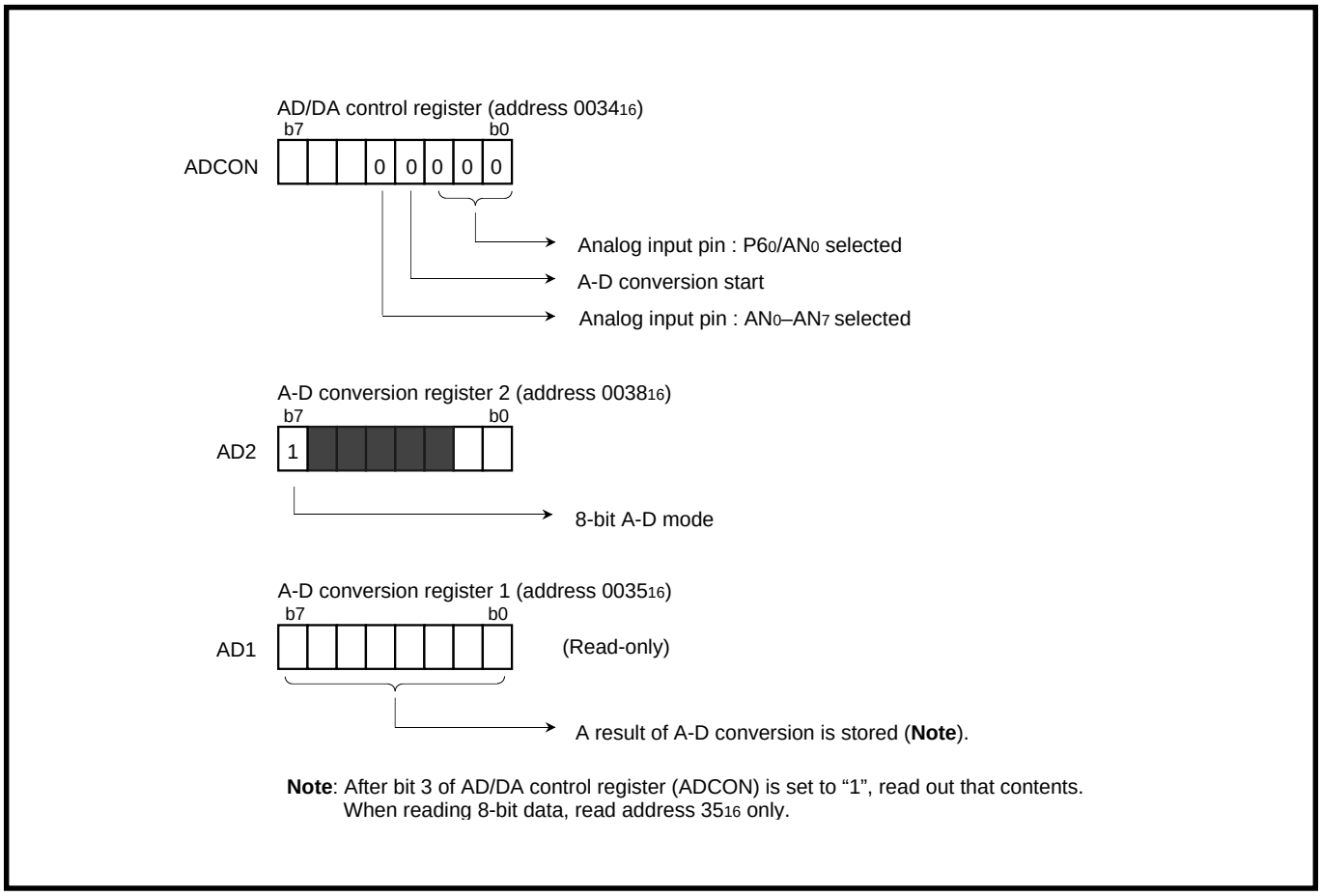


Fig. 2.6.12 Relevant registers setting

An analog input signal from a sensor is converted to the digital value according to the relevant registers setting shown by Figure 2.6.12. Figure 2.6.13 shows the control procedure for 8-bit A-D mode.

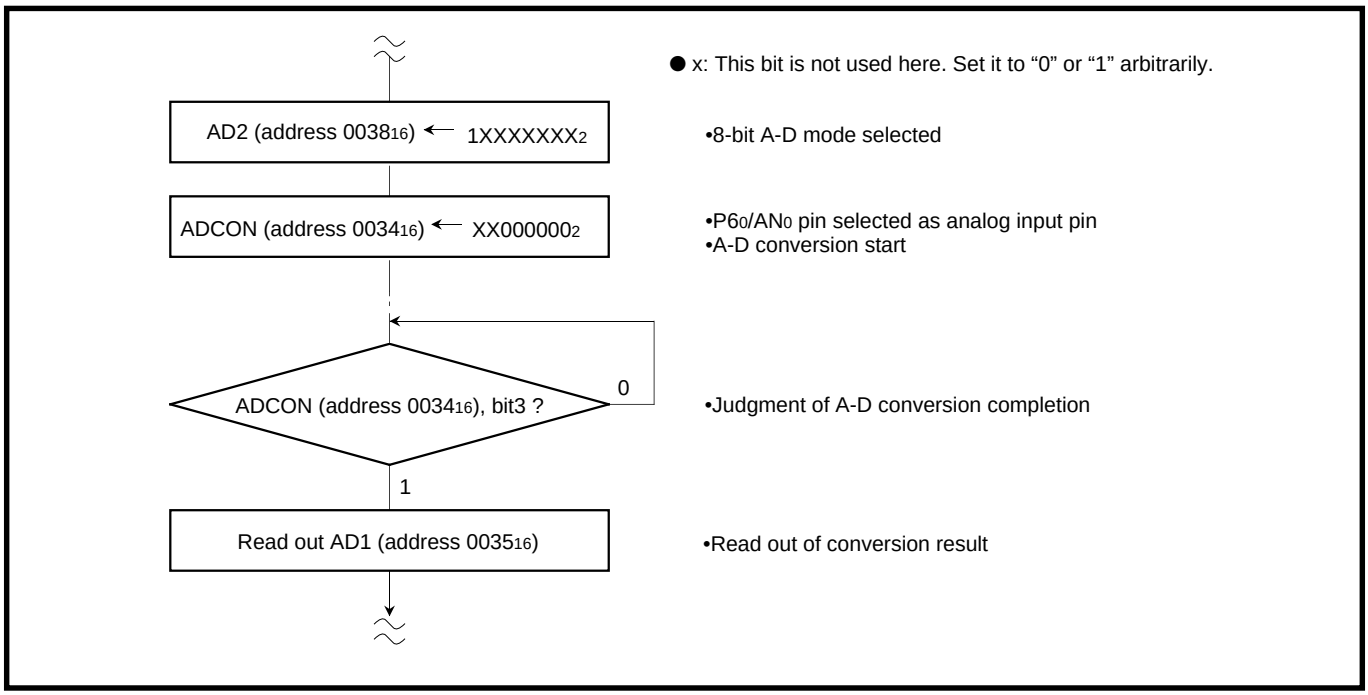


Fig. 2.6.13 Control procedure (8-bit A-D mode)

2.6.4 Notes on A-D converter

(1) Analog input pin

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 µF to 1 µF. Further, be sure to verify the operation of application products on the user side.

● **Reason**

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A-D conversion precision to be worse.

(2) A-D converter power source pin

The AVSS pin is A-D converter power source pins. Regardless of using the A-D conversion function or not, connect it as following :

• AVSS : Connect to the VSS line

● **Reason**

If the AVSS pin is opened, the microcomputer may have a failure because of noise or others.

(3) Clock frequency during A-D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. Thus, make sure the following during an A-D conversion.

• f(XIN) is 500 kHz or more

• Do not execute the **STP** instruction

(4) Difference between at 8-bit reading in 10-bit A-D mode and at 8-bit A-D mode

At 8-bit reading in the 10-bit A-D mode, “–1/2 LSB” correction is not performed to the A-D conversion result.

In the 8-bit A-D mode, the A-D conversion characteristics is the same as 3802 group’s characteristics because “–1/2 LSB” correction is performed.

2.7 D-A Converter

This paragraph explains the registers setting method and the notes relevant to the D-A converter.

2.7.1 Memory map

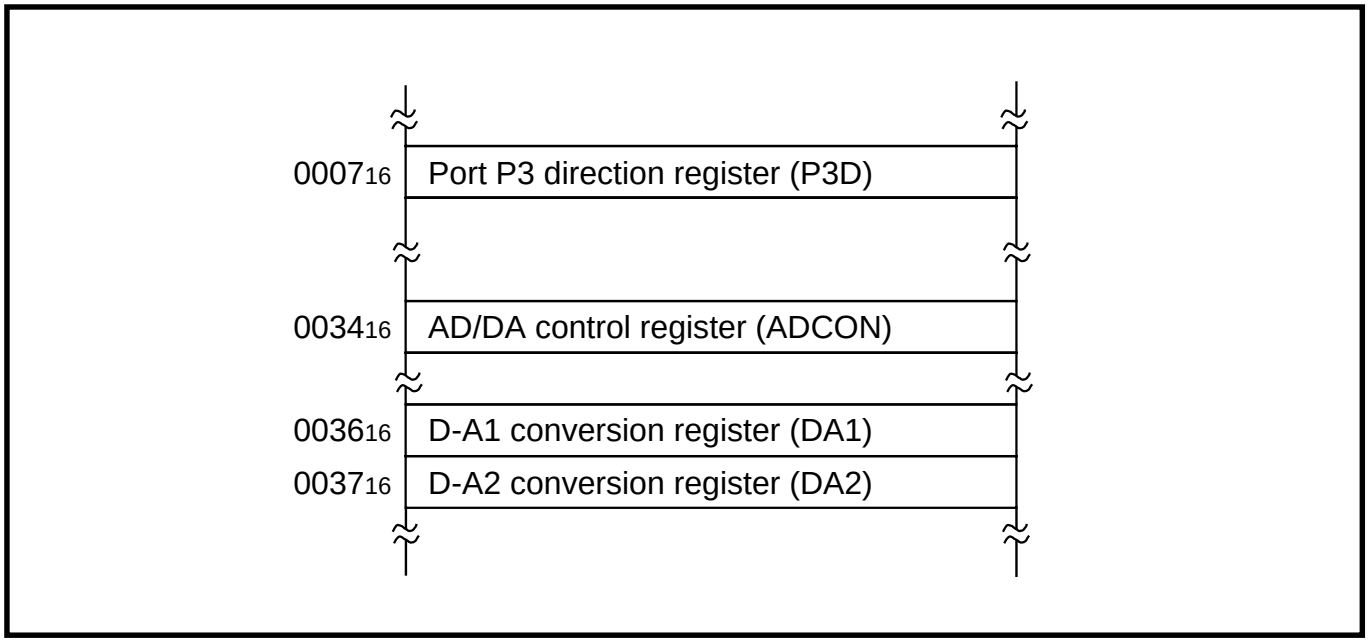


Fig. 2.7.1 Memory map of registers relevant to D-A converter

2.7.2 Relevant registers

Port P3 direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port P3 direction register
(P3D: address 0007_{16})

b	Name	Functions	At reset	R	W
0	Port P3 direction register	0 : Port $P3_0$ input mode 1 : Port $P3_0$ output mode	0	×	○
1		0 : Port $P3_1$ input mode 1 : Port $P3_1$ output mode	0	×	○
2		0 : Port $P3_2$ input mode 1 : Port $P3_2$ output mode	0	×	○
3		0 : Port $P3_3$ input mode 1 : Port $P3_3$ output mode	0	×	○
4		0 : Port $P3_4$ input mode 1 : Port $P3_4$ output mode	0	×	○
5		0 : Port $P3_5$ input mode 1 : Port $P3_5$ output mode	0	×	○
6		0 : Port $P3_6$ input mode 1 : Port $P3_6$ output mode	0	×	○
7		0 : Port $P3_7$ input mode 1 : Port $P3_7$ output mode	0	×	○

Fig. 2.7.2 Structure of Port P5 direction register

AD/DA control register

b7 b6 b5 b4 b3 b2 b1 b0

AD/DA control register
(ADCON: address 0034_{16})

b	Name	Functions	At reset	R	W
0	Analog input pin selection bits 1	b2 b1 b0 0 0 0: $P6_0/AN_0$ or $P0_0/AN_8$ 0 0 1: $P6_1/AN_1$ or $P0_1/AN_9$ 0 1 0: $P6_2/AN_2$ or $P0_2/AN_{10}$ 0 1 1: $P6_3/AN_3$ or $P0_3/AN_{11}$ 1 0 0: $P6_4/AN_4$ or $P0_4/AN_{12}$ 1 0 1: $P6_5/AN_5$ or $P0_5/AN_{13}$ 1 1 0: $P6_6/AN_6$ or $P0_6/AN_{14}$ 1 1 1: $P6_7/AN_7$ or $P0_7/AN_{15}$	0	○	○
1			0	○	○
2			0	○	○
3	AD conversion completion bit	0: Conversion in progress 1: Conversion completed	1	○	○
4	Analog input pin selection bit 2	0: AN_0 to AN_7 side 1: AN_8 to AN_{15} side	0	○	○
5	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are “0”.		0	○	×
6	DA_1 output enable bit	0: DA_1 output disabled 1: DA_1 output enabled	0	○	○
7	DA_2 output enable bit	0: DA_2 output disabled 1: DA_2 output enabled	0	○	○

Fig. 2.7.3 Structure of AD/DA control register

D-Ai conversion register

b7 b6 b5 b4 b3 b2 b1 b0

D-Ai conversion register (i = 1, 2)
(DAi: addresses 0036_{16}, 0037_{16})

b	Functions	At reset	R	W
0	This is D-A output value stored bits. This is write exclusive register.	0	×	○
1		0	×	○
2		0	×	○
3		0	×	○
4		0	×	○
5		0	×	○
6		0	×	○
7		0	×	○

Fig. 2.7.4 Structure of D-Ai converter register

2.7.3 D-A converter application example

(1) Speaker output volume modulation

Outline: The volume of a speaker output is modulated by using D-A converter.

Specifications: •Timer X modulates the period of sound for the pitch interval, so that a fixed pitch ("la": approx. 440 Hz) can be output. Modulating the amplitude with the D-A output value controls the volume.
•Use f(X_{IN}) = 6 MHz.
•Use DA1 ($P3_0/DA_1$ pin) as D-A converter.

Figure 2.7.5 shows a peripheral circuit example and Figure 2.7.6 shows a speaker output example. Figure 2.7.7 shows the relevant registers setting.

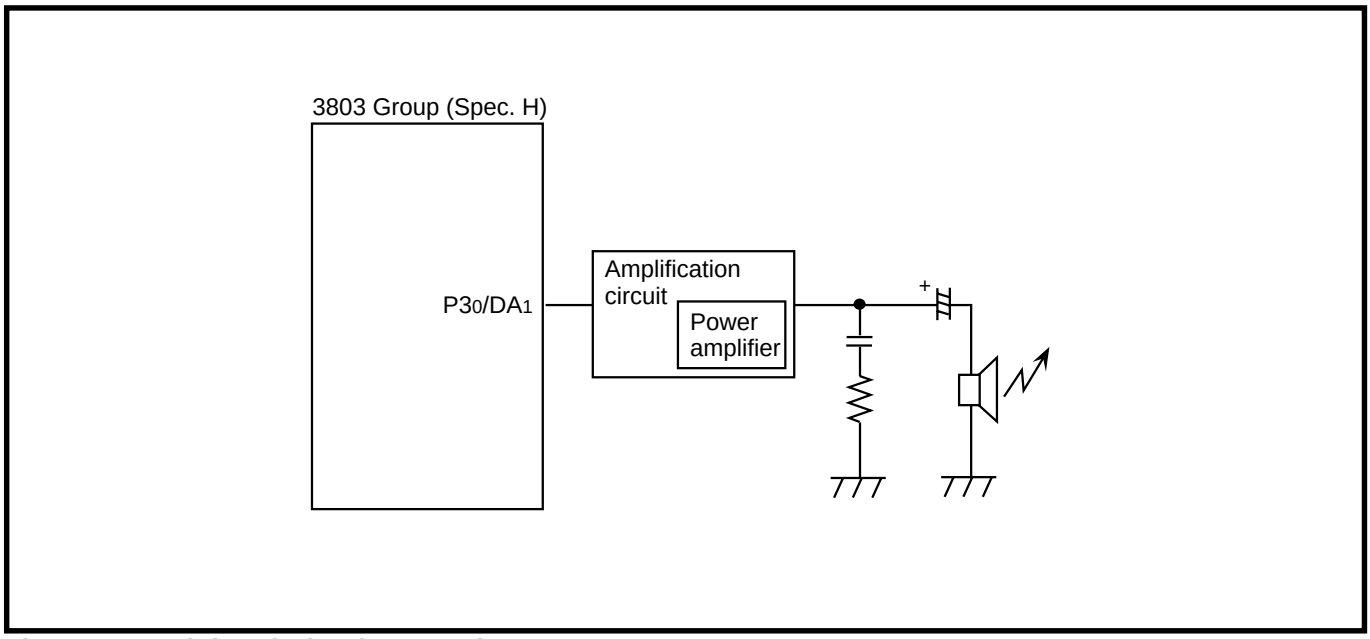


Fig. 2.7.5 Peripheral circuit example

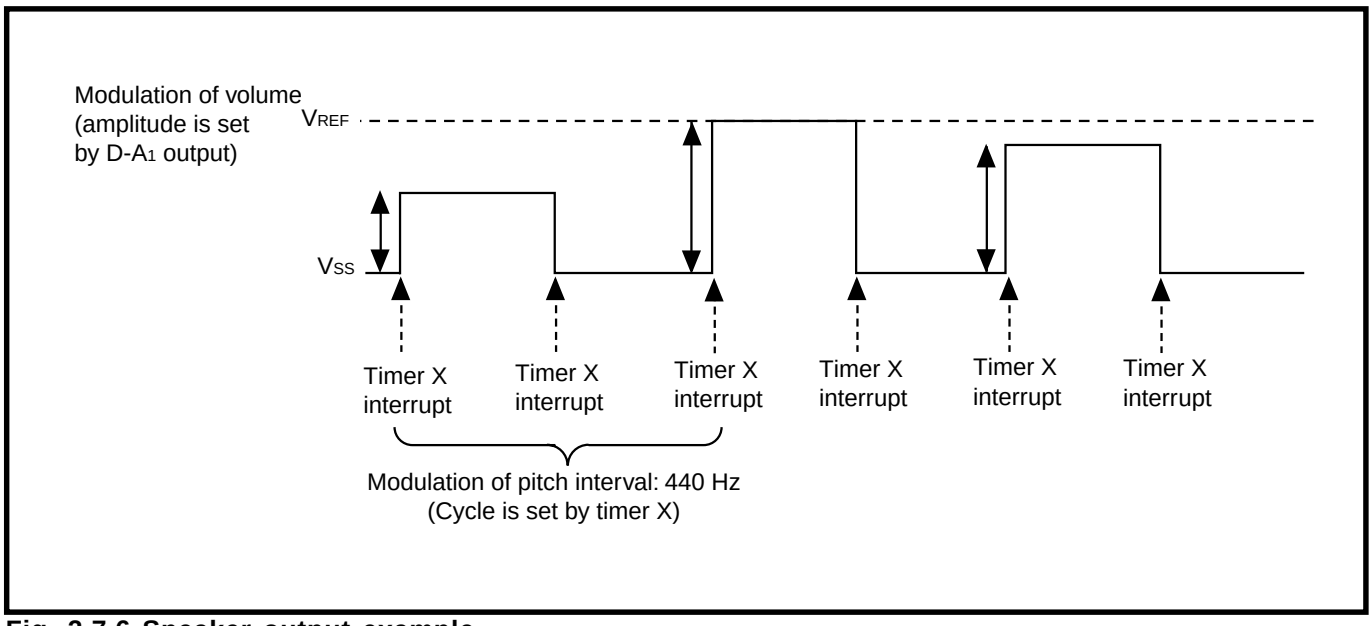


Fig. 2.7.6 Speaker output example

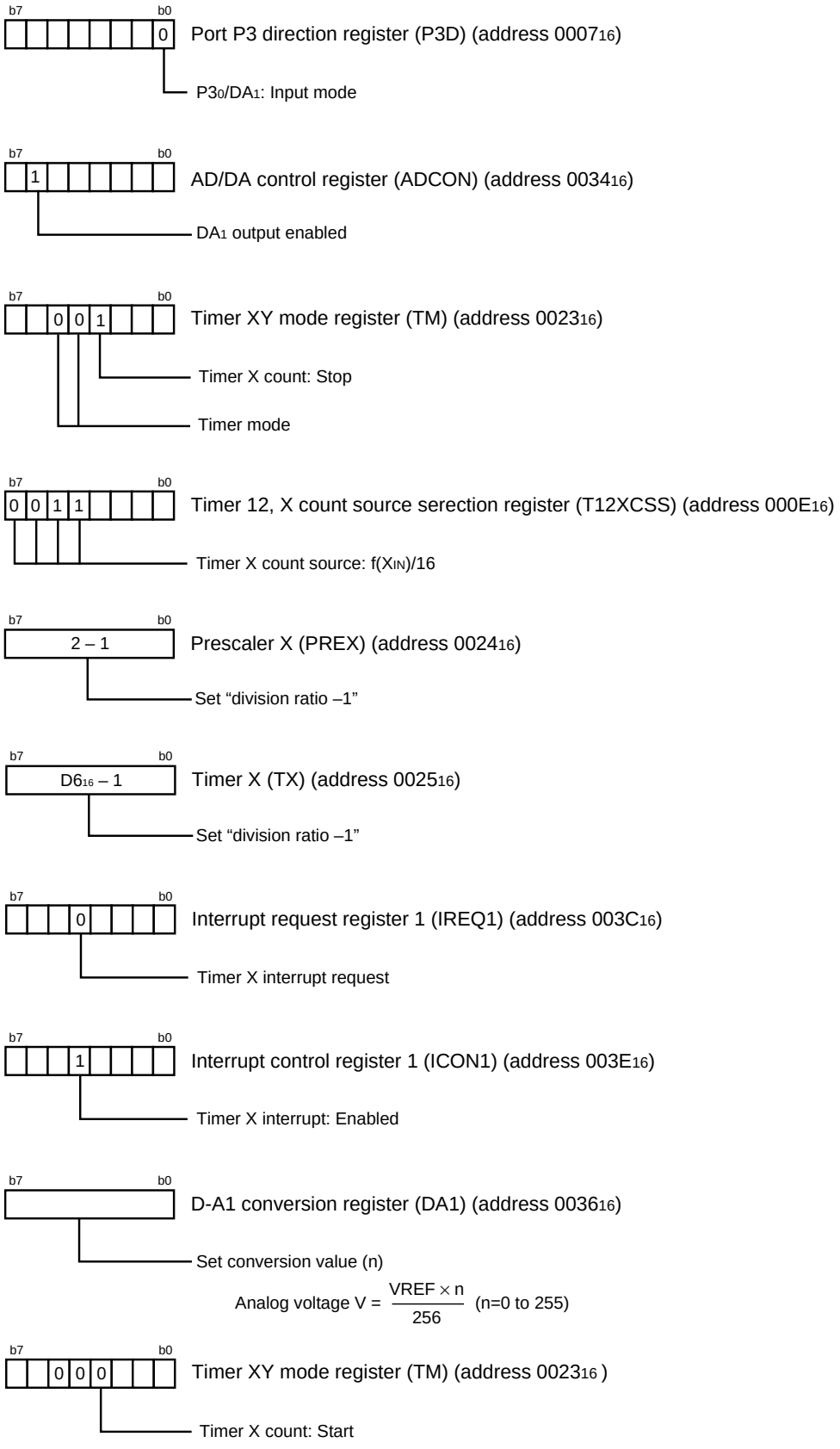


Fig. 2.7.7 Relevant registers setting

When the registers are set as shown in Figure 2.7.7, the speaker output volume is modulated by the D-A output value. Figure 2.7.8 shows the control procedure.

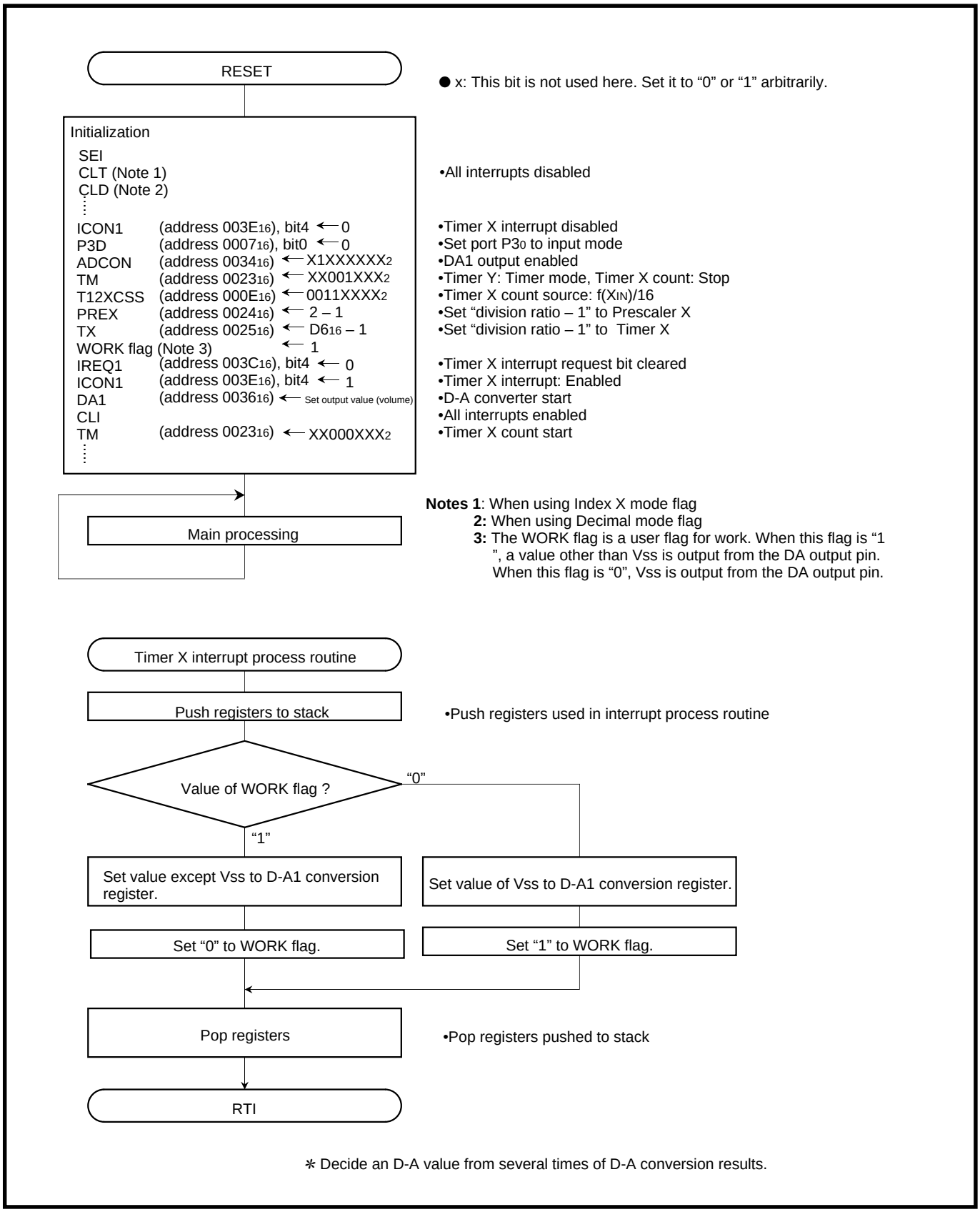


Fig. 2.7.8 Control procedure

2.7.4 Notes on D-A converter

(1) Vcc when using D-A converter

The D-A converter accuracy when Vcc is 4.0 V or less differs from that of when Vcc is 4.0 V or more. When using the D-A converter, we recommend using a Vcc of 4.0 V or more.

(2) D-Ai conversion register when not using D-A converter

When a D-A converter is not used, set all values of the D-Ai conversion registers (i = 1, 2) to "00_{16}". The initial value after reset is "00_{16}".

2.8 Watchdog timer

This paragraph explains the registers setting method and the notes relevant to the watchdog timer.

2.8.1 Memory map

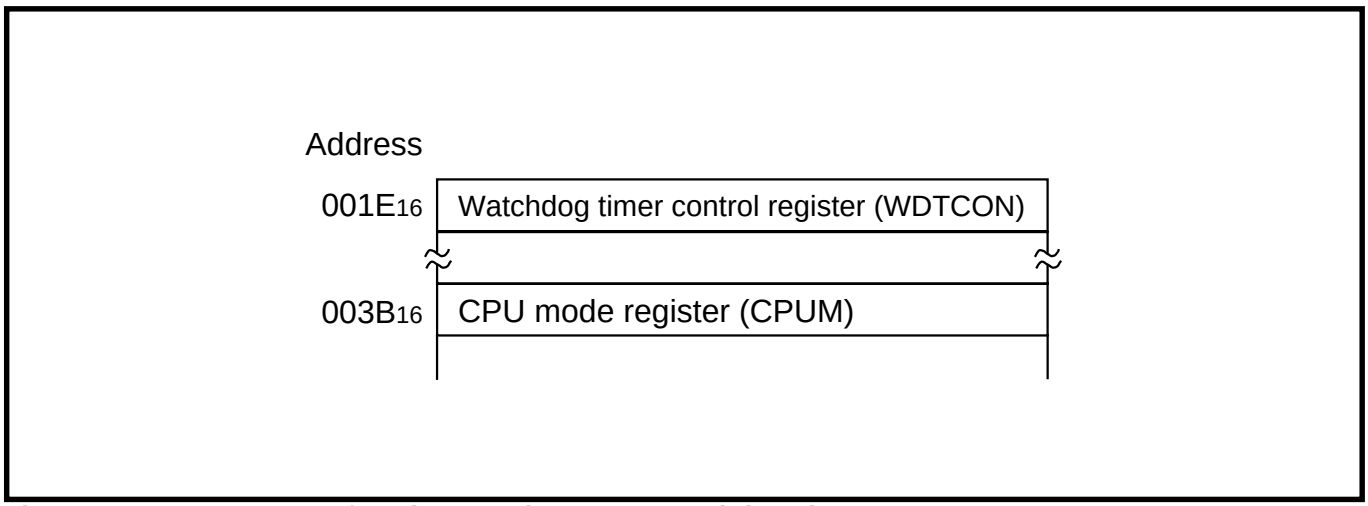


Fig. 2.8.1 Memory map of registers relevant to watchdog timer

2.8.2 Relevant registers

Watchdog timer control register

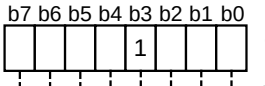
b7 b6 b5 b4 b3 b2 b1 b0

Watchdog timer control register
(WDTCON: address 001E16)

b	Name	Functions	At reset	R	W
0	Watchdog timer H (for read-out of high-order 6 bit)		1	○	×
1			1	○	×
2			1	○	×
3			1	○	×
4			1	○	×
5			1	○	×
6	STP instruction disable bit	0: STP instruction enabled 1: STP instruction disabled	0	○	○
7	Watchdog timer H count source selection bit	0: Watchdog timer L underflow 1: f(XIN)/16 or f(XCIN)/16	0	○	○

Fig. 2.8.2 Structure of Watchdog timer control register

CPU mode register



CPU mode register
(CPUM: address 003B16)

b	Name	Functions	At reset	R	W
0	Processor mode bits	b1 b0 00 : Single-chip mode 01 : 10 : } Not available 11 :	0	○	○
1			0	○	○
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	○	○
3	Fix this bit to “1”.		1	○	○
4	Port Xc switch bit	0: I/O port function (stop oscillating) 1: XCIN-XCOUT oscillation function	0	○	○
5	Main clock (XIN-XOUT) stop bit	0: Oscillating 1: Stopped	0	○	○
6	Main clock division ratio selection bits	b7 b6 0 0: ϕ=f(XIN)/2 (high-speed mode) 0 1: ϕ=f(XIN)/8 (middle-speed mode) 1 0: ϕ=f(XCIN)/2 (low-speed mode) 1 1: Not available	1	○	○
7			0	○	○

Fig. 2.8.3 Structure of CPU mode register

2.8.3 Watchdog timer application examples

(1) Detection of program runaway

Outline: If program runaway occurs, let the microcomputer reset, using the internal timer for detection of program runaway.

Specifications:
- High-speed mode is used as a main clock division ratio.
- An underflow signal of the watchdog timer L is supplied as the count source of watchdog timer H.
- 1 cycle of main routine is 65.536 ms or less.
- Before the watchdog timer H underflows, “0” is set into bit 7 of the watchdog timer control register at every cycle in a main routine.
- An underflow of watchdog timer H is judged to be program runaway, and the microcomputer is returned to the reset status.

Figure 2.8.4 shows a watchdog timer connection and division ratio setting; Figure 2.8.5 shows the relevant registers setting; Figure 2.8.6 shows the control procedure.

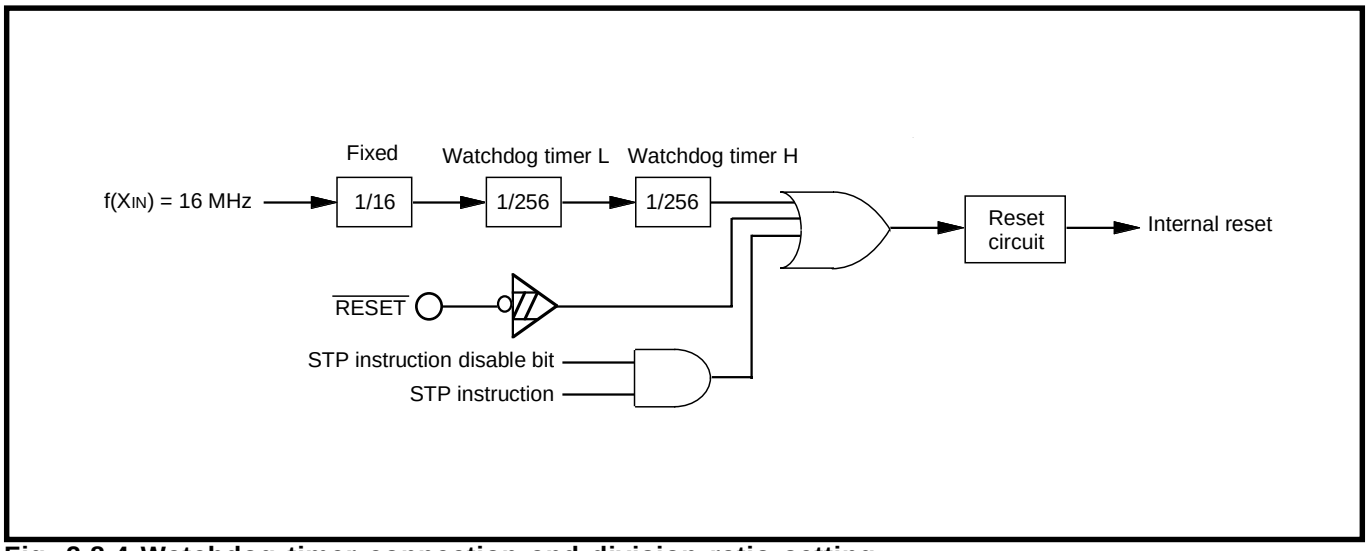


Fig. 2.8.4 Watchdog timer connection and division ratio setting

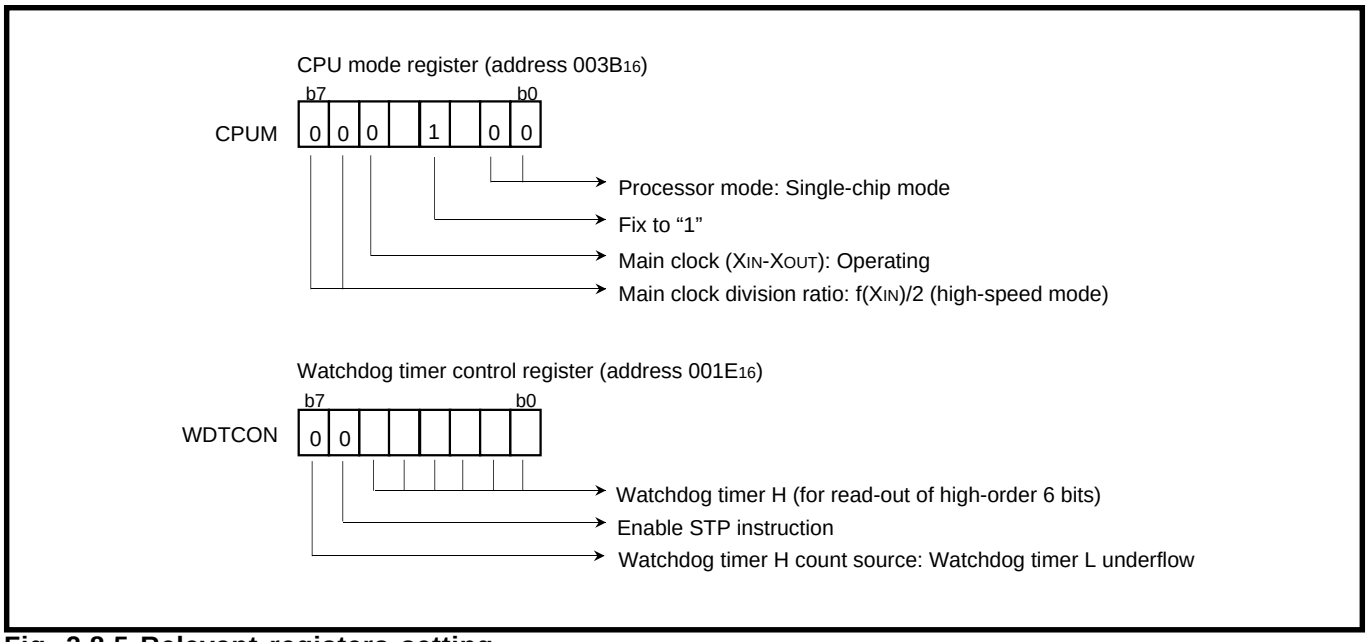


Fig. 2.8.5 Relevant registers setting

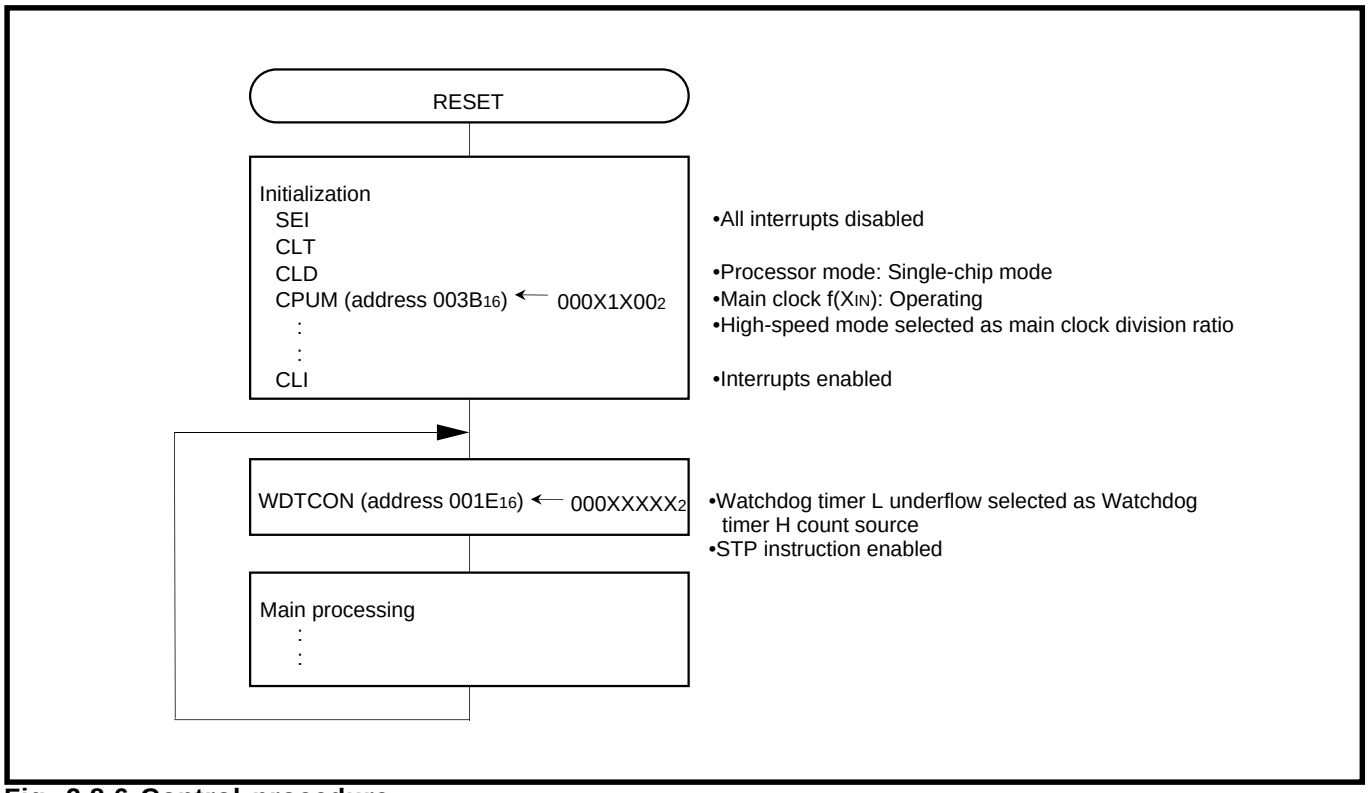


Fig. 2.8.6 Control procedure

2.8.4 Notes on watchdog timer

- Make sure that the watchdog timer H does not underflow while waiting Stop release, because the watchdog timer keeps counting during that term.
- When the STP instruction disable bit has been set to "1", it is impossible to switch it to "0" by a program.

2.9 Reset

2.9.1 Connection example of reset IC

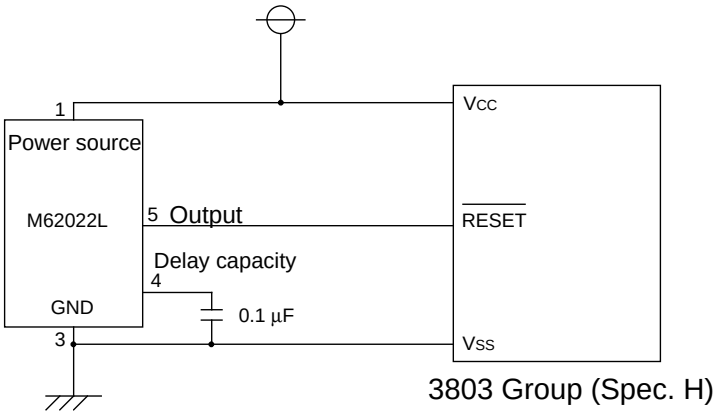


Fig. 2.9.1 Example of poweron reset circuit

Figure 2.9.2 shows the system example which switches to the RAM backup mode by detecting a drop of the system power source voltage with the INT interrupt.

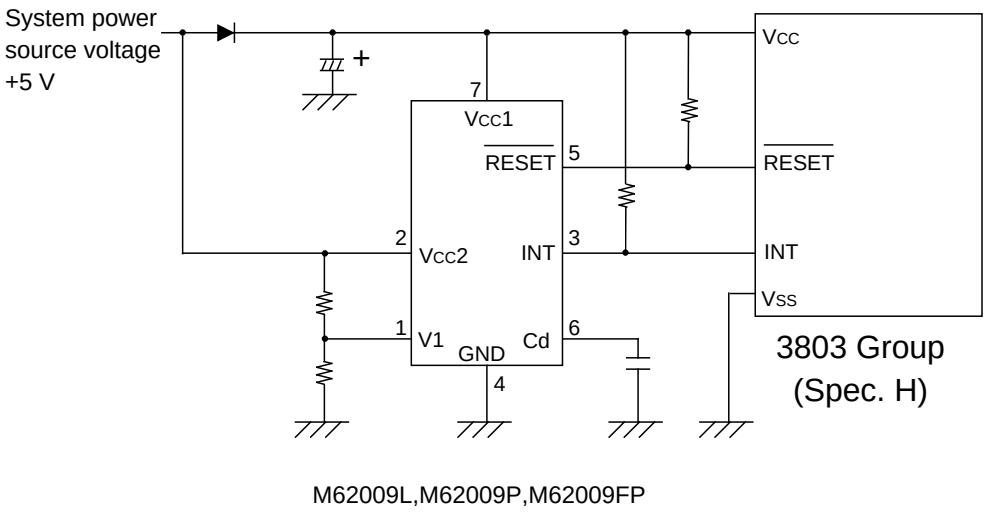


Fig. 2.9.2 RAM backup system

2.9.2 Notes on $\overline{\text{RESET}}$ pin

Connecting capacitor

In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the Vss pin. Use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

● **Reason**

If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

2.10 Clock generating circuit

This paragraph explains how to set the registers relevant to the clock generating circuit and describes an application example.

2.10.1 Relevant registers

CPU mode register

b7 b6 b5 b4 b3 b2 b1 b0

1

CPU mode register
(CPUM: address 003B16)

b	Name	Functions	At reset	R	W
0	Processor mode bits	b1 b0 00 : Single-chip mode 01 : Not available 10 : Not available 11 : Not available	0	○	○
1			0	○	○
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	○	○
3	Fix this bit to “1”.		1	○	○
4	Port Xc switch bit	0: I/O port function (oscillation stopped) 1: XCIN-XCOUT oscillation function	0	○	○
5	Main clock (XIN-XOUT) stop bit	0: Oscillating 1: Stopped	0	○	○
6	Main clock division ratio selection bits	b7 b6 0 0: ϕ=f(XIN)/2 (high-speed mode) 0 1: ϕ=f(XIN)/8 (middle-speed mode) 1 0: ϕ=f(XCIN)/2 (low-speed mode) 1 1: Not available	1	○	○
7			0	○	○

Fig. 2.10.1 Structure of CPU mode register

2.10.2 Clock generating circuit application example

(1) Status transition during power failure

Outline: The clock counts up every second by using the timer interrupt during a power failure.

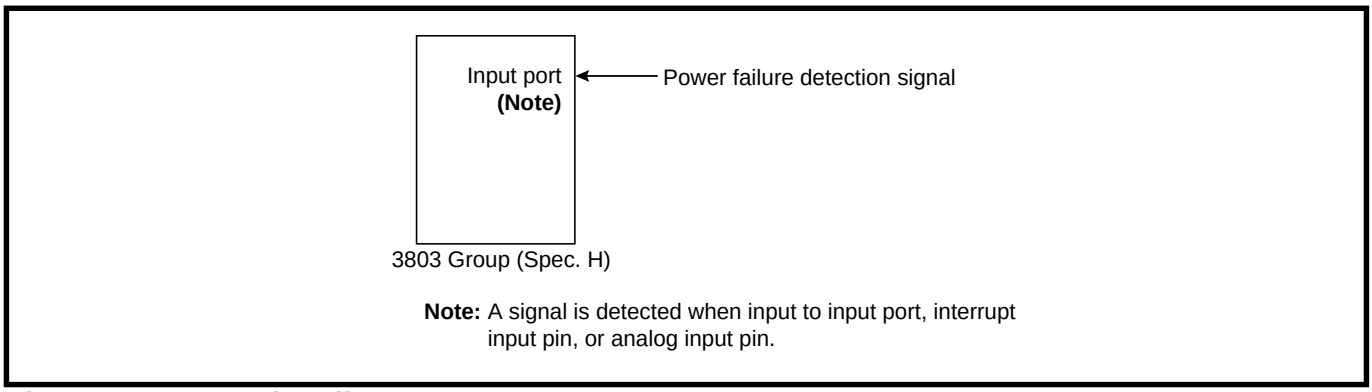


Fig. 2.10.2 Connection diagram

Specifications: •Reducing power dissipation as low as possible while maintaining clock function
•Clock: f(X_{IN}) = 8 MHz, f(X_{CIN}) = 32.768 kHz
•Port processing
Input port: Fixed to “H” or “L” level externally.
Output port: Fixed to output level that does not cause current flow to the external.
(Example) Fix to “H” for an LED circuit that turns on at “L” output level.
I/O port: Input port → Fixed to “H” or “L” level externally.
Output port → Output of data that does not consume current
V_{REF} pin: Terminate A-D conversion operation
Stop V_{REF} current dissipation by setting value of D-Ai conversion register to “00_{16}”.

Figure 2.10.3 shows the status transition diagram during power failure and Figure 2.10.4 shows the setting of relevant registers.

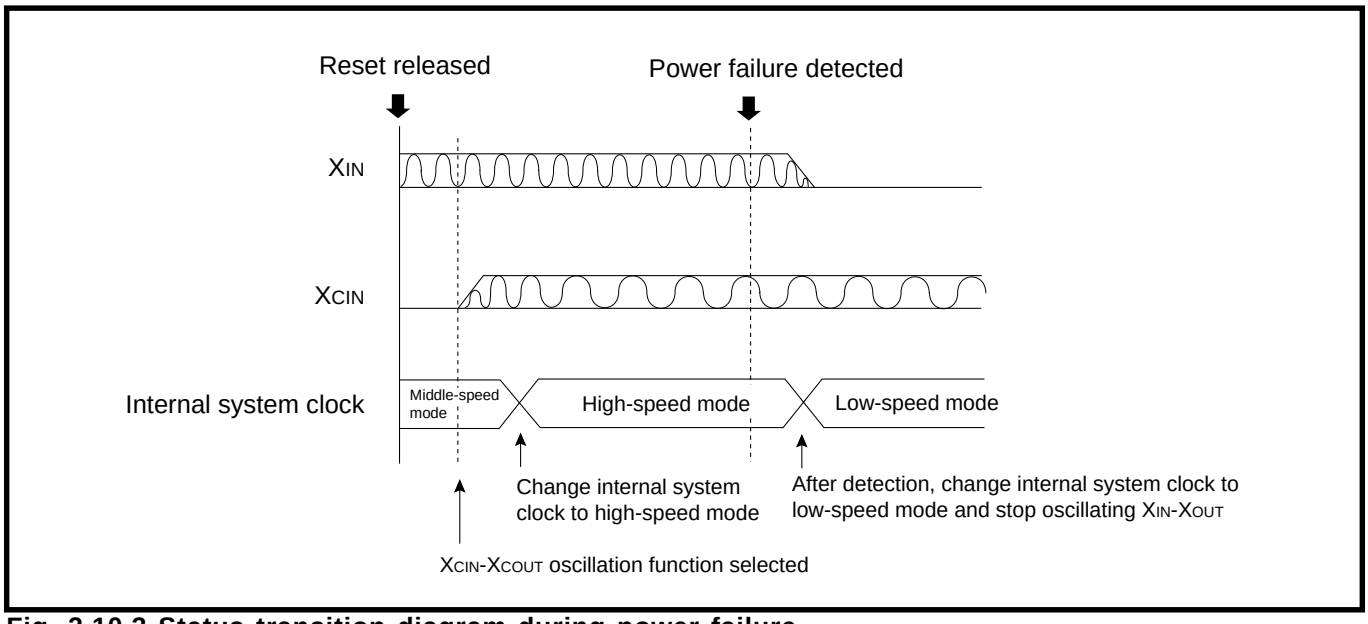


Fig. 2.10.3 Status transition diagram during power failure

Notes 1: This setting is necessary only when selecting the high-speed mode.
2: When selecting the middle-speed mode, bit 6 is “1”.

Fig. 2.10.4 Setting of relevant registers

Control procedure: To prepare for a power failure, set the relevant registers in the order shown below.

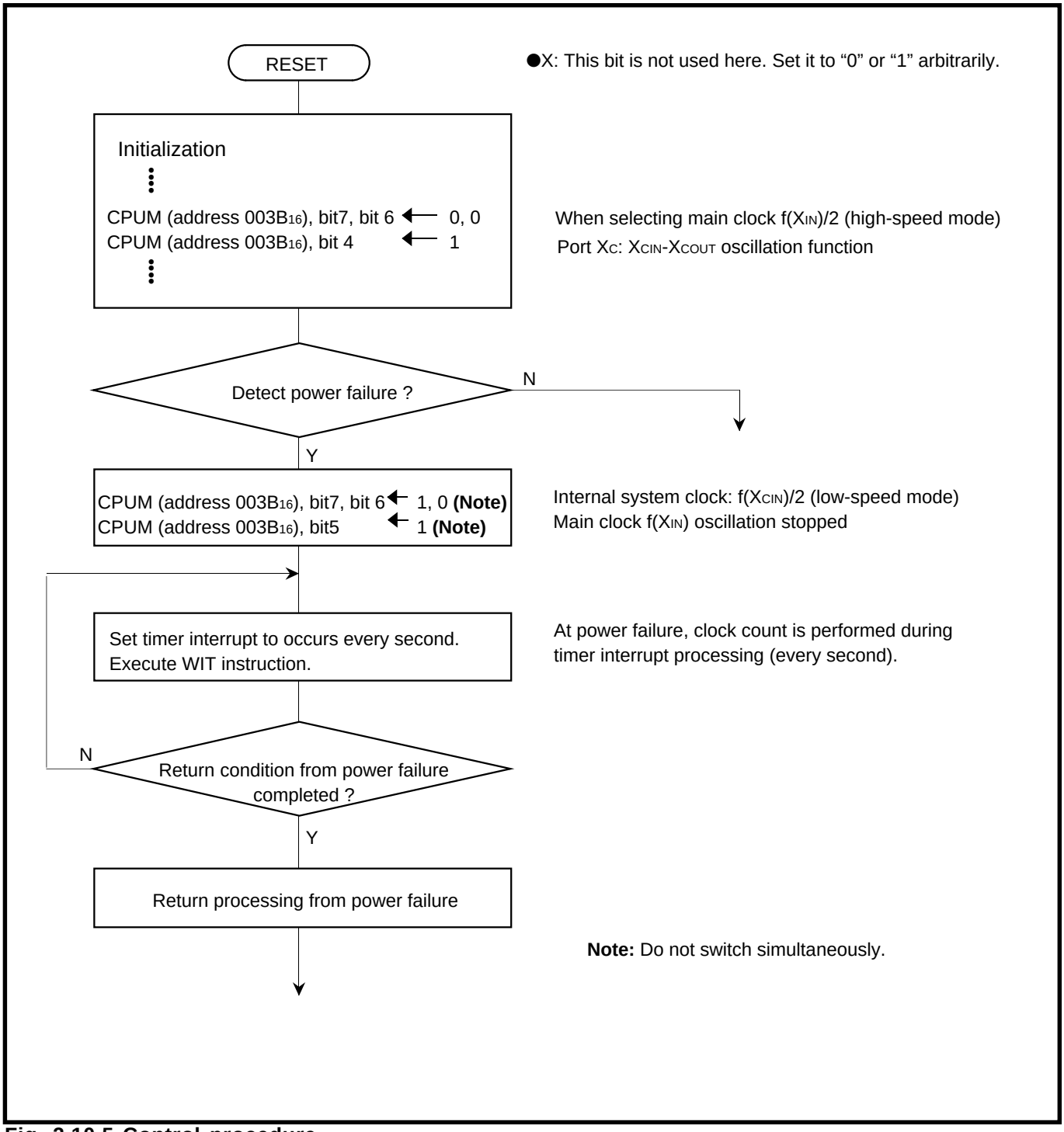


Fig. 2.10.5 Control procedure

2.11 Standby function

The 3803 group (Spec. H) is provided with standby functions to stop the CPU by software and put the CPU into the low-power operation.
The following two types of standby functions are available.
•Stop mode using STP instruction
•Wait mode using WIT instruction

2.11.1 Stop mode

The stop mode is set by executing the STP instruction. In the stop mode, the oscillation of both clocks (X_{IN}–X_{OUT}, X_{CIN}–X_{COUT}) stop and the internal clock ϕ stops at the “H” level. The CPU stops and peripheral units stop operating. As a result, power dissipation is reduced.

(1) State in stop mode

Table 2.11.1 shows the state in the stop mode.

Table 2.11.1 State in stop mode

Item	State in stop mode
Oscillation	Stopped.
CPU	Stopped.
Internal clock ϕ	Stopped at “H” level.
I/O ports P0–P6	Retains the state at the STP instruction execution.
Timer	Stopped. (Timers 1, 2, X, Y, Z) However, Timers X, Y, Z can be operated in the event counter mode.
PWM	Stopped.
Watchdog timer	Stopped.
Serial I/O1, Serial I/O2, Serial I/O3	Stopped. However, these can be operated only when an external clock is selected.
A-D converter	Stopped.
D-A converter	Retains output voltage.

(2) Release of stop mode

The stop mode is released by a reset input or by the occurrence of an interrupt request. Note the differences in the restoration process according to reset input or interrupt request, as described below.

■Restoration by reset input

The stop mode is released by holding the $\overline{\text{RESET}}$ pin to the "L" input level during the stop mode. Oscillation is started when all ports are in the input state and the stop mode of the main clock (X_{IN}-X_{OUT}) is released.

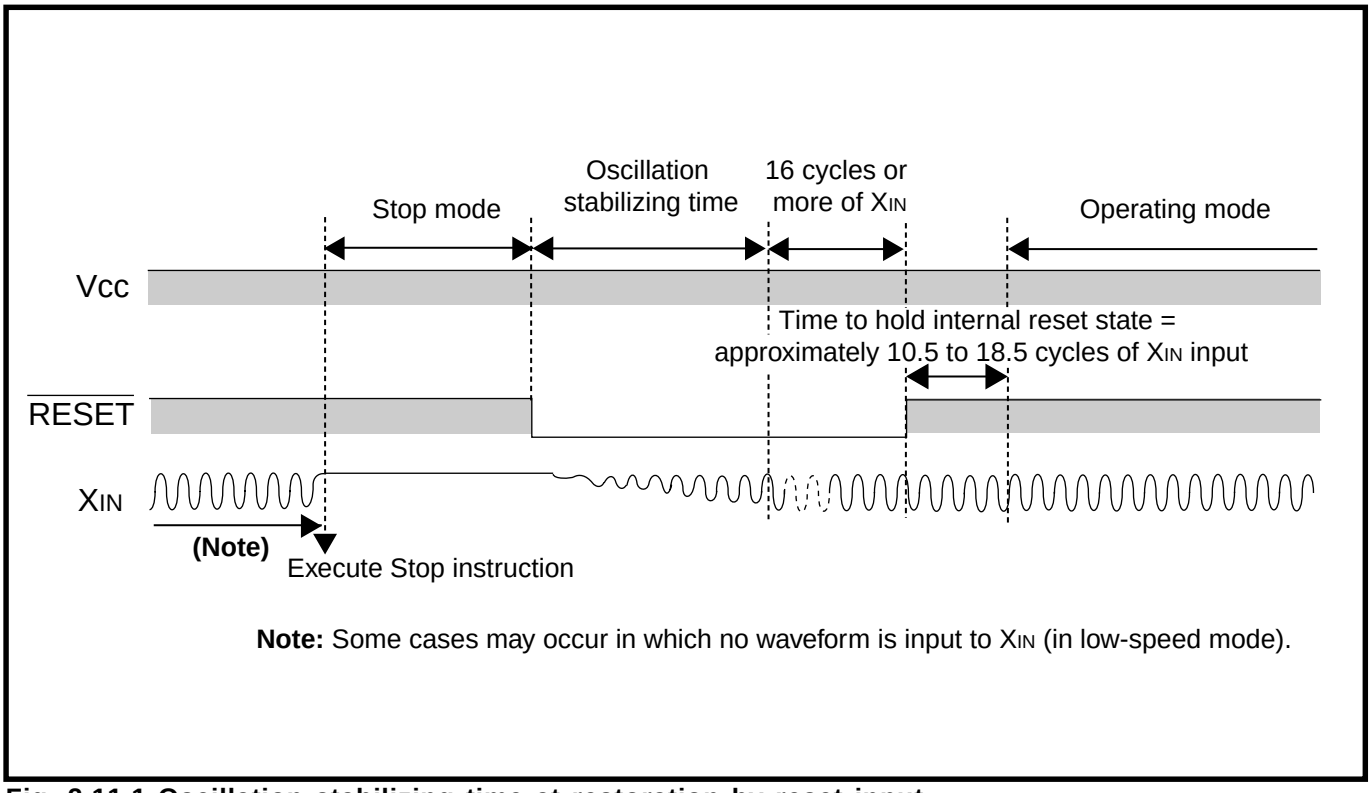
Oscillation is unstable when restarted. For this reason, time for stabilizing of oscillation (oscillation stabilizing time) is required. The input of the $\overline{\text{RESET}}$ pin should be held at the "L" level until oscillation stabilizes.

When the $\overline{\text{RESET}}$ pin is held at the "L" level for 16 cycles or more of X_{IN} after the oscillation has stabilized, the microcomputer will go to the reset state. After the input level of the $\overline{\text{RESET}}$ pin is returned to "H", the reset state is released in approximately 10.5 to 18.5 cycles of the X_{IN} input.

Figure 2.11.1 shows the oscillation stabilizing time at restoration by reset input.

At release of the stop mode by reset input, the internal RAM retains its contents previous to the reset. However, the previous contents of the CPU register and SFR are not retained.

For more details concerning reset, refer to "2.9 Reset".



Note: Some cases may occur in which no waveform is input to X_{IN} (in low-speed mode).

Fig. 2.11.1 Oscillation stabilizing time at restoration by reset input

■Restoration by interrupt request

The occurrence of an interrupt request in the stop mode releases the stop mode. As a result, oscillation is resumed. The interrupts available for restoration are:

•INT_0–INT_4
•$CNTR_0$, $CNTR_1$, $CNTR_2$
•Serial I/O (1, 2, 3) using an external clock
•Timer X, Y, Z using an external event count

However, when using any of these interrupt requests for restoration from the stop mode, in order to enable the selected interrupt, you must execute the STP instruction after setting the following conditions.

[Necessary register setting]

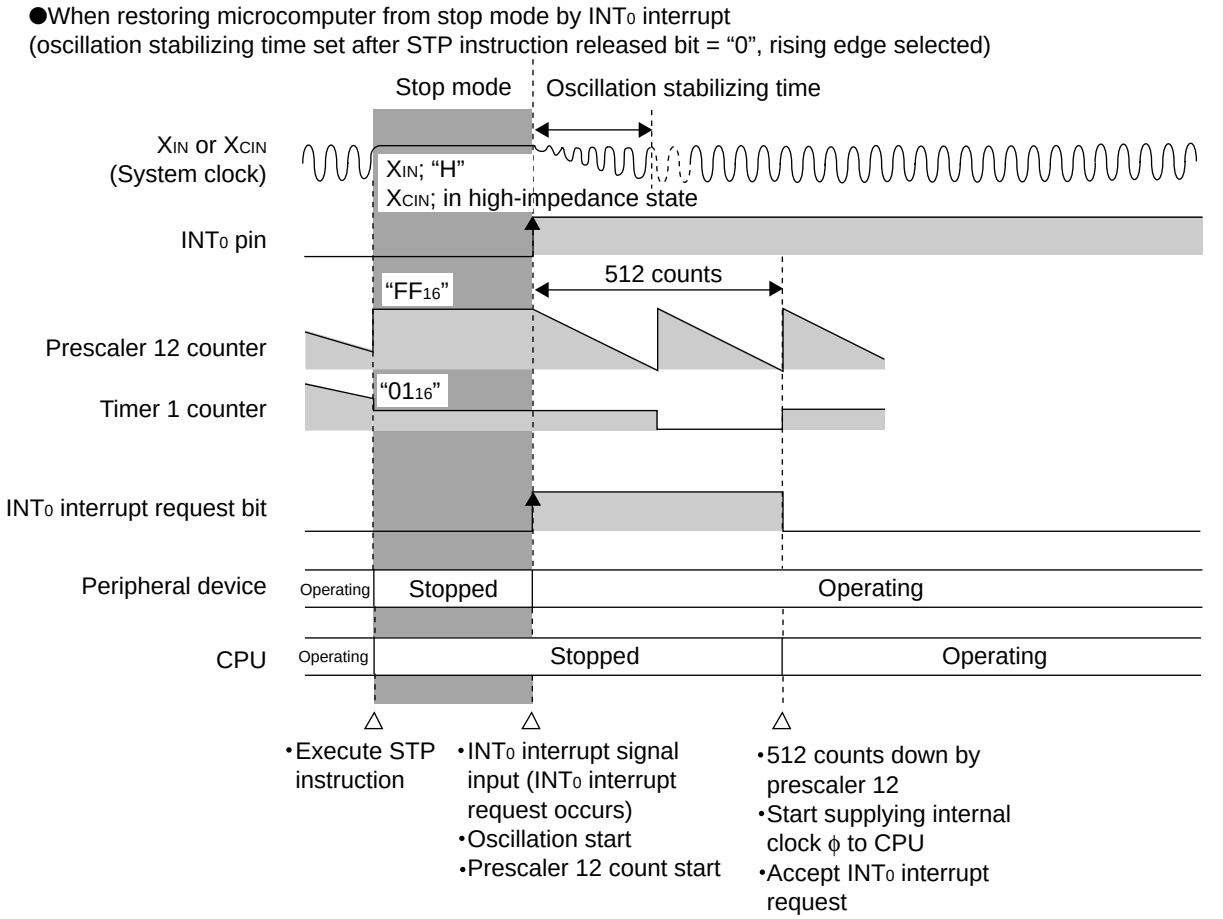
① Interrupt disable flag I = “0” (interrupt enabled)
② Timer 1 interrupt enable bit = “0” (interrupt disabled)
③ Interrupt request bit of interrupt source to be used for restoration = “0” (no interrupt request issued)
④ Interrupt enable bit of interrupt source to be used for restoration = “1” (interrupts enabled)

For more details concerning interrupts, refer to “2.2 Interrupts”.

Oscillation is unstable when restarted. For this reason, time for stabilizing of oscillation (oscillation stabilizing time) is required. For restoration by an interrupt request, waiting time prior to supplying internal clock ϕ to the CPU is automatically generated*2 by Prescaler 12 and Timer 1*1. This waiting time is reserved as the oscillation stabilizing time on the system clock side. The supply of internal clock ϕ to the CPU is started at the Timer 1 underflow.

Figure 2.11.2 shows an execution sequence example at restoration by the occurrence of an INT_0 interrupt request.

✻1: If the STP instruction is executed when the oscillation stabilizing time set after STP instruction released bit is “0”, “FF_{16}” and “01_{16}” are automatically set in the Prescaler 12 counter/latch and Timer 1 counter/latch, respectively. When the oscillation stabilizing time set after STP instruction released bit is “1”, nothing is automatically set to either Prescaler 12 or Timer 1. For this reason, any suitable value can be set to Prescaler 12 and Timer 1 for the oscillation stabilizing time.
✻2: Immediately after the oscillation is started, the count source is supplied to the prescaler 12 so that a count operation is started.



Note: The count source set at STP instruction execution is connected as the prescaler 12 count source.

Fig. 2.11.2 Execution sequence example at restoration by occurrence of INT0 interrupt request

(3) Notes on using stop mode

■Register setting

Since values of the prescaler 12 and Timer 1 are automatically reloaded when returning from the stop mode, set them again, respectively. (When the oscillation stabilizing time set after STP instruction released bit is "0")

■Clock restoration

After restoration from the stop mode to the normal mode by an interrupt request, the contents of the CPU mode register previous to the STP instruction execution are retained. Accordingly, if both main clock and sub clock were oscillating before execution of the STP instruction, the oscillation of both clocks is resumed at restoration.

In the above case, when the main clock side is set as a system clock, the oscillation stabilizing time until the timer 1 underflow is reserved at restoration from the stop mode.

When the oscillation stabilizing time set after STP instruction released bit is "0", the time for 512 counts of the count source become the oscillation stabilizing time. When the oscillation stabilizing time set after STP instruction released bit is "1", an arbitrarily count value set to the prescaler 12 and the timer 1 become the oscillation stabilizing time.

At this time, note that the oscillation on the sub clock side may not be stabilized even after the lapse of the oscillation stabilizing time of the main clock side.

2.11.2 Wait mode

The wait mode is set by execution of the WIT instruction. In the wait mode, oscillation continues, but the internal clock ϕ stops at the “H” level.
The CPU stops, but most of the peripheral units continue operating.

(1) State in wait mode

The continuation of oscillation permits clock supply to the peripheral units. Table 2.11.2 shows the state in the wait mode.

Table 2.11.2 State in wait mode

Item	State in wait mode
Oscillation	Operating.
CPU	Stopped.
Internal clock ϕ	Stopped at “H” level.
I/O ports P0–P6	Retains the state at the WIT instruction execution.
Timer	Operating.
PWM	Operating.
Watchdog timer	Operating.
Serial I/O1, Serial I/O2, Serial I/O3	Operating.
A-D converter	Operating.
D-A converter	Retains output voltage.

(2) Release of wait mode

The wait mode is released by reset input or by the occurrence of an interrupt request. Note the differences in the restoration process according to reset input or interrupt request, as described below.

In the wait mode, oscillation is continued, so an instruction can be executed immediately after the wait mode is released.

■Restoration by reset input

The wait mode is released by holding the input level of the $\overline{\text{RESET}}$ pin at “L” in the wait mode. Upon release of the wait mode, all ports are in the input state, and supply of the internal clock ϕ to the CPU is started. To reset the microcomputer, the $\overline{\text{RESET}}$ pin should be held at an “L” level for 16 cycles or more of X_{IN}. The reset state is released in approximately 10.5 cycles to 18.5 cycles of the X_{IN} input after the input of the $\overline{\text{RESET}}$ pin is returned to the “H” level.

At release of wait mode, the internal RAM retains its contents previous to the reset. However, the previous contents of the CPU register and SFR are not retained.

Figure 2.11.3 shows the reset input time.

For more details concerning reset, refer to “2.9 Reset”.

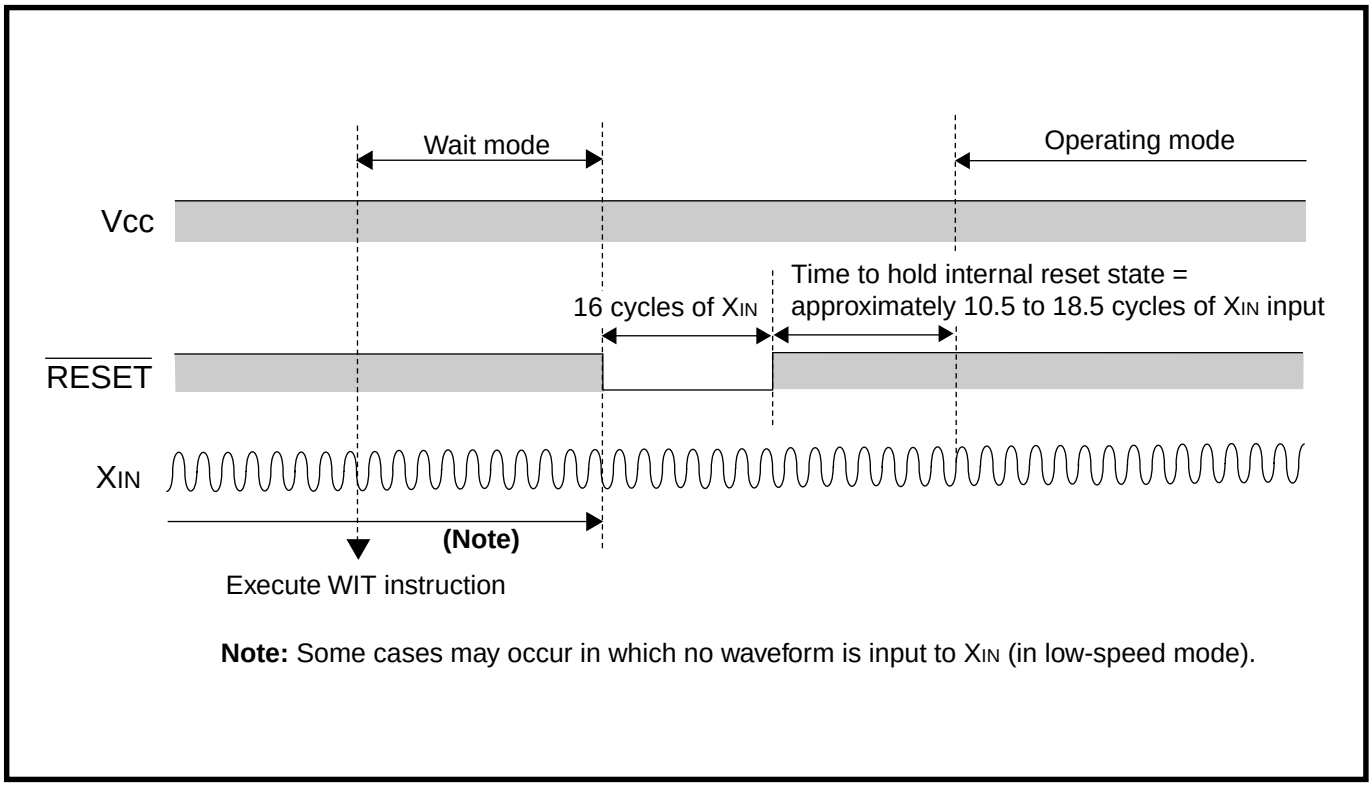


Fig. 2.11.3 Reset input time

■Restoration by interrupt request

In the wait mode, the occurrence of an interrupt request releases the wait mode and supply of the internal clock ϕ to the CPU is started. At the same time, the interrupt request used for restoration is accepted, so the interrupt processing routine is executed.

However, when using an interrupt request for restoration from the wait mode, in order to enable the selected interrupt, you must execute the STP instruction after setting the following conditions.

[Necessary register setting]

① Interrupt disable flag I = “0” (interrupt enabled)

② Interrupt request bit of interrupt source to be used for restoration = “0” (no interrupt request issued)

③ Interrupt enable bit of interrupt source to be used for restoration = “1” (interrupts enabled)

For more details concerning interrupts, refer to “2.2 Interrupts”.

(3) Notes on wait mode

■Clock restoration

If the wait mode is released by a reset when X_{CIN} is set as the system clock and X_{IN} oscillation is stopped during execution of the WIT instruction, X_{CIN} oscillation stops, X_{IN} oscillations starts, and X_{IN} is set as the system clock.

In the above case, the $\overline{\text{RESET}}$ pin should be held at “L” until the oscillation is stabilized.

2.12 Flash memory mode

This paragraph explains the registers setting method and the notes relevant to the flash memory mode of M38039FFHSP/FP/HP/KP.

2.12.1 Overview

The functions of the flash memory version are similar to those of the mask ROM version except that the flash memory is built-in and some of the SFR area differ from that of the mask ROM version (refer to "2.12.2 Memory map").

In the flash memory version, the built-in flash memory can be programmed or erased by using the following three modes.

- CPU rewrite mode
- Parallel I/O mode
- Standard serial I/O mode

2.12.2 Memory map

M38039FFHSP/FP/HP/KP have 60 Kbytes of built-in flash memory.

Figure 2.12.1 shows the memory map of the flash memory version.

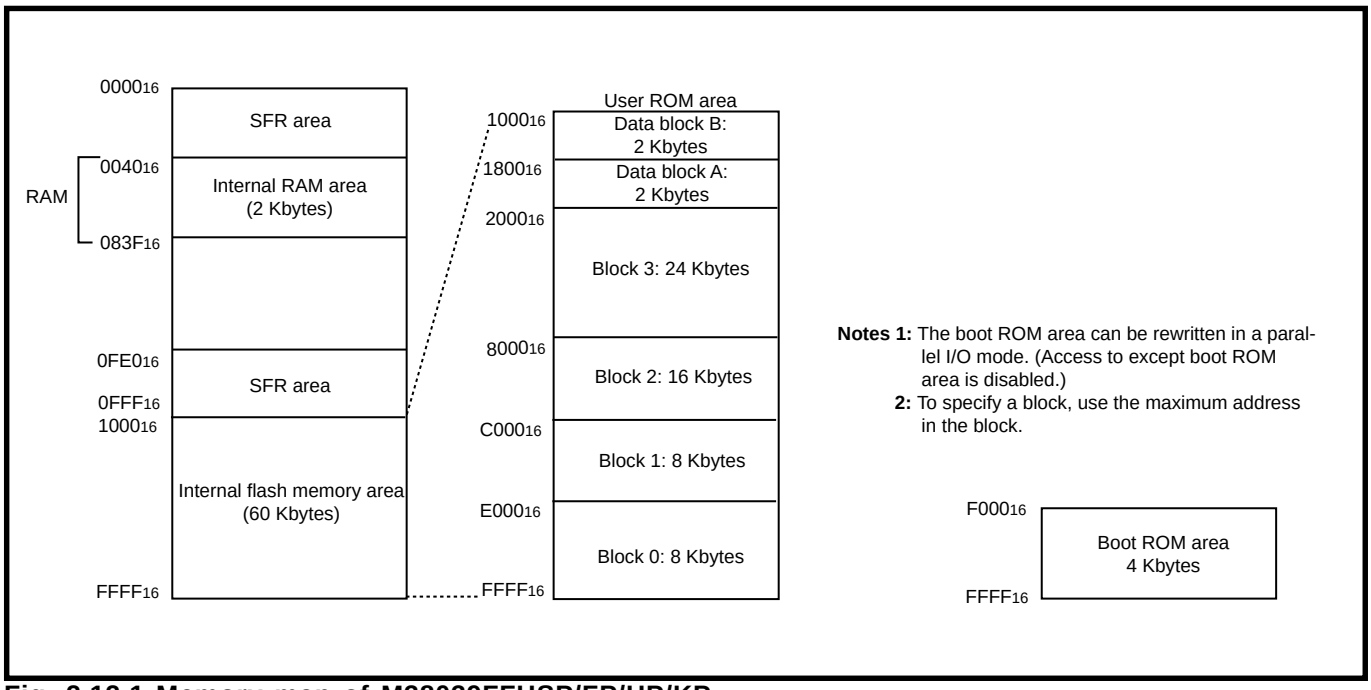


Fig. 2.12.1 Memory map of M38039FFHSP/FP/HP/KP

2.12.3 Relevant registers

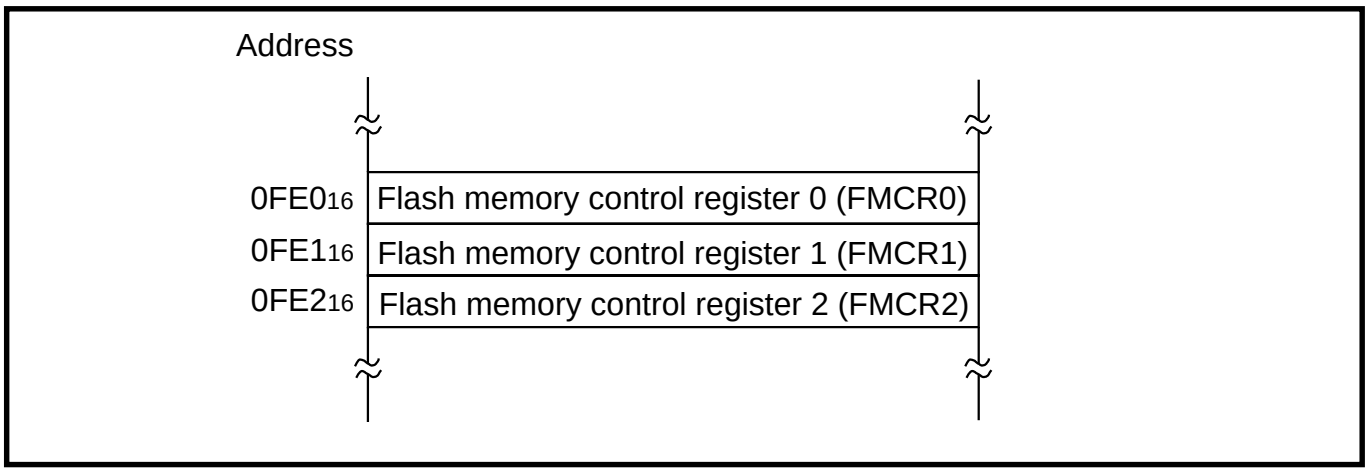


Fig. 2.12.2 Memory map of registers relevant to flash memory

Flash memory control register 0

b7 b6 b5 b4 b3 b2 b1 b0

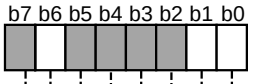
Flash memory control register 0
(FMCR0 : address 0FE016)

b	Name	Functions	At reset	R	W
0	RY/$\overline{BY}$ status flag	0 : Busy (being automatic written or automatic erased) 1 : Ready	1	○	×
1	CPU rewrite mode select bit **(Note 1)**	0 : CPU rewrite mode invalid (software commandes invalid) 1 : CPU rewrite mode valid (Software commands acceptable)	0	○	○
2	8 KB user block E/W enable bit **(Notes 1, 2)**	0: E/W disabled 1: E/W enabled	0	○	○
3	Flash memory reset bit **(Notes 3, 4)**	0: Normal operation 1: Reset	0	○	○
4	Not used (Do not write “1” to this bit.)		0	○	○
5	User ROM area select bit **(Note 5)**	0: User ROM area is accessed 1: Boot ROM area is accessed	0	○	○
6	Program status flag	0: Pass 1: Error	0	○	×
7	Erase status flag	0: Pass 1: Error	0	○	×

Notes 1: For this bit to be set to “1”, the user needs to write a “0” and then a “1” to it in succession. For this bit to be set to “0”, write “0” only to this bit.
2: This bit can be written only when the CPU rewrite mode select bit is “1”.
3: Effective only when the CPU rewrite mode select bit = “1”. Fix this bit to “0” when the CPU rewrite mode select bit is “0”.
4: When setting this bit to “1” (when the control circuit of flash memory is reset), the flash memory cannot be accessed for 10 μs.
5: Write to this bit from program on RAM.

Fig. 2.12.3 Structure of Flash memory control register 0

Flash memory control register 1



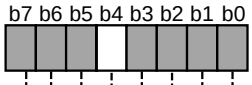
Flash memory control register 1
(FMCR1 : address 0FE1$_{16}$)

b	Name	Functions	At reset	R	W
0	Erase suspend enable bit **(Note 1)**	0 : Suspend invalid 1 : Suspend valid	0	○	○
1	Erase suspend request bit **(Note 2)**	0 : Erase restart (no request issued) 1 : Suspend request (request issued)	0	○	○
2	Nothing is arranged for these bits. If writing to these bits, write “0”. The contents are undefined at reading.		0	○	×
3			0	○	×
4			0	○	×
5			0	○	×
6	Erase suspend flag	0 : Erase active 1 : Erase inactive (Erase suspend mode)	1	○	×
7	Nothing is arranged for these bits. If writing to these bits, write “0”. The contents are undefined at reading.		0	○	×

Notes 1: For this bit to be set to “1”, the user needs to write a “0” and then a “1” to it in succession.
2: Only when the erase suspend bit is “1”, this bit is valid.

Fig. 2.12.4 Structure of Flash memory control register 1

Flash memory control register 2



Flash memory control register 2
(FMCR2 : address 0FE2$_{16}$)

b	Name	Functions	At reset	R	W
0	Nothing is arranged for these bits. If writing to these bits, write “0”. The contents are undefined at reading.		1	○	×
1			0	○	×
2			1	○	×
3			0	○	×
4	All user block E/W enable bit **(Notes 1, 2)**	0 : E/W disabled 1 : E/W enabled	0	○	○
5	Nothing is arranged for these bits. If writing to these bits, write “0”. The contents are undefined at reading.		0	○	×
6			1	○	×
7			0	○	×

Notes 1: For this bit to be set to “1”, the user needs to write a “0” and then a “1” to it in succession.
2: Effective only when the CPU rewrite mode select bit = “1”.

Fig. 2.12.5 Structure of Flash memory control register 2

2.12.4 Parallel I/O mode

In the parallel I/O mode, program/erase to the built-in flash memory can be performed by a flash memory programmer (EFP-I etc.).

The memory area of program/erase is from $0F000_{16}$ to $0FFFF_{16}$ (boot ROM area) or from 01000_{16} to $0FFFF_{16}$ (user ROM area). Be especially careful when erasing; if the memory area is not set correctly, the products will be damaged eternally.

Table 2.12.1 shows the parallel unit when programming by EFP-I in the parallel I/O mode.

•EFP-I provided by Suisei Electronics System Co., Ltd. (http://www.suisei.co.jp/index_e.htm) (product available in Asia and Oceania only)

Table 2.12.1 Parallel unit when parallel programming (when using EFP-I provided by Suisei Electronics System Co., Ltd.)

Products	Parallel unit	Boot ROM area	User ROM area
M38039FFHSP	EF3803F-64S	$0F000_{16}$ to $0FFFF_{16}$	01000_{16} to $0FFFF_{16}$
M38039FFHFP	EF3803F-64F		
M38039FFHHP	EF3803F-64H		
M38039FFHKP	EF3803F-64U		

2.12.5 Standard serial I/O mode

Table 2.12.2 shows a pin connection example (4 wires) between the programmer (EFP-I; Serial unit EF1SRP-01U is required additionally) and the microcomputer when programming in the standard serial I/O mode 1.

•EFP-I provided by Suisei Electronics System Co., Ltd. (http://www.suisei.co.jp/index_e.htm) (product available in Asia and Oceania only)

Table 2.12.2 Connection example to programmer when serial programming (4 wires)

Function	EFP-I (EF1SRP-01U)		Flash memory version		
	Signal name	EF1RP-01U side connector Line number	Pin name	M38039FFHSP pin number	M38039FFHSP pin number
Transfer clock input	T_SCLK	9	$P4_6/S_{CLK1}$	21	13
Serial data input	T_TXD	10	$P4_4/RxD_1$	23	15
Serial data output	T_RXD	11	$P4_5/TxD_1$	22	14
Transmit/Receive enable output	T_BUSY	12	$P4_7/\overline{S_{RDY1}}/CNTR_2$	20	12
"H" input	T_VPP	3	CNV_{SS}	26	18
Reset input	T_RESET	14	$\overline{RESET}$ (**Note 1**)	27	19
Target board power source monitor input	T_VDD **(Note 2)**	4	V_{CC} (**Note 2**)	1	57
GND	GND **(Note 3)**	1, 2, 15, 16	V_{SS}, AV_{SS} (**Note 3**)	32, 3	24, 59

Notes 1: Since reset release after write verification is not performed, when operating MCU after writing, separate a target connection cable.

2: Supply Vcc of EFP-I side from user side so that the power supply voltage of the output buffer used by the EFP-I side becomes the same as user side power supply voltage (Vcc).

3: Four pins (No. 1, 2, 15, and 16) of the EF1SRP-01U side connector are prepared for GND signal. When connecting with a target board, although connection of only one pin does not have a problem, we recommend connecting with two or more pins.

2.12.6 CPU rewrite mode

In the CPU rewrite mode, issuing software commands through the Central Processing Unit (CPU) can rewrite the built-in flash memory. Accordingly, the contents of the built-in flash memory can be rewritten with the microcomputer itself mounted on board, without using the programmer.
Store the rewrite control program to the built-in flash memory in advance. The built-in flash memory cannot be read in the CPU rewrite mode. Accordingly, after transferring the rewrite control program to RAM, execute it on the RAM.
The following commands can be used in the CPU rewrite mode: read array, read status register, clear status register, program, and block erase. For details concerning each command, refer to 3803 Group (Spec.H) Data Sheet “Flash memory mode (CPU rewrite mode)”.

(1) CPU rewrite mode beginning/release procedures

Operation procedure in the CPU rewrite mode for the built-in flash memory is described below.

[Beginning procedure]

① Apply “H” to the CNV_{SS} pin and $P4_5/TxD_1$ pin (at selecting boot ROM area).
② Release reset.
③ Set bits 6 and 7 (main clock division ratio selection bits) of the CPU mode register. (Make sure that system clock ϕ is less than 4.0 MHz.)
④ After CPU rewrite mode control program is transferred to internal RAM, jump to this control program on RAM. (The following operations are controlled by this control program).
⑤ Set “1” to the CPU rewrite mode select bit (bit 1 of address $0FFE_{16}$).
For this bit to be set to “1”, the user needs to write “0” and then “1” to it in succession.
⑥ Set “1” to the all user block E/W enable bit (bit 4 of address $0FE2_{16}$). Set the 8 KB user block E/W enable bit. (Set to “0” when E/W is disabled, and set to “1” when E/W is enabled.)*
* For these bits to be set to “1”, the user needs to write “0” and then “1” to those in succession.
⑦ Flash memory operations are executed by using software commands.

Note: The following procedures are also necessary.
- Control for data which is input from the external (serial I/O etc.) and to be programmed to the flash memory.
- Initial setting for ports, etc.
- Writing to the watchdog timer

[Release procedure]

① Execute the read array command.
② In order to disable E/W to the user ROM area (except for data block), set “0” to the all user block E/W enable bit (bit 4 of $0FE2_{16}$) and the 8 KB user block E/W enable bit (bit 2 of $0FE0_{16}$) **(Note 2)**.
③ Set the CPU rewrite mode select bit (bit 1 of address $0FFE_{16}$) to “0”.
④ Jump from the CPU rewriting control program on RAM to the user program on the flash memory.

Note 2: Although E/W inhibition is not indispensable, the safety of system improves by disabling E/W except the time of E/W execution.

Also, execute the following processing before the CPU reprogramming mode is selected so that interrupts will not occur during the CPU reprogramming mode.

• Set the interrupt disable flag (I) to “1”

When the watchdog timer has already started, write to the watchdog timer control register (address $1E_{16}$) periodically during the CPU reprogramming mode in order not to generate the reset by the underflow of the watchdog timer H.

During the program or erase execution, watchdog timer is automatically cleared. Accordingly, the inernal reset by underflow does not occur.

When the interrupt request or reset occurs in the CPU reprogramming mode, the microcomputer enters the following state;

• Interrupt occurs

This may cause a program runaway because the read from the flash memory which has the interrupt vector area cannot be performed.

• Underflow of watchdog timer H, reset

This may cause a microcomputer reset; the built-in flash memory control circuit and the flash memory control register are reset. When reset state is released with CNVss = “H” and $P4_5/TxD_1$ = “H”, CPU starts in the boot mode.

Also, when the above interrupt and reset occur during program/erase, error data may still exist after reset release because the reprogramming of the flash memory is not completed, so that reprogramming of the flash memory in the parallel I/O mode or serial I/O mode is required.

2.12.7 Flash memory mode application examples

The control pin processing example on the system board in the standard serial I/O mode and the control example in the CPU rewrite mode are described below.

(1) Control pin connection example on system board in standard serial I/O mode

As shown in Figure 2.12.4, in the standard serial I/O mode, the built-in flash memory can be rewritten with the microcomputer mounted on board. Connection examples of control pins ($P4_4$/RxD, $P4_5$/TxD, $P4_6/S_{CLK1}$, $P4_7/\overline{S_{RDY1}}/CNTR_2$, CNV_{SS}, and $\overline{RESET}$ pin) in the standard serial I/O mode are described below.

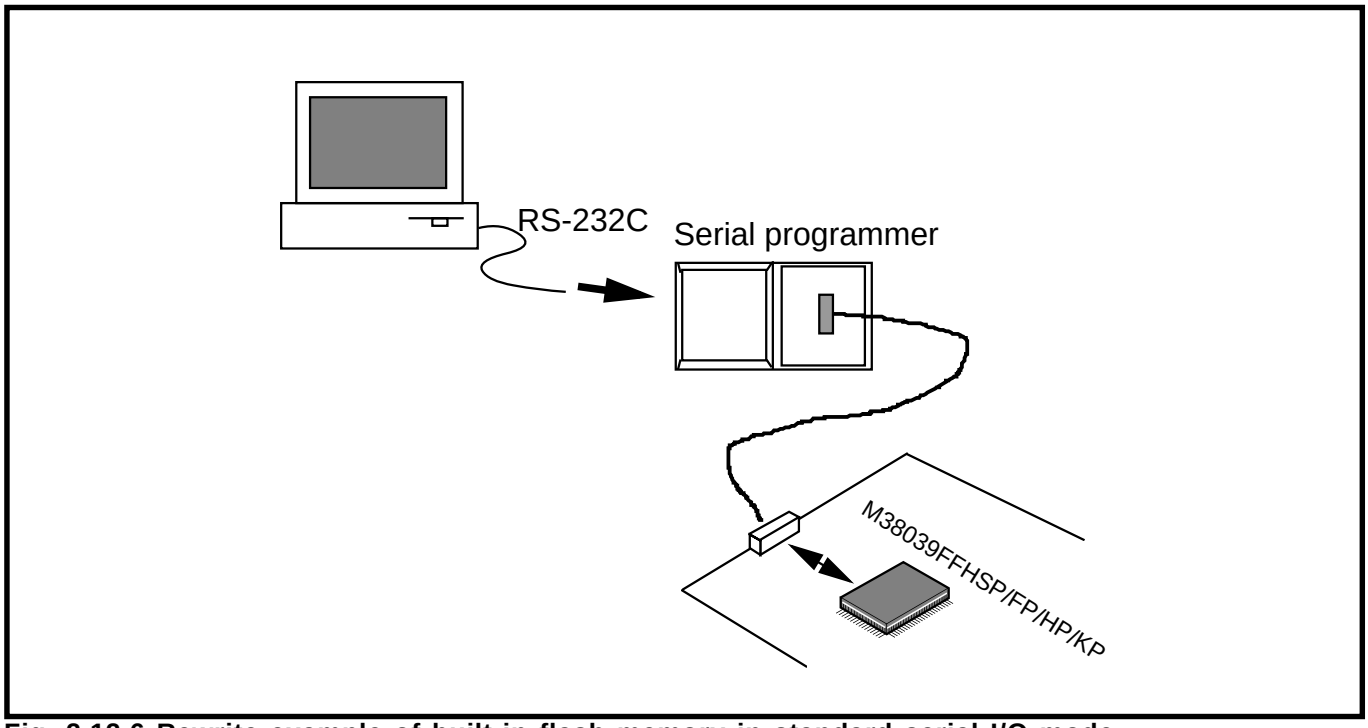
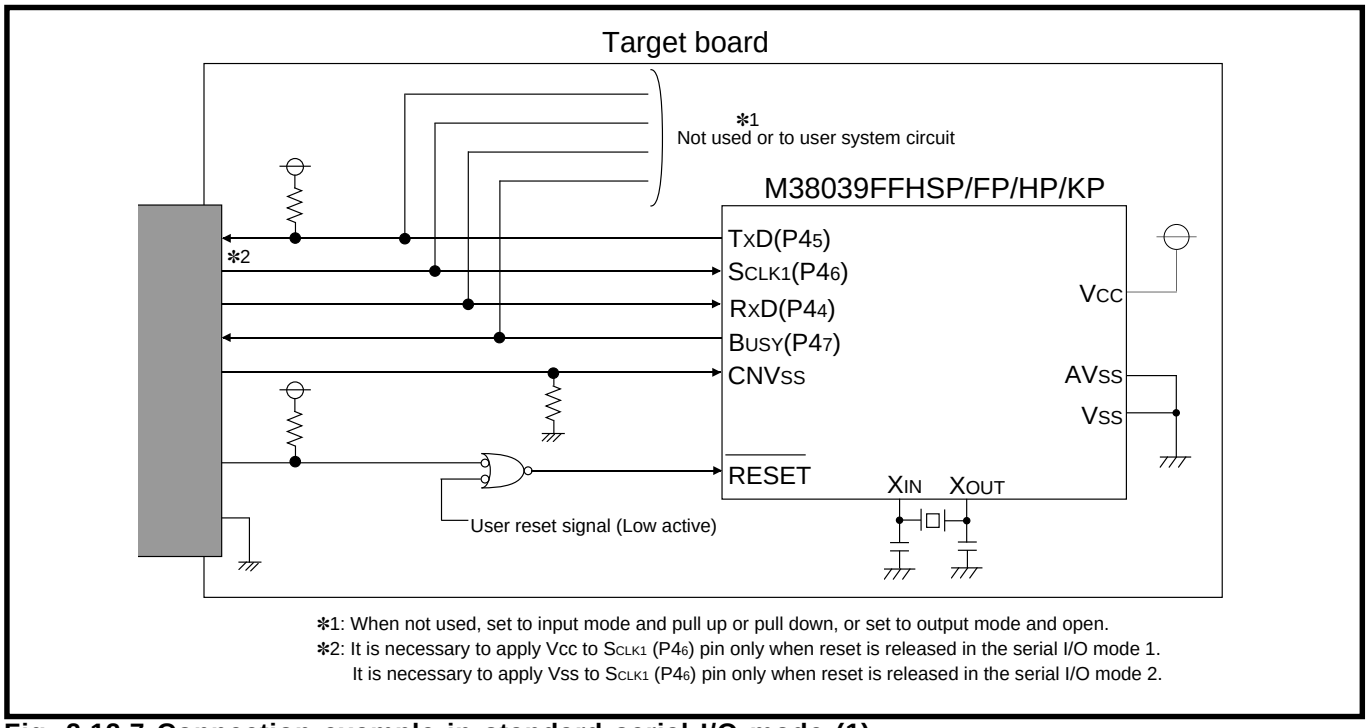


Fig. 2.12.6 Rewrite example of built-in flash memory in standard serial I/O mode

① **When control signals are not affected to user system circuit**

When the control signals in the standard serial I/O mode are not used or not affected to the user system circuit, they can be connected as shown in Figure 2.12.7.

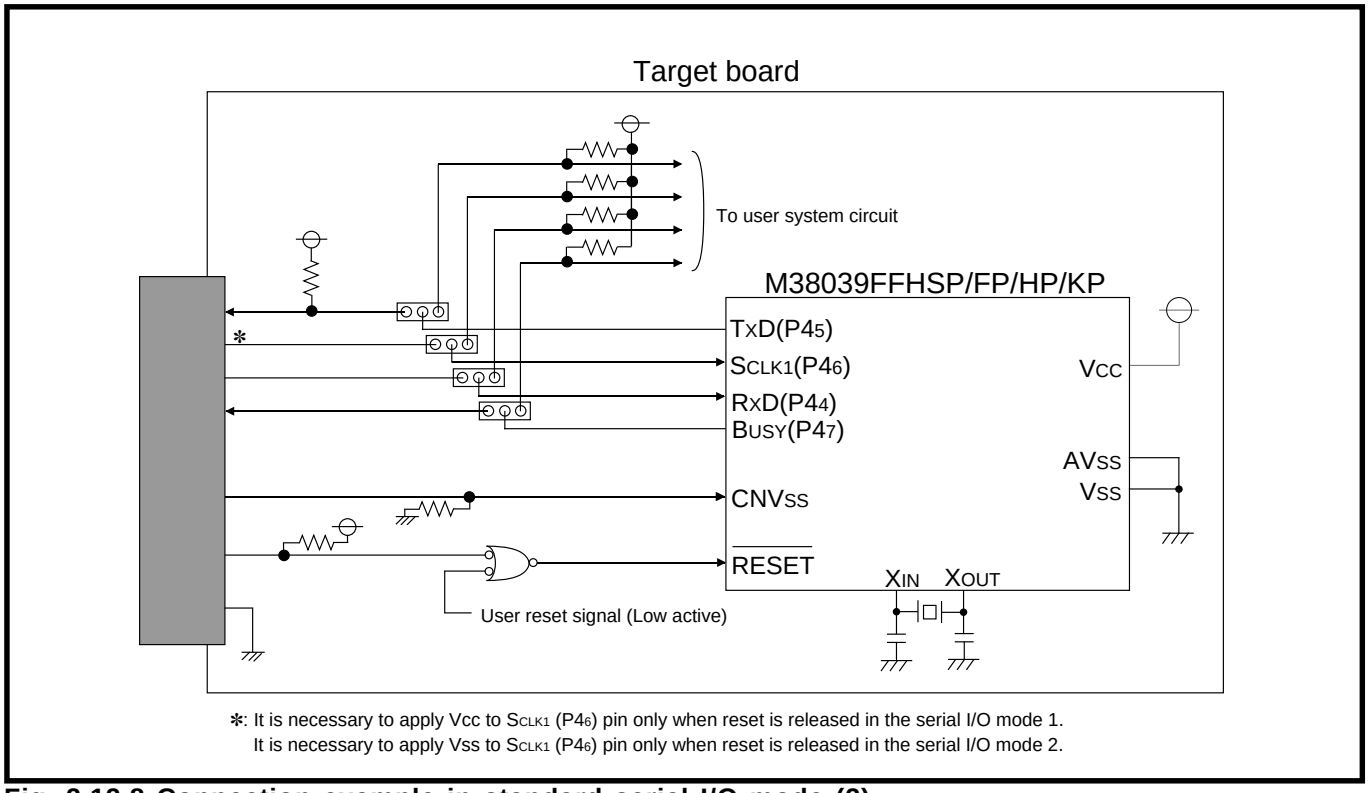


*1: When not used, set to input mode and pull up or pull down, or set to output mode and open.
*2: It is necessary to apply Vcc to SCLK1 (P46) pin only when reset is released in the serial I/O mode 1.
It is necessary to apply Vss to SCLK1 (P46) pin only when reset is released in the serial I/O mode 2.

Fig. 2.12.7 Connection example in standard serial I/O mode (1)

② **When control signals are affected to user system circuit-1**

Figure 2.12.8 shows an example that the jumper switch cut-off the control signals not to supply to the user system circuit in the standard serial I/O mode.

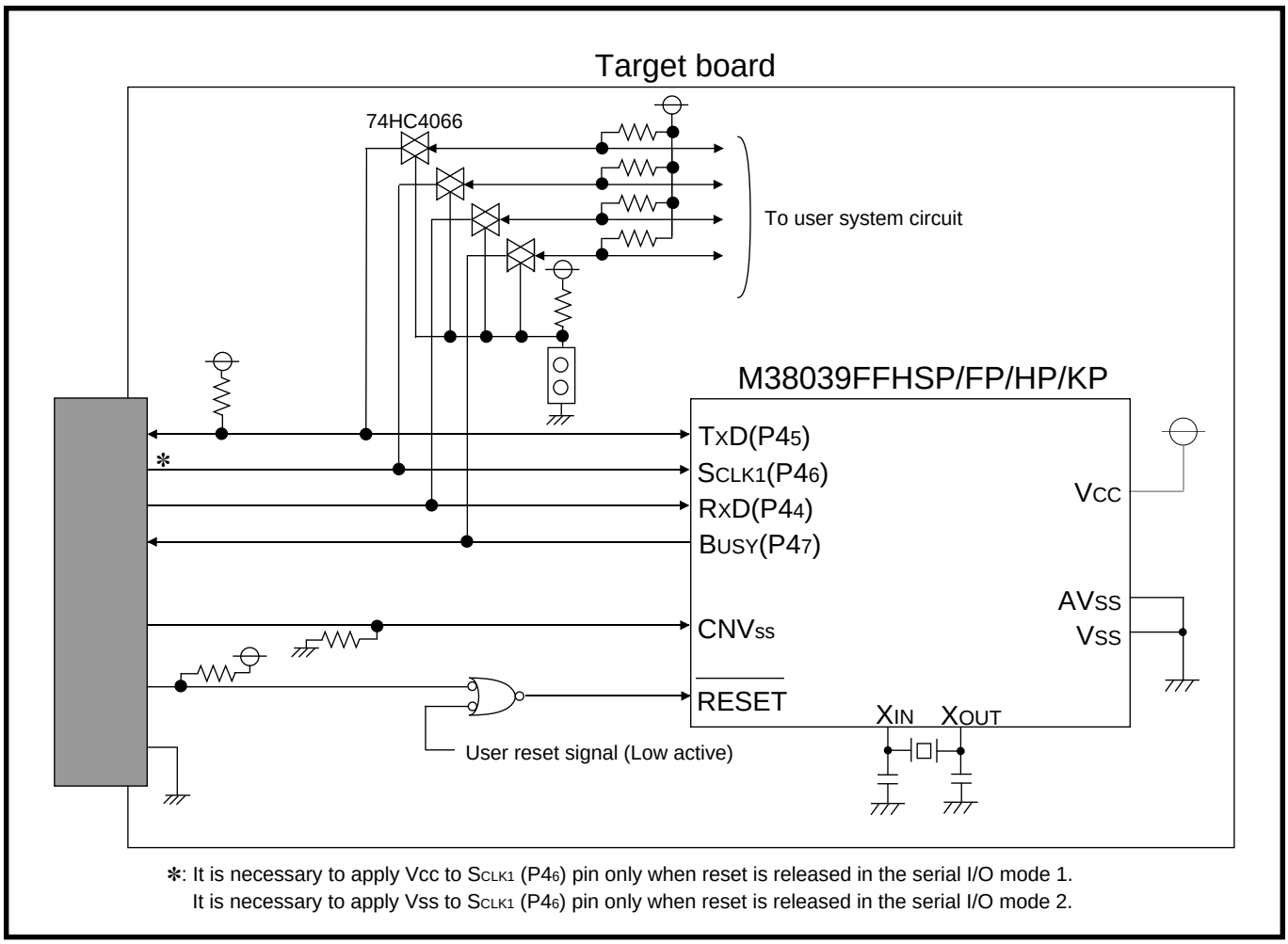


*: It is necessary to apply Vcc to SCLK1 (P46) pin only when reset is released in the serial I/O mode 1.
It is necessary to apply Vss to SCLK1 (P46) pin only when reset is released in the serial I/O mode 2.

Fig. 2.12.8 Connection example in standard serial I/O mode (2)

③ **When control signals are affected to user system circuit-2**

Figure 2.12.9 shows an example that the analog switch (74HC4066) cut-off the control signals not to supply to the user system circuit in the standard serial I/O mode.



*: It is necessary to apply Vcc to SCLK1 (P46) pin only when reset is released in the serial I/O mode 1.
It is necessary to apply Vss to SCLK1 (P46) pin only when reset is released in the serial I/O mode 2.

Fig. 2.12.9 Connection example in standard serial I/O mode (3)

(2) Control pin termination example in CPU rewrite mode

In this example, data is received by using serial I/O, and the data is programmed to the built-in flash memory in the CPU rewrite mode.

Figure 2.12.10 shows an example of the reprogramming system for the built-in flash memory in the CPU rewrite mode. For the CPU rewrite mode beginning/release method, refer to “2.12.6 CPU rewrite mode.”

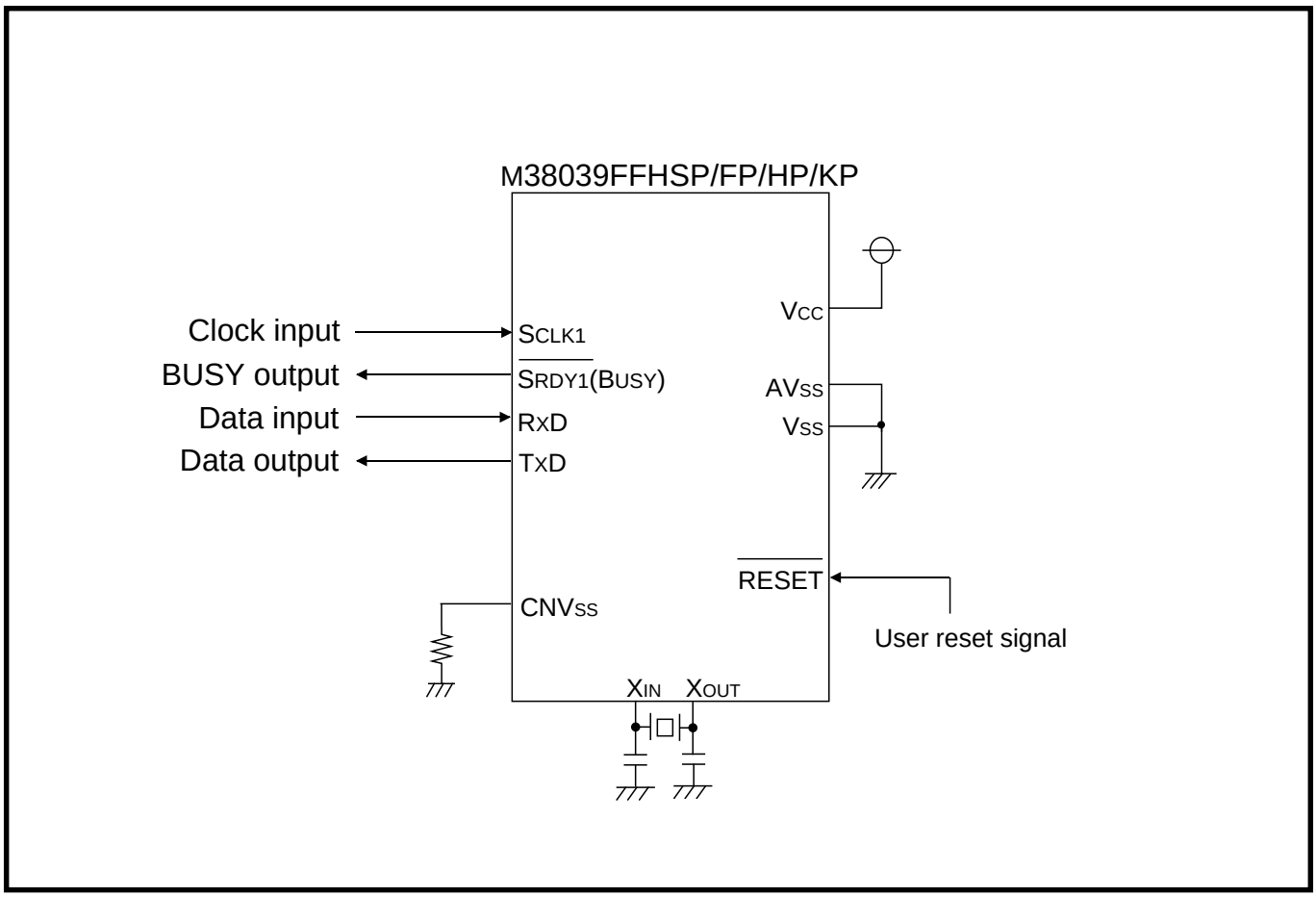


Fig. 2.12.10 Example of rewrite system for built-in flash memory in CPU rewrite mode (single-chip mode)

2.12.8 Notes on CPU rewrite mode

(1) Operation speed
During CPU rewrite mode, set the system clock ϕ 4.0 MHz or less using the main clock division ratio selection bits (bits 6 and 7 of address $003B_{16}$).

(2) Instructions inhibited against use
The instructions which refer to the internal data of the flash memory cannot be used during the CPU rewrite mode.

(3) Interrupts inhibited against use
The interrupts cannot be used during the CPU rewrite mode because they refer to the internal data of the flash memory.

(4) Watchdog timer
In case of the watchdog timer has been running already, the internal reset generated by watchdog timer underflow does not happen, because of watchdog timer is always clearing during program or erase operation.

(5) Reset
Reset is always valid. In case of CNV_{SS} = “H” when reset is released, boot mode is active. So the program starts from the address contained in address $FFFC_{16}$ and $FFFD_{16}$ in boot ROM area.

3. Reference Program Example

Please find the reference program on the Renesas Technology website.
Click the upper left menu of the screen “Application Notes” on the 740 family.

4. Reference

Data Sheet
3803 Group (Spec.H) Data Sheet

Technical News/Technical Update
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5. Website and Support

Renesas Technology Corporation Semiconductor Home Page
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REVISION HISTORY	3803 Group (Spec.H) Peripheral Function Application

Rev.	Date	Description	
		Page	Summary
1.00	Nov 14, 2005	-	This application note is issued using the information of "Chapter 2 APPLICATION" in the 3803 Group (Spec.H) User's Manual Rev.2.02.
		34	Fig.2.3.17 Control procedure is partly revised
		62	Fig.2.4.21 Registers setting relevant to transmitting side is partly revised
		64	Fig.2.4.23 Control procedure of transmitting side is partly revised
		68	Fig.2.4.29 Control procedure of serial I/O1 is partly revised
		71	Fig.2.4.33 Connection diagram is partly revised Specifications, Limitations of specifications are revised
		72	Fig.2.4.34 Timing chart is revised Fig.2.4.35 Relevant registers setting is partly revised
		73	●Control in the master unit is revised Fig.2.4.36 Control procedure of master unit is revised
		74	●Control in the slave unit is revised Fig.2.4.37 Control procedure of slave unit is revised
		79	Fig.2.4.42 Control procedure of transmitting side is partly revised
		80	Fig.2.4.43 Control procedure of receiving side is partly revised

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