Interfacing the RC3233x Series with HiFn 7902

Application Note AN-364

Notes

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Revision History

March 11, 2002: Initial publication.

October 18, 2002: Changed device designation to RC3233x to include 3 devices: RC32334, RC32333, and RC32332.

Introduction

The 79RC3233x series are integrated communications processors that integrate a high-performance 32-bit MIPS instruction set architecture CPU core with a number of on-chip peripherals. These peripherals include a SDRAM controller, PCI interface, and other general purpose peripherals such as UART, DMA, and Timers. The system bus features de-multiplexed address and data buses.

HiFn 7902

The HiFn 7902 is a high performance pipelined security processor that integrates a math processor and a random number generator. These blocks provide additional features to support public key cryptography. The integrated algorithms support standard network security protocols. With a minimum amount of external logic, the HiFn 7902 can be interfaced with standard processors, such as the RC3233x. A typical security application using the HiFn 7902 and RC3233x is a virtual private network (VPN) shown in Figure 1 below.

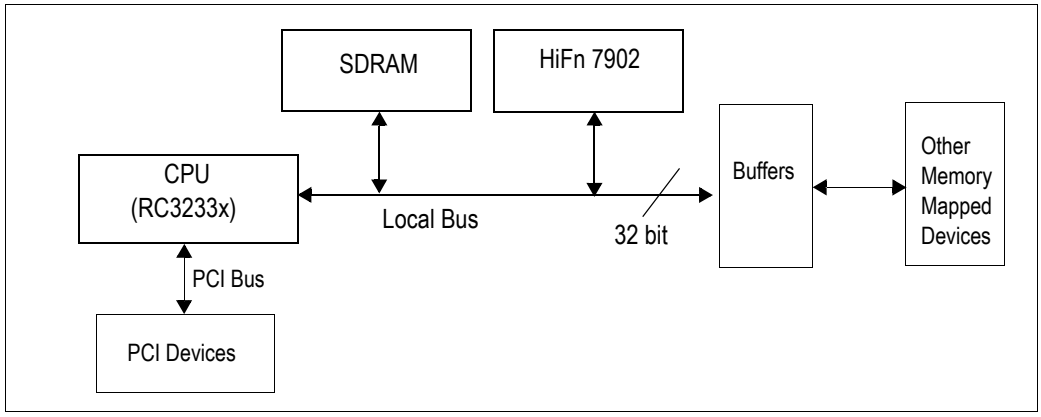

Figure 1 Typical VPN Router Application

Interfacing the RC3233x with the HiFn 7902

The HiFn 7902 data sheet refers to some pins, such as the address and data pins, with dual names. This application note uses the generic names to show the connections between the two devices. The connection between the RC3233x and HiFn 7902 components is similar to an SRAM interface in some aspects. Data can be transferred between the RC3233x and the security processor using standard load and store commands. The local system bus interface of the RC3233x provides the necessary signals to connect to the HiFn 7902. Since the Burst mode is not recommended for the RC3233x, the HiFn 7902 will be used in the single-beat transfer mode, i.e., non-burst mode. Figure 2 below shows an example interface between the two devices.

Notes

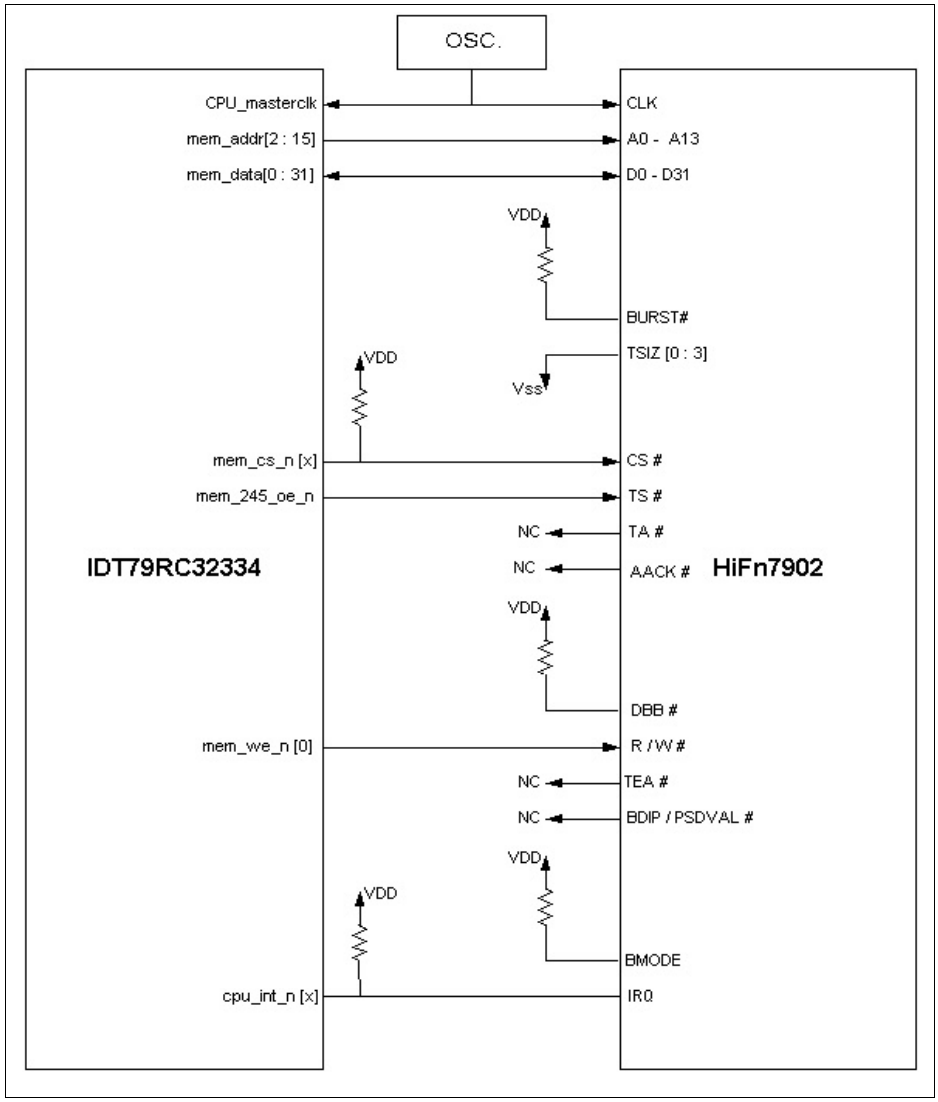

Figure 2 Example of HiFn 7902 Interface to the RC32334

The features of various pins and their interface is as described below:

CLK

This pin supplies the bus clock to the HiFn 7902 from the cpu-masterclk pin of the integrated processor. The HiFn 7902 can function at clock rates between 40Mhz to 66Mhz. The RC3233x local bus interface supports up to 75Mhz operation.

A0 - A13

The address bus of the HiFn 7902 is referred by dual names in the HiFn 7902 data sheet. The A0 - A13 lines are for interfacing any standard integrated processor to the address bus. These 14 lines are inputs to the HiFn 7902 where A0 is the least significant bit (LSB). The value specified on this bus indicates the memory location or register being accessed by the integrated processor.

D0 - D31

Like the address bus, the data bus is given dual names. The conventional DO - D31 indicates that the HiFn 7902 is being used with a standard processor. This bus is bi-directional and is normally an input unless a Read operation is being performed. It interfaces to the RC3233x's data bus.

Notes

BURST #

This pin is used to indicate a burst transfer. However, burst transfers cannot be used with the RC3233x as a burst transfer would complete with an implementation specific method that does not meet the RC3233x's burst protocol or command recovery period (i.e. BTA period). Therefore, the BURST # pin is tied to "high" to ensure that it never gets enabled.

TSIZ [0 : 3]

These pins are inputs to the HiFn 7902 and indicate the transfer size. Since BURST # is tied to high, TSIZ [0 : 1] will have values of [00], indicating the transfer size is a word (4 bytes). Pins TSIZ [2 : 3] are not used and therefore tied to low to prevent the input buffers from floating.

CS #

The chip select pin is an input to the HiFn 7902 and is used along with the R/W # pin to initiate a data transfer in either direction.

TS #

Transfer start is an input to the HiFn 7902 and indicates a start of transfer. A similar function is provided by the RC3233x's mem_245_oe_n output. This output controls the output enable to optional FCT245 transceiver bank by asserting during both read and write operations. Note that the timing requirements for the TS # signal are met by the mem_245_oe_n signals.

TA #

The transfer acknowledge pin is an output from the HiFn 7902 and indicates an end of transfer. This feature is not supported by the RC3233x. Therefore, the TA # pin is left unconnected.

AACK # and DBB #

The AACK # and DBB # pins are specific pins designed in the HiFn 7902 processor to make it compatible with other processors, such as the MPC8260. The AACK # pin is left open and the DBB # pin is tied high for this interface, as recommended by HiFn.

R / W #

The read/write input pin in the HiFn 7902 is active high, when the pin is high a read operation is performed. This pin is driven by the mem_we_n[0] pin of the RC3233x.

TEA #

The transfer error acknowledge feature of the HiFn 7902 is not supported by the RC3233x. This pin is left unconnected.

BDIP / PSDVAL #

Since the burst data transfers are not recommended when using the RC3233x, this pin is left unconnected. Its function is to indicate that a burst transfer is in progress.

BMODE

As recommended for the HiFn 7902, the BMODE pin is tied high when any processor other than the MPC8260 is used.

IRQ

The interrupt request is a tri-stateable output from the HiFn 7902 processor. It can be used with one of the valid interrupts cpu_int_n [5:4], [2:0] of the RC3233x. This signal is pulled high, as recommended in the HiFn 7902 data sheet.

Timing

Note that some of the functions of the HiFn 7902 are unused, as mentioned in the section above. The functions that are used for the RC3233x and HiFn 7902 interface meet all applicable timing requirements. Specifically, the R / W # single-beat timing is met between the RC3233x and HiFn 7902.

Notes

For information on timing for the RC32334, refer to Table 6, AC Timing Characteristics, in the RC32334 Data Sheet, located at: http://www.idt.com/products/pages/Integrated_Processors-79RC32334.html.

For information on timing for the RC32332, refer to Table 6, AC Timing Characteristics, in the RC32332 Data Sheet, located at: http://www.idt.com/products/pages/Integrated_Processors-79RC32332.html.

Conclusion

Using the example interface shown in Figure 2 above, the RC3233x can be easily connected to the HiFn 7902 device for single-beat transfers. Note that this document is for reference purposes only and is intended to give the system designer a first-hand view of the interface between the two processors. The logic has not been verified or characterized by IDT.

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