Connecting RC32355/RC32351 to the AD6449-48/AD6482 ADSL Digital Datapump

Notes

Revision History

November 5, 2001: Initial publication.

December 18, 2001: Added RC32351

Background

The RC32355/RC32351 Integrated Communications Processor (ICP) meets the requirements of various embedded communications applications, including residential gateways, Internet Access Devices (IAD), SOHO routers, and wireless systems. It is a single-chip solution that incorporates most of the generic system functions and application-specific interfaces that enable rapid time to market, very low cost systems, simplified designs, and reduced board real estate.

In addition to a high performance 32-bit CPU core, the RC32355/RC32351 ICP incorporates a number of on-chip generic peripherals, including an SDRAM controller, a separate memory/IO controller supporting 8-, 16- and 32-bit peripherals, an interrupt controller, timers, and serial ports. The RC32355/RC32351 device also integrates four on-chip peripherals specifically targeted for communications applications:

1. A 10/100Mbps Ethernet controller.
2. An ATM segmentation and reassembly (SAR) capable of operating up to 25Mbps.
3. A USB device controller supporting data rates up to 12Mbps, fully compatible with version 1.1 of the USB specification.
4. An industry-standard TDM/PCM bus interface (not available on the RC32351). The TDM bus enables an interface to directly access external devices such as telephone CODECs and quality audio A/Ds and D/As. This feature is critical for applications requiring support of voice, mix voice, and data to support voice-over-x applications.

This technical note describes the interface between the RC32355/RC32351 and the Analog Device's AD6449-48/AD6482 ADSL Digital Datapump.

AD6482 Description

The AD6482 Digital Datapump (Eagle) integrates a framer, DMT coprocessor, DSP, and interleave RAM on a single chip. It performs all physical-layer digital transceiver functions needed for ADSL systems. A block diagram of the Eagle chipset is shown on Figure 1.

Notes

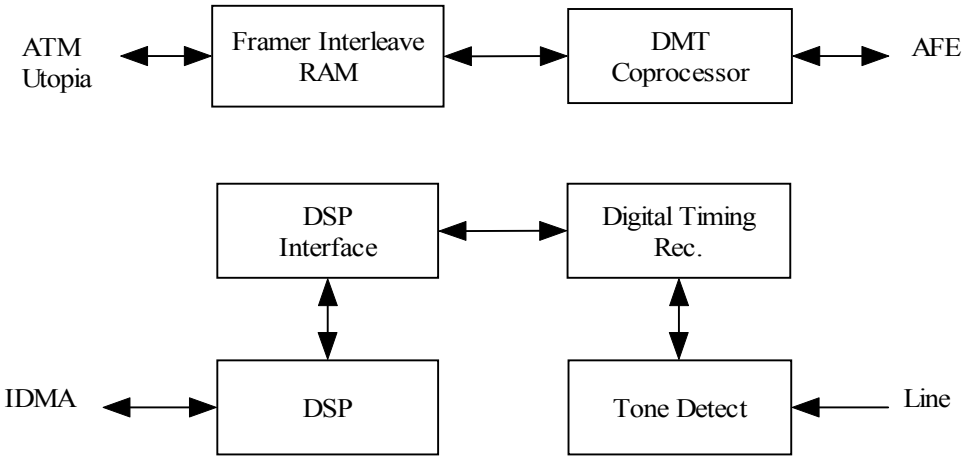

Figure 1 AD6482 Block Diagram

ADSL modem code is usually in an external flash memory location and is downloaded by the DSP model after hardware reset. The AD6482 device allows code to be downloaded through the IDMA port. The IDMA boot method allows elimination of the flash memory for the ADSL subsystem.

The IDMA port is a 16-bit parallel port that allows the DSP internal memory to be accessed by an external agent. The IDMA port has a multiplexed address and data bus that allows access to both 16-bit data memory and 24 bit program memory. Internal DSP memory can be accessed even during DSP operations.

IDMA Interface

IAD15-0	I/O	IDMA port address/data bus
IRDN	I	IDMA read enable
IWRN	I	IDMA write enable
ISN	I	IDMA port select
IAL	I	IDMA port address latch enable
IACKN	O	IDMA port access ready acknowledge

For writing information into IDMA control register, both ISN and IAL signals should be asserted. The control register is memory-mapped at 0x3FE0 and cannot be read back. Refer to Figure 2.

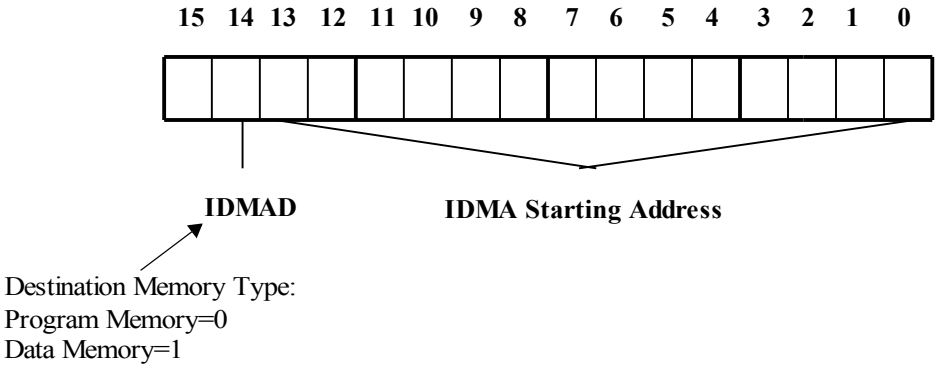

Figure 2 IDMA Control Register

Notes

Reading from the DSP memory is achieved by activating ISN and IRDN. Similarly, writing is performed by asserting ISN and IWRN.

IDMAD Bit

The IDMA bit determines if the data or the program memory is being accessed. Because program memory is 24 bits wide, 2 accesses are needed for every word. On the first access, the upper 16 bits of the 24-bit word are accessed. On the second access, the lower 8 bits of the IAD bus, containing valid data, are accessed. For reads, the upper 8 bits are 0; for writes, the upper 8 bits are ignored.

After the completion of an entire memory access (1 word for data memory and 2 words for the program memory), the starting address in automatically incremented by one. Thus, the transfer of a block of "n" words requires first writing to the IDMA control register followed by n or 2n 16-bit transfers, depending on whether data or the program memory is being accessed.

Hardware Interfacing with IDT79RC355

Hardware interfacing with the 79RC32355/RC32351 is shown in Figure 3. The logic can be implemented as a part of a PLD or with discrete components.

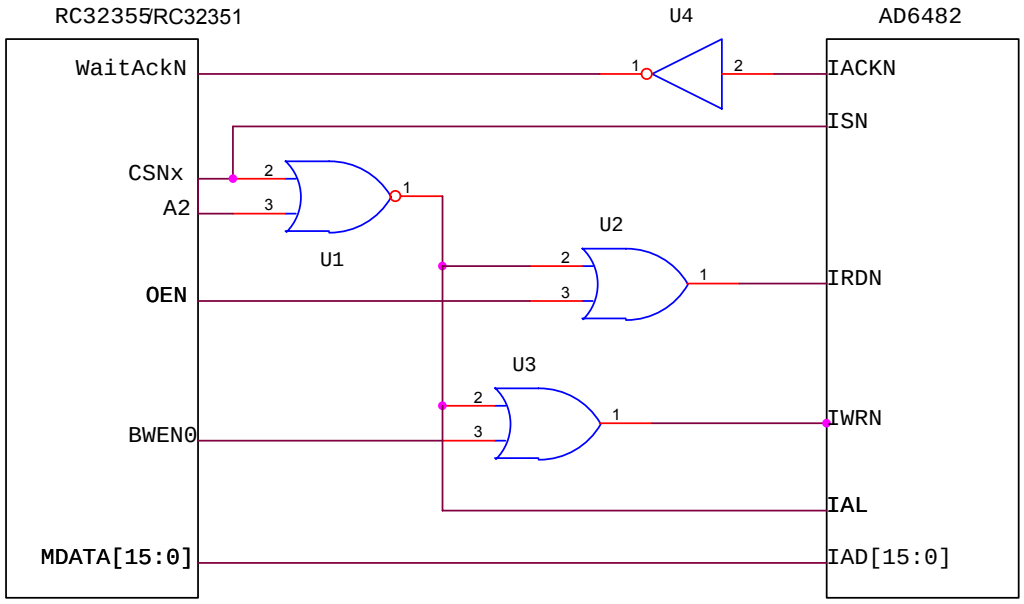

Figure 3 Interface Between RC32355/RC32351 and AD6482

Addresses are written to the IDMA control register when CSNx is active (i.e., 0) and A2=0. During address write cycles, IRDN and IWRN should be high. This is implemented with OR gates U2 and U3. The desired address should be driven on the data lines during this transaction.

Information is written to or read from data or program memory when CSNx is active and A2=1.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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