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RENESAS

Application Note

Operation of Ravin-E with V850 Devices

Document No. S17194EE1V0AN00
Date Published June 2004

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Chapter 1 Introduction

Ravin-E (µPD72255) is a graphics display controller, which has originally been designed for use in high-end automotive navigation and multimedia systems. These systems require typically a high performance CPU for different tasks like processing of sensor data (gyro, acceleration sensor, compass, GPS), navigation and tracking, audio processing (noise and echo cancellation, speech recognition, compressed audio decoding) and last but not least graphics and probably video processing. Especially audio and graphics processing can be very demanding if the quality requirement exceeds a certain minimum level. For these reasons, Ravin-E was designed for use with high end 32- and 64-bit CPUs of the MIPS RISC family.

Recently more and more customers outside of the automotive business have recognized the sophisticated features of Ravin-E and they share the requirement of a high quality display controller, but without the need of very high CPU performance. Many of these customers have already used derivatives of the V850 products, they are familiar with the architecture and the development tools and therefore they are reluctant to change the product family. V850 products can also offer some cost advantage over the MIPS RISC devices and also most V850 devices are available with on-chip ROM or Flash. In many cases also the on-chip peripherals of the V850 devices are more attractive for a particular application than those of the MIPS RISC devices.

This application note describes the basic functionality of the Ravin-E and the V850/V850E bus interfaces as well as the possibilities to connect them to each other. While we do not especially recommend to connect a V850 or V850E with 16-bit external bus to Ravin-E, this is possible and an outline of the required interface is shown in chapter 2.4 at page 16. Chapter 2.2 at page 11 shows the interface to a V850E/ME2, which has a 32-bit bus interface. Unlike the 16-bit bus interface, the connection between Ravin-E and a V850E/ME2 with 32-bit interface has been physically built and extensively tested. Sample programs are discussed in chapter 4.3 (page 22) and some timing measurements are provided in chapter 5.

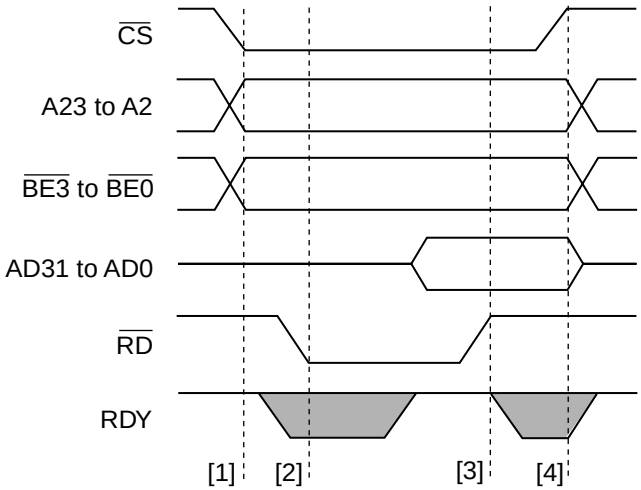
Chapter 2 Hardware Description

2.1 Ravin-E Bus Interface

Ravin-E is a high end graphics display controller and as such it generates significant data traffic on its buses which increases with the resolution and frame rate of the display, the number of display layers and the size and frame rate of a captured video. A wide CPU-bus interface is required, when pixel images are transferred directly to the frame buffer, or when large drawing lists are downloaded. For these reasons, the CPU and SDRAM interfaces are 32-bit wide and the CPU bus can be switched between PCI mode and asynchronous (SRAM-like) mode. This application note is restricted to the SRAM-like mode, because there are no V850 devices with built-in PCI interface.

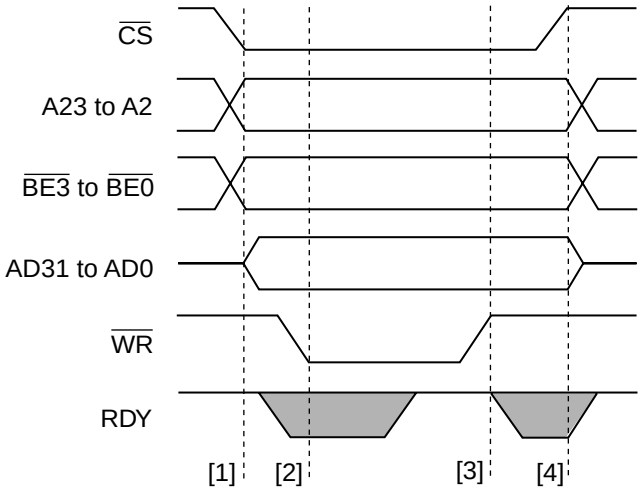
The Ravin-E read and write timing diagrams are depicted in Figure 2-1 and Figure 2-2 respectively. For reading data from Ravin-E, the CPU must apply the addresses, the byte enable signals and chip select. In response to chip select, Ravin-E pulls the RDY signal low, to indicate that the data is not yet available. The CPU must then activate RD to request a data read. After the requested data is available, Ravin-E releases the RDY signal so that the CPU can finish its bus cycle.

Figure 2-1: Ravin-E read timing



A write cycle is very similar to a read cycle. The Ravin-E data bus is switched to input and data is provided by the CPU. Again, when the RDY signal is released, the CPU can finish its bus write cycle.

Figure 2-2: Ravin-E write timing



2.2 V850E/ME2 Bus Interface

The V850E/ME2 has an external bus interface, which supports accesses to SRAM/ROM/Flash and to SDRAM. These memory access methods share the same address and data bus, but they use different control signals. For SDRAM accesses, the address lines carry the multiplexed row and column address signals.

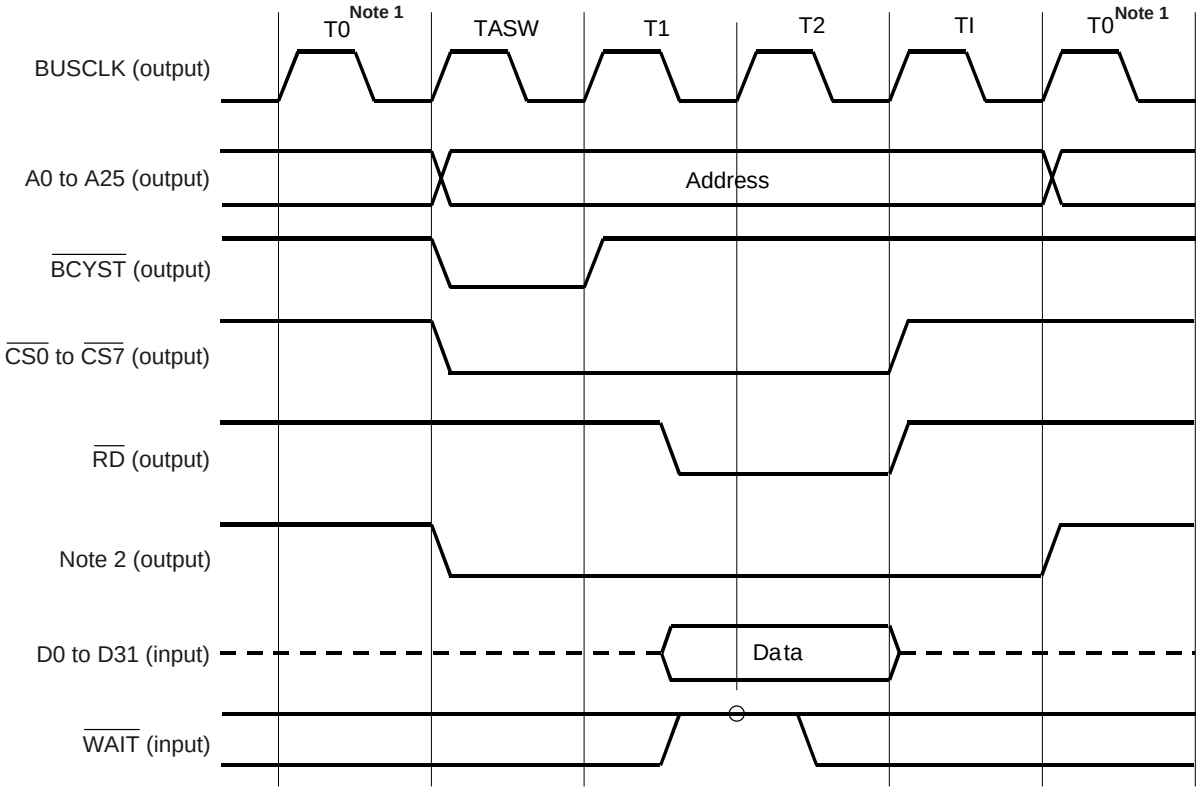
The principle read and write timings of the V850E/ME2 for SRAM accesses are depicted in Figure 2-3 and Figure 2-4. It is apparent that the V850E/ME2 timing is a synchronous timing, in which all bus activity is referenced to a rising or falling edge of the BUSCLK output. A basic and maximum speed SRAM bus cycle consists of the T1 and the T2 state. The addresses and the chip select signal become valid after the rising edge of T1. The $\overline{RD}$ or $\overline{WR}$ output is activated with the T1 falling edge and T2 is used for data transfer. At the end of T2, i.e. with the rising clock edge of the subsequent state, the data transfer is finished and the control signals are returned to inactive.

Four control signals indicate which portion of the data bus conveys valid data. If A is a word address, then $\overline{LLBE}$ indicates valid data at A+0, $\overline{LUBE}$ at A+1, $\overline{ULBE}$ at A+2 and $\overline{UUBE}$ applies for A+3. Note that the $\overline{xxBE}$ signals are shared with the $\overline{xxWR}$ signals. Ravin-E requires $\overline{xxBE}$ functionality, because the enable signals must be stable while $\overline{RD}$ or $\overline{WR}$ are active. As this is not the default after reset, the PFCCT register must be set to 0x0f during initialization to allow Ravin-E accesses.

The basic bus access can be extended in several ways. The address setup time is extended by inserting up to three address wait states (TASW) before the T1 bus state. Up to seven wait states can be automatically inserted between the T1 and the T2 state. Further wait states are generated, as long as the $\overline{WAIT}$ input is pulled low and up to three idle states (TI) can be inserted at the end of the bus cycle.

Figure 2-3: V850E/ME2 principle SRAM read timing

(a) When read (without speculative read, address set up wait, idle state insertion)



Notes: 1. State (T0) inserted between bus cycles

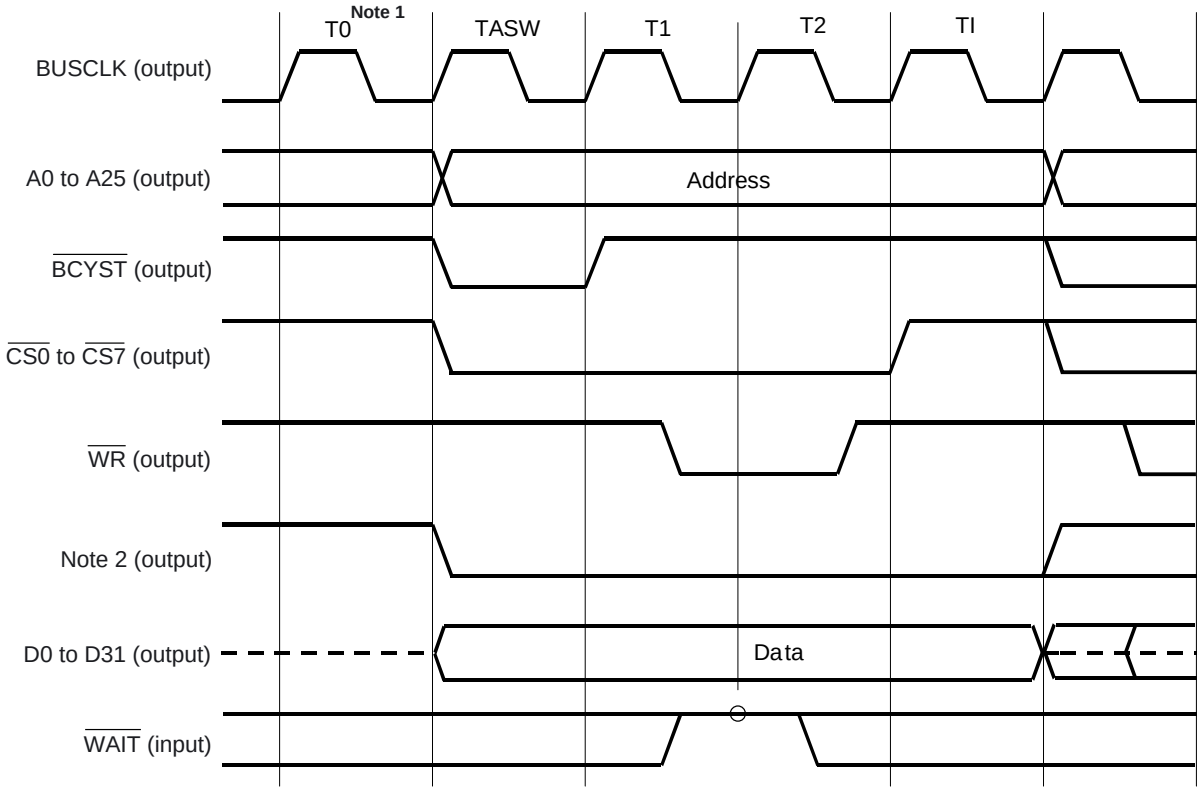
2. UUBE, ULBE, LUBE, LLBE

Remarks: 1. The circle O indicates the sampling timing.

2. The broken lines indicate the high-impedance state.

Figure 2-4: V850E/ME2 principle SRAM write timing

(a) When written (address setup wait, idle state insertion)



Notes: 1. State (T0) inserted between bus cycles

2. UUBE, ULBE, LUBE, LLBE

Remarks: 1. The circle O indicates the sampling timing.

2. The broken lines indicate the high-impedance state.

2.3 Access Time Considerations

As it is the case with probably most electronic designs, the designer may have a certain degree of freedom in the interpretation of the electrical specifications. Many timings have minimum and maximum values specified. These parameter ranges account for the full specified voltage and temperature range. They also include variations in the manufacturing process and aging of the device. Therefore it is reasonable to assume that the drift of parameters on the same device are correlated to one another. In first approximation, all subcomponents of the device have the same temperature and operating voltage, they went through the same manufacturing process and they have the same age. In the following discussion we assume therefore, that the variation of all parameters is the same. While this assumption is probably not acceptable for safety critical equipment, it is common practice for most designs that have reduced safety requirements. According to individual taste and risk assessment, one can apply a safety margin between 0 and 100%. The full safety margin will most likely impact the performance.

The following table lists the most critical parameters for reliable operation of Ravin-E with the V850E/ME2. An eye must be kept on the other parameters as well, but they are usually uncritical and met under all conditions.

The V850E/ME2 has different minimum bus clock cycle times. Depending on the bus load capacitance, 19 ns (52.6 MHz) or 14.2 ns (70.4 MHz) are permitted. To keep things simple, the table neglects signal rise and fall times. For conditions where the timing margin is small, it is advisable to consider these rise and fall times as well as propagation delays of the PCB traces.

Table 2-1: Most critical parameters for reliable operation of Ravin-E with the V850E/ME2

Ravin-E parameter	Ravin-E	V850E/ME2 Busclk T=19 ns	Margin (n=0)	V850E/ME2 Busclk T=14.2 ns	Margin (n=0)	V850E/ME2 timing calculation
T_{AS}	min. 5 ns	6.5 + n × 19 ns	1.5 ns	4.1+ n × 14.2 ns	-0.9 ns	$t_{WKH1} + t_{DKRDL} - t_{DKA} + n \times T$
T_{RS}/T_{WS}	min. 0 ns	6.5 + n × 19 ns	6.5 ns	4.1+ n × 14.2 ns	4.1 ns	$t_{WKH1} + t_{DKRDL} - t_{DKA} + n \times T$
T_{AH}	min. 5 ns	14.5 ns	9.5 ns	12.1 ns	7.1 ns	$t_{SWK} + t_{WKH1} + t_{HKWRH}$
T_{DH}	min. 5 ns	0 ns	5 ns	0 ns	5 ns	$t_{HKID} - t_{HKRDH}$
T_{AWH}	min. 5 ns	8.5 ns	3.5 ns	6.1 ns	1.1 ns	$t_{WKL1} + t_{HKOD} - t_{HKWRH}$
T_{DRCS}	min. 0 ns	0 ns	0 ns	0 ns	0 ns	$t_{HKA} - t_{HKRDA}$
T_{DD}	max. 5 ns	19 ns	14 ns	14.2 ns	9.2 ns	$t_{SWK} + T - t_{SKID}$

Remark: n is the number of address wait states

The following table is an except from the current V850E/ME2 data sheet and it lists the timing values that have been used for the above calculations. Note that these values might change in subsequent revisions, so make always sure to use the latest data sheet.

Table 2-2: Timing values

Symbol	Min	Max
t_{WKH1}	0.5T - 2 ns	0.5T + 2 ns
t_{WKL1}	0.5T - 2 ns	0.5T + 2 ns
t_{DKRDL}	1 ns	11 ns
t_{DKA}	2 ns	11 ns
t_{SWK}	6 ns	
t_{HKWRH}	1 ns	11 ns
t_{HKID}	2 ns	
t_{HKRDH}	2 ns	11 ns
t_{HKOD}	2 ns	11 ns
t_{HKA}	2 ns	11 ns
t_{HKRDA}	2 ns	11 ns
t_{SKID}	6 ns	

The above analysis of V850E/ME2 and Ravin-E timings shows that both devices can be connected to each other with sufficient margin. If the V850E/ME2 is operating at the maximum bus speed of T=14.2 ns, then an address wait state must be inserted for reliable operation.

T_{DRCS} is the $\overline{RD}$ to $\overline{CS}$ delay time, which requires that $\overline{CS}$ must not return to inactive before $\overline{RD}$ is inactive. That specification might be a concern, because the timing margin is 0 ns. Violation of the T_{DRCS} specification will, however, not automatically lead to a corrupted bus-cycle. The cycle will simply end prematurely and the timing parameters that are related to the rising edge of $\overline{RD}$, will not be valid anymore. If the host CPU is happy with the reduced data hold time T_{DH}, then this is a perfectly valid Ravin-E read cycle.

2.4 Connecting a V850 or V850E with 16-bit External Bus to Ravin-E

Ravin-E requires a 32-bit bus interface, but most V850 and V850E devices provide only a 16-bit wide data bus. In some applications one might accept the reduced performance that comes with the 16-bit interface of a V850. In this chapter we discuss a basic bus extender, which adapts the 16-bit V850 bus to the 32-bit Ravin-E bus. It should be noted that we have never really built such a circuit and consequently this is just a “thought experiment”. We have written and simulated Verilog code, which can be easily mapped into a small CPLD. Building the bus extender in discrete logic doesn't seem worthwhile.
The described bus extender has multiple limitations. Obviously it reduces the data throughput to half the bus frequency, because two bus accesses are required where only one would be necessary in a pure 32-bit system. A more subtle restriction is the address space. Most V850 devices can only address external memory of up to 1, 4 or 16 MB. That is more than sufficient to access the Ravin-E Registers, which occupy only 4 KB, but it may be less than the size of the Ravin-E frame buffer. In such a case the HostCpuBaseAddr register will have to be updated every time when the required frame buffer address is out of the current scope. Finally, the described bus extender supports only 32-bit word accesses. Read-modify-write cycles are required, if smaller entities have to be written. With a little more overhead it will be possible to access bytes and halfwords, but we restrict this description on the basics. For this reason, the current implementation does not use the $\overline{\text{UUBE}}$... $\overline{\text{LLBE}}$ signals.

The principle idea of the bus extender is to register the halfword, which cannot currently be transferred. When doing a word access via a 16-bit bus, the V850 devices transfer the lower 16-bit halfword in the first bus cycle and the higher 16-bit halfword in the second bus cycle. Therefore the bus extender must provide two different 16-bit registers, one for read accesses and the other one for write accesses.

For read accesses, i.e. data transfer from Ravin-E to the V850, the first CPU bus cycle performs a 32-bit Ravin-E read access and with the rising edge of the CPU $\overline{\text{RD}}$ signal, the upper halfword is stored in a 16-bit register, while the lower halfword is directly read from Ravin-E. The subsequent 16-bit read access transfers the stored upper halfword to the CPU. The write access is very similar, but the lower halfword must be stored during the first write access, while the second write access actually transfers the upper halfword from the CPU directly to Ravin-E, while the lower halfword is taken from the register. As can be seen in the timing diagram on the subsequent page, the bus extender generates chip enable and byte enable signals also for those V850 cycles, which do not generate Ravin-E cycles. No actual Ravin-E cycle will be executed, however, because the read and write lines remain inactive. This is a principle yet acceptable flaw in the concept. The reason are the delayed read and write signals relative to the chip enable input. Only when read or write gets active, we can decide whether or not a Ravin-E cycle is to be performed, but then it may be too late to activate the chip and byte enable outputs.

A workaround for that dilemma would be to perform the Ravin-E cycles always when the upper or lower halfword is accessed, independent of the data transfer direction. Then the bus extender can decide depending on the A1 address, whether to generate a Ravin-E cycle. The drawback of that solution would be that word accesses are only performed for reading or writing. The other word access would have to be replaced by two halfword accesses.

2.4.1 Bus extender Verilog code

```
// DESIGNER  :Michael Kraemer
// OBJECT    :MODULE BusExtender for V850 16-bit bus to Ravin-E 32-bit bus
// DATE      :07. April 2004
// REVISION  :1.0

// Untested Sample!!! Use with care!
// This module shall interface a 16-bit V850 CPU to a 32-bit Ravin-E

module BusExtender(dv, dr, ncei, nwri, nrdi, a1, nceo, nwro, nrdo, nbeo,
                   rdyi, nwaito, probe) ;

    inout   [15:0] dv ; // 16-bit V850 data bus
    inout   [31:0] dr ; // 32-bit Ravin-E data bus
    input   ncei ;      // chip enable input (active low)
    input   nwri ;      // write input (active low)
    input   nrdi ;      // read input (active low)
    input   a1 ;        // A1 from CPU
    output  nceo ;      // chip enable output (active low)
    output  nwro ;      // chip enable output (active low)
    output  nrdo ;      // chip enable output (active low)
    output  [3:0] nbeo ;// byte enable output (active low)
    input   rdyi ;      // ready input from Ravin-E (active high)

    output  nwaito ;    // wait output to CPU (active low)
    output  probe ;

    reg     [15:0] dreg ;// data register
    reg     rnw ;       // to remember read or write access

    wire    cpuread_lower, cpuread_upper, cpuwrite_lower, cpuwrite_upper ;
    wire    cpuread, cpuwrite, cclk ;

//assign defaults
assign cpuwrite = ~ncei & ~nwri ;
assign cpuread = ~ncei & ~nrdi ;
assign cpuread_lower = ~ncei & ~nrdi & ~a1 ;
assign cpuread_upper = ~ncei & ~nrdi & a1 ;
assign cpuwrite_lower = ~ncei & ~nwri & ~a1 ;
assign cpuwrite_upper = ~ncei & ~nwri & a1 ;
assign nceo = ncei ;
assign nwro = ~cpuwrite_upper ;
assign nrdo = ~cpuread_lower ;
assign nbeo[3:0] = {ncei, ncei, ncei, ncei} ;
assign nwaito = ~(~rdyi & (cpuwrite_upper | cpuread_lower)) ;
assign cclk = ncei | ~((~nrdi & ~a1) | (~nwri & ~a1)) ;
assign probe = rnw ;

always @(negedge nwri or negedge nrdi)
begin
   if (!nwri) rnw <= 0 ;
   if (!nrdi) rnw <= 1 ;
end

always @(posedge cclk)
begin
```

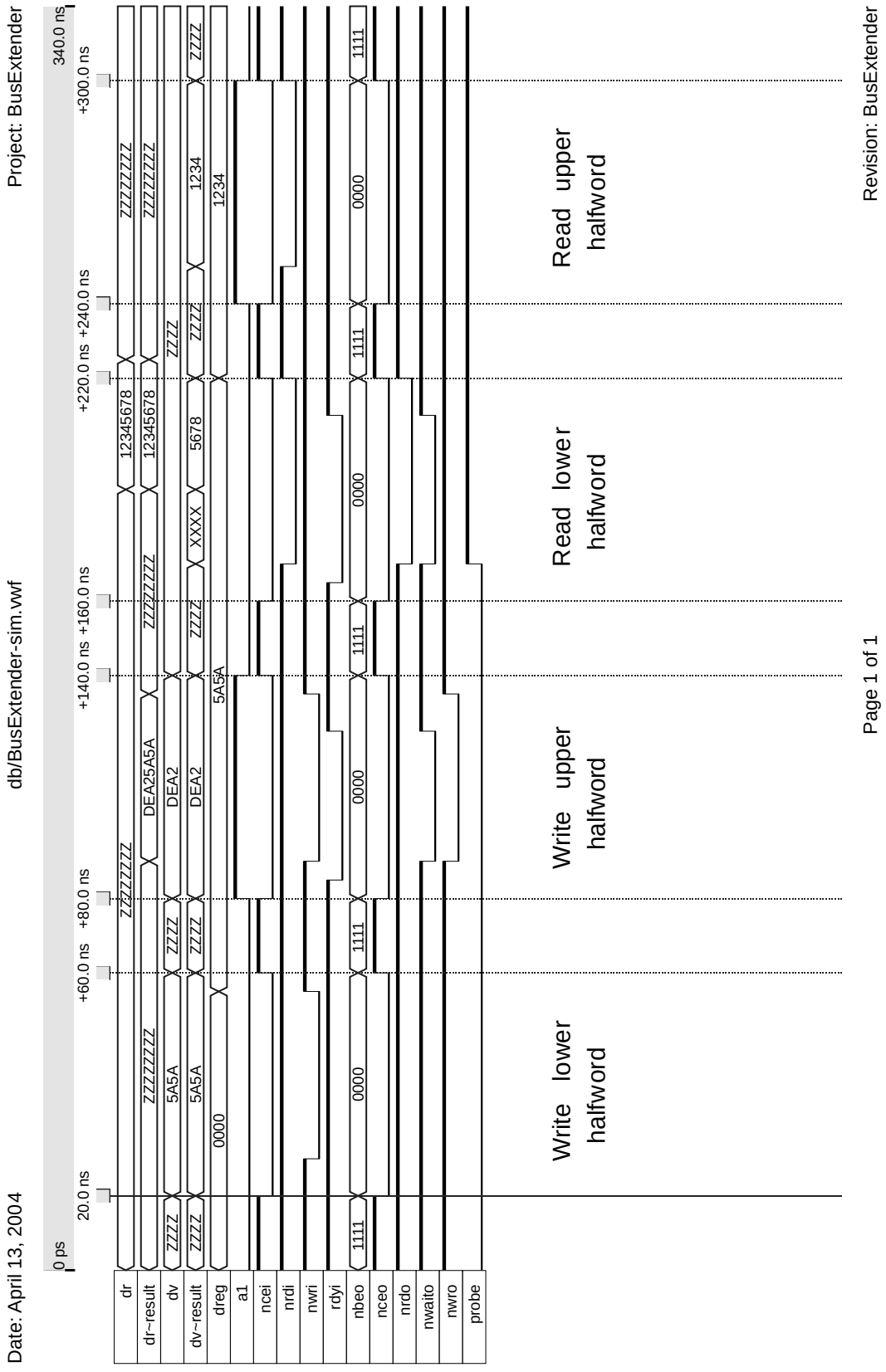
```
   if (rnw)
      dreg[15:0] <= dr[31:16] ;
   else
      dreg[15:0] <= dv[15:0] ;
end

assign dv[15:0] = ~cpuread ? 16'hz :
                  ~a1 ? dr[15:0] :
                  dreg[15:0] ;
assign dr[31:0] = cpuwrite_upper ? {dv[15:0],dreg[15:0]} : 32'hz ;

endmodule
```

2.4.2 Bus extender simulated timing diagram

Figure 2-5: Bus extender simulated timing diagram



Chapter 3 V850E/ME2 Application Test Board

We have built an application test board with the V850E/ME2 (called ME2-board). Its schematics are depicted in Chapter 6. This document does not cover the USB, serial interfaces and touch panel interfaces which the ME2-board provides, because they are currently untested. Therefore reuse the respective parts of the schematics with care. The 32-bit bus interface has been made compatible with the Ravin-E startware board (startWARE-GHS-RavinE), which is not covered by this document. Please check the startWARE-GHS-RavinE Users Manual (Doc. Nr. TPS-HE-U-6001) for details about that board.

The major building blocks of the ME2-board are the V850E/ME2 CPU, the Flash/SDRAM memory, the external bus drivers and the connector as well as the different voltage regulators and the reset generator. These building blocks are briefly described below.

U1 is the V850E/ME2 CPU. An 18.432 MHz crystal is connected to its built-in oscillator, so that an internal operating frequency of 8*18.432 = 147.456 MHz can be achieved. J1 is the CPU N-Wire connector which enables debugging through any of NEC's V850 emulators. The mode select inputs (MODE[1:0], JIT[1:0], SSEL[1:0] and PLLSEL) are connected to jumpers, so that any supported configuration can be chosen. DIP-switch S1 is connected to a few unused port pins and it is not dedicated for a specific purpose.

The 32-bit wide address/data-bus interfaces to the memory block and to the drivers for access to the Ravin-E board. The address lines are automatically properly multiplexed for access to the SDRAMs. Two parallel 16-bit wide memories are used for Flash as well as for the SDRAM. We use 256-MBit memories in either case, so that 64 MB Flash memory and 64 MB SDRAM are available. Due to internal restrictions of the V850E/ME2 address decoding, these sizes may not be completely accessible.
Different voltage regulators are implemented on the ME2-board. Switching regulator U13 generates a stabilized 5 V master supply voltage V_{DD50}, from which all other voltages are derived by linear regulators. U18 generates V_{DD33} and U11 generates V_{DD15} for the core supply. Each of them has shunt resistors in front of its input voltage pin, which reduce the input voltage and dissipate some of the power. That allows for a reduced heatsink area on the PCB. Heatsinks other than the PCB copper are not required as long as the load current on V_{DD33} does not exceed 700 mA and the one on V_{DD15} doesn't exceed 250 mA. U2 is a voltage reference for AD-converter. Four LEDs are provided to indicate the availability of the V_{DD50}, V_{DD33}, V_{DD15} and AV_{REF} voltages. Amplifying transistors are implemented for V_{DD15} and for AV_{REF}. V_{DD15} is too low to drive an LED and AV_{REF} should not be loaded excessively by a LED current.

U14 is a reset controller with a manual reset push button PB1. It supervises the V_{DD33} supply voltage and can generate an NMI before the reset occurs.
There are a few untested building blocks on the ME2-board. The analog inputs 0..3 are connected to a discrete external touch-panel interface. Analog inputs 4..7 are available at row-connector J3 and can be terminated by R2..R5 if unused. The USB function pins are connected to USB-connector U15. The circuit is copied from the V850E/ME2 user manual. The two serial ports of the ME2 device are connected via RS232-transceiver U20 to two external DSUB-9 male connectors.

Chapter 4 Software Description

4.1 Ravin-E Graphics Library

The Ravin-E graphics library (RGL) was originally written for the NEC MIPS RISC devices VR41xx. It has been ported to the V850E/ME2 basically just by re-compiling it with the V850E Green Hills tools. An os_sleep(n) function has been provided, which delays by roughly n milliseconds. It is used for timeouts and it need not be very precise, but if the CPU core frequency differs much from 150 MHz, it should be adapted accordingly. os_sleep has been added to rgl_custom.c. This is the file in which also the base address of the Ravin-E frame buffer (PhysFB) and the Ravin-E registers (PhysReg) must be adapted.
A detailed description of the RGL can be found in the “Ravin-E Graphics Library Manual” in the rgl\doc directory.

4.2 Display of PNG files

In order to display png files (Portable Network Graphics), we have ported the free PNG Reference Library libpng (www.libpng.org) to the V850. This library requires the zlib compression library (www.gzip.org), which has also been ported. These two libraries are documented on their respective websites. Calls to zlib functions are transparent and the libpng user need not bother too much about that zlib library. It should be noted, however, that a certain amount of heap space is required for both libpng and zlib. Also the stack size should not be too small, as these functions seem to use it extensively. They have clearly been written with personal computers in mind and are not optimized for the limited memory resources of embedded applications. Nevertheless there is a limited number of tuning possibilities by defining certain variables that control compilation of the libraries. See the respective documentation for details.

4.3 Demonstration Programs

Two rather simple demo programs are supplied along with this application note. **Datalogger** is an application, which displays a simple four channel datalogger grid on the background layer. This is simply a predefined image that is stored in a PNG-file and extracted once at initialization time into the frame buffer. Four traces are displayed on the foreground layer, which move from the right side to the left, so that the older values appear on the left and the newer values on the right side. The displayed values are generated from pseudo random numbers which are low pass filtered to make them look like real analogue input data.

Display of the trace lines makes use of Ravin-E's feature to move the viewport freely over the virtual display area. When the display line wraps over, Ravin-E does not actually display the image data from the subsequent line, but the data from the beginning of the current line. This feature permits the impression of a moving image, without actually copying data within the frame buffer. Only the start address of the viewport is constantly updated. In the case of the datalogger demo program, the right most column is updated in addition to the viewport address, as always new data shall be displayed.

The datalogger demo program requires very little CPU performance. Almost all CPU time is spent in the “os_sleep(20)” delay at the end of function main.

Animation is a demo program which displays a rotating image on the screen. This endless movie is simply made by displaying a sequence of 60 PNG images cyclically, so that the impression of a movie is generated. The images were produced by POVRay (www.povray.org) and ThumbsPlus (www.thumbsplus.com) was used to generate a common palette for all of them. A common palette is required to eliminate the temporal noise, which would otherwise occur due to the asynchronous update of the palette and the display data.

The animation is very simple and it requires the whole CPU time. There is no delay implemented to slow down the movement. An improvement of speed is possible in many ways. In the current implementation every single image is decompressed again before it is displayed. The most simple improvement at the expense of RAM space would be to decompress the images only once at initialization time and merely copy them to the frame buffer at run time. That would not only save the decompression time itself, but also the assembly time of the individual pixels. Also the actual data transfer would not be performed pixel by pixel but 32-bit wide, i.e. two or four pixels at a time. The performance and the required CPU time can be further improved by copying the decompressed individual images into Ravin-E's frame buffer to a location, which is not currently being displayed. Transfer of the image to the screen location would then be accomplished by a BITBLT command to Ravin-E. For the CPU that is a simple sequence of a few register write operations and as such it would virtually cost no CPU time at all.

Chapter 5 Performance Measurements

Semiconductor data sheets usually specify timing parameters under well defined conditions. These parameters are required to design a reliable system, but often they cannot be used to estimate the performance of a real system as they use idealistic assumptions. The system performance is usually limited by many factors, which may sometimes not be calculated or simulated.

Therefore it is useful to measure certain key performance values under real-life conditions. That is what we have done with the **benchmark** application, and the results are documented in this chapter.

The benchmarks runs on the V850E/ME2 board with the startWARE-GHS-RavinE board connected to it. The V850E/ME2 is clocked with 147.456 MHz, the code is executed from the internal instruction memory and data and stack are located into the internal data memory. The selected screen resolution is 800 × 600 pixel at 60 Hz frame rate and two display layers are enabled, one with 16 bit per pixel and the other one with 8 bit per pixel. In this configuration, the screen refresh uses approximately 25% of the available bandwidth between Ravin-E and its SDRAMs. This is an average bus load calculated for a whole frame and it includes the sync pulses, during which no data transfer takes place at all. The average data rate during the display of a scan line is about twice as high with short periods of essentially 100% bus load when a burst read is issued to fill the video output pipeline.

5.1 Data transfer rates between V850E/ME2 and Ravin-E frame buffer

This part of the benchmark measures the speed of word read and write transfers between the V850E/ME2 and the frame buffer. These figures become important when the CPU generates an image, rather than sending commands to Ravin-E to render it. For the timing of the sequential access, the benchmark executes a number of read/write accesses to subsequent frame buffer addresses. That is similar to the case, when a predefined image (e.g. PNG image) is decompressed and transferred to the frame buffer. Both the CPU and Ravin-E can make use of burst accesses whenever applicable.

For the random access measurements, the CPU accesses words within a predefined address range in a pseudo random order. In most cases here, burst accesses have no advantage, actually the may reduce the access times tremendously, because most of the transferred data may be discarded. This effect can clearly be seen in the case of random read operations.

Table 5-1: Random read operations

Operation	Time per 32-bit word access [ns]
sequential read	393
sequential write	288
random read	2346
random write	288

The measured values vary slightly between multiple measurements. That is due to the asynchronous screen refresh that takes place constantly in the background.

5.2 Vector drawing speed

To measure the vector drawing speed, we draw long lines in different angles with the rgl_DrawLine function, which is setup to use the Ravin-E drawing engine. A total of 50 lines are drawn on the 16-bpp layer and 49 lines are drawn on the 8-bpp layer. All lines start from the top left to the top right of the screen and they end at the bottom right to the bottom left. This is just to have different line lengths and different angles. On the 800 × 600 screen, the line lengths vary between 600 and 1000 pixels. These are the results of the timing measurements:

Table 5-2: Vector drawing speed timing measurements

Operation (600 ~ 1000 pixels)	Average drawing time per line [µs]
8-bpp Draw Line	47.5
16-bpp Draw Line	27.9

5.3 Filled rectangle drawing speed

The rectangle drawing speed is measured by calling the rgl_DrawBltFillRect function a few hundred times and then calculating the average execution speed for drawing one rectangle. We have chosen arbitrarily a size of 30 × 10 pixels and the position of each rectangle on the screen is random. Again we measured the speed for an 8-bpp and for a 16-bpp layer. Here are the results:

Table 5-3: Filled rectangle drawing speed timing measurements

Operation (30 × 10 pixels)	Average drawing time per rectangle [µs]
8-bpp DrawBltFillRect	7.3
16-bpp DrawBltFillRect	9.4

Chapter 6 Schematics of V850E/ME2 Application Test Board

Figure 6-1: V850E/ME2 Board

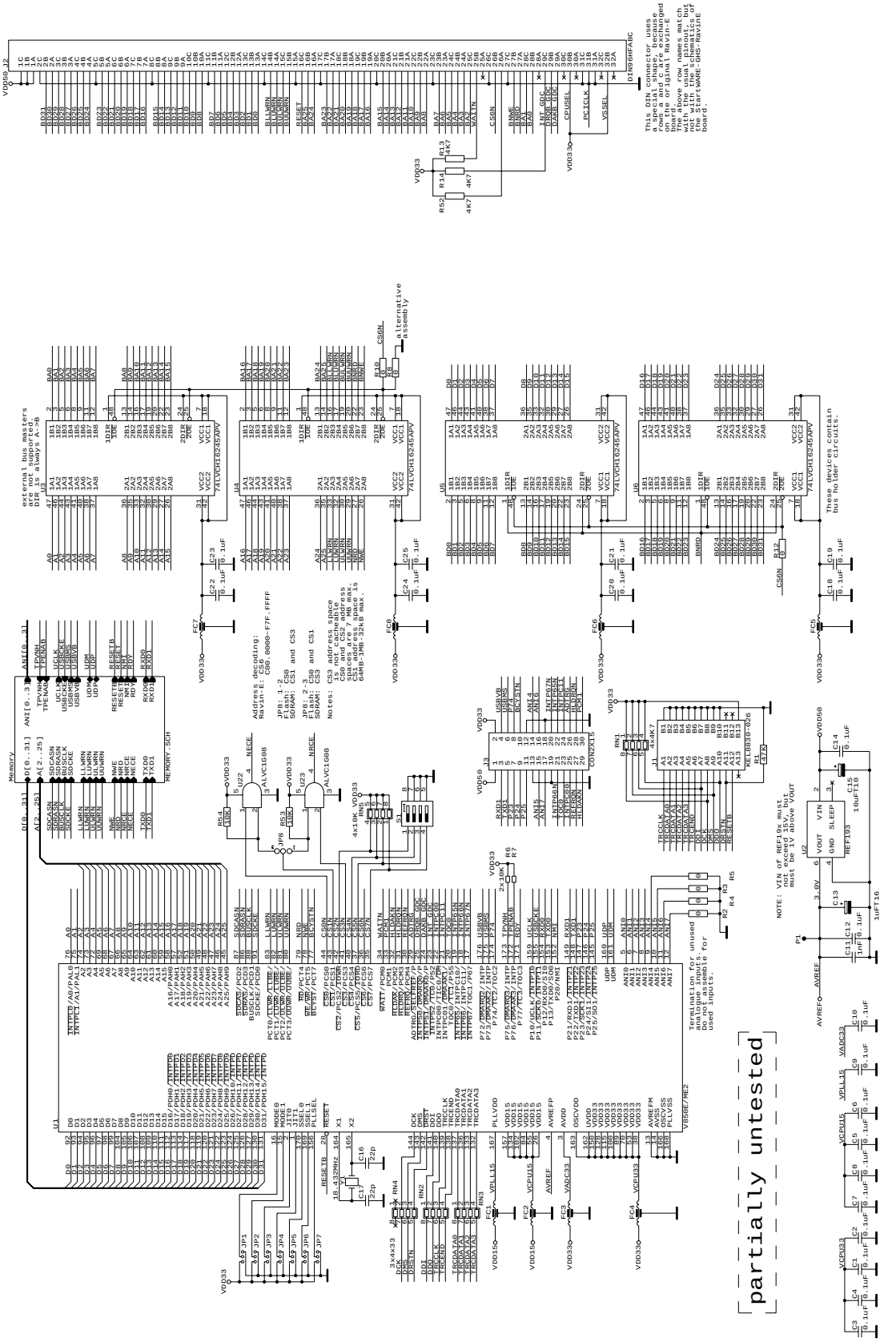
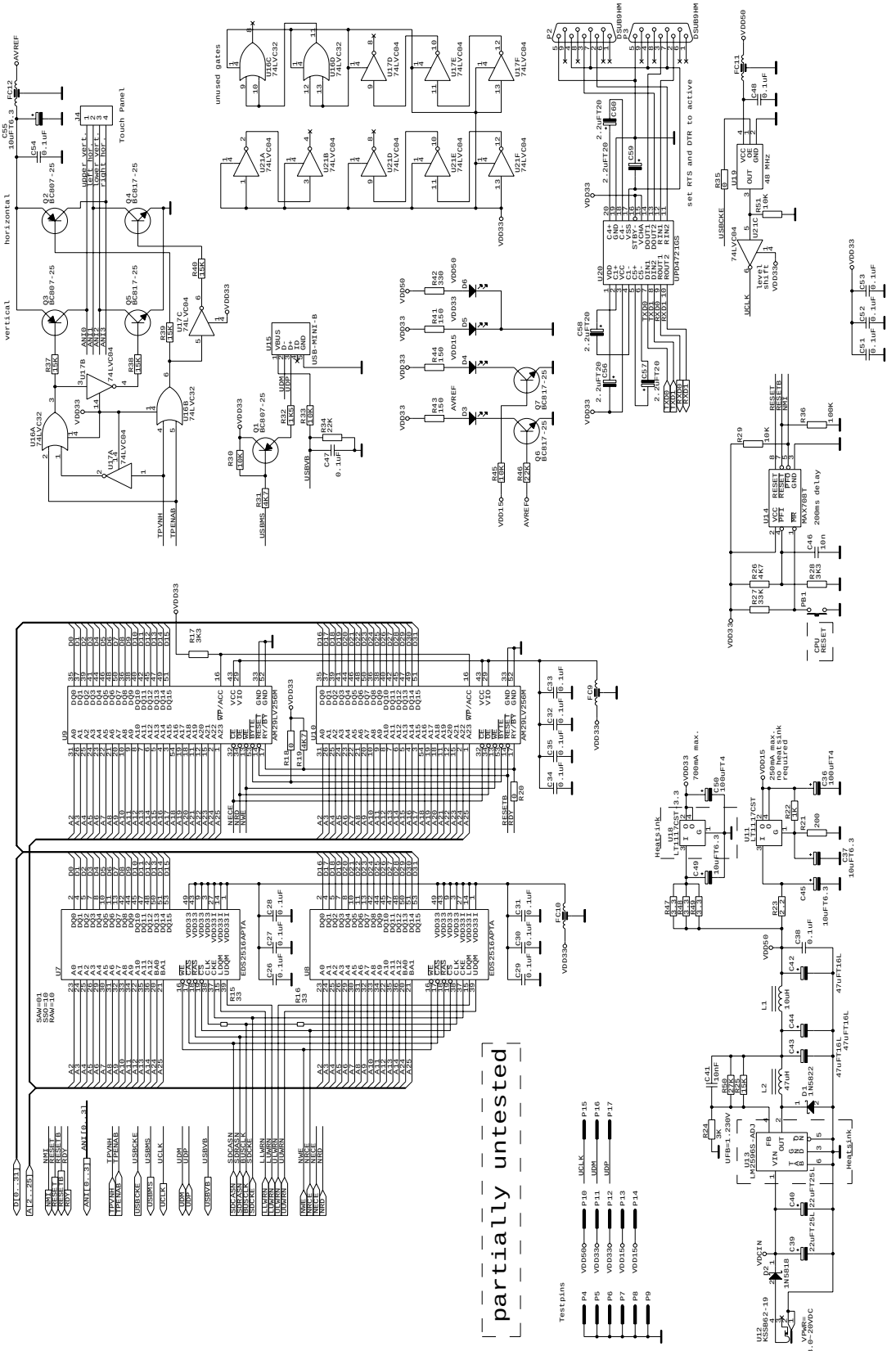


Figure 6-2: SDRAM /Flash Memory, Power, USB, Reset



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