Expanding the RC3233x Address Lines

Application Note
AN-305

Notes

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Revision History

August 8, 2001: Initial publication.

October 18, 2002: Changed device designation to RC3233x which includes 3 devices: RC32334, RC32333, and RC32332.

Background

The RC3233x series are integrated communications processors that combine a 32-bit MIPS instruction set architecture (ISA) CPU core with a number of on-chip peripherals to enable direct connection to boot memory, main memory, IO, and PCI. The RC3233x also includes system logic for DMA, reset, interrupts, timers and UARTs. The RC3233x series integrate all of the peripherals commonly associated with an embedded system to reduce real estate consumption, design time, and cost.

This application note describes how to expand the RC3233x address lines for addressing large capacity memory mapped peripherals. The RC32334 has 26 address lines, which it uses to map a maximum address space of 2^26 memory locations (64MB). The RC32332 and RC32333 have 23 address lines. This restricts the maximum address space to 2^23 memory locations (8MB). For some specialized applications, this amount of memory space is inadequate. Because the SDRAM main memory is accessed via row-column addressing, this 64MB/8MB memory limitation does not apply.

Description

The RC3233x series drive the full 32-bit address of the next transaction on the data lines in the first clock cycle of all memory transactions. When the debug signal *debug_cpu_ads_n* is asserted, it indicates that either a CPU or a DMA transaction is beginning and that the *mem_data[31:0]* bus contains the current block address.

Therefore, it is possible to use *debug_cpu_ads_n* to latch in the full 32-bit address. Note that ADS is driven for an entire cycle and data should be latched in the middle of its valid window (see Figure 1). As a result, to be effective, *debug_cpu_ads_n* must be used as an enable to a negative edge clocked flip-flop which is clocked off the system clock *cpu_masterclk*.

Figure 1 describes the timing among control signals and Figure 2 shows an example of one possible hardware implementation.

Notes

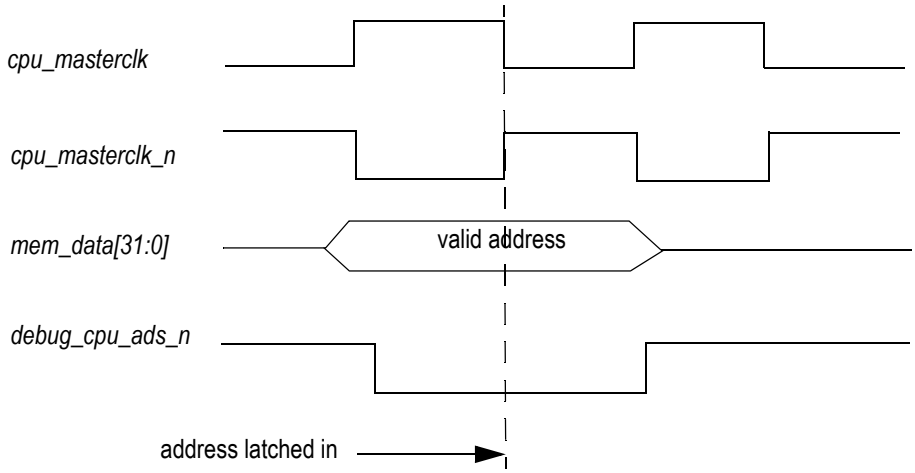

Figure 1 Control Signal Timing

CLOCK = *cpu_masterclk*

ENABLE = *debug_cpu_ads_n*

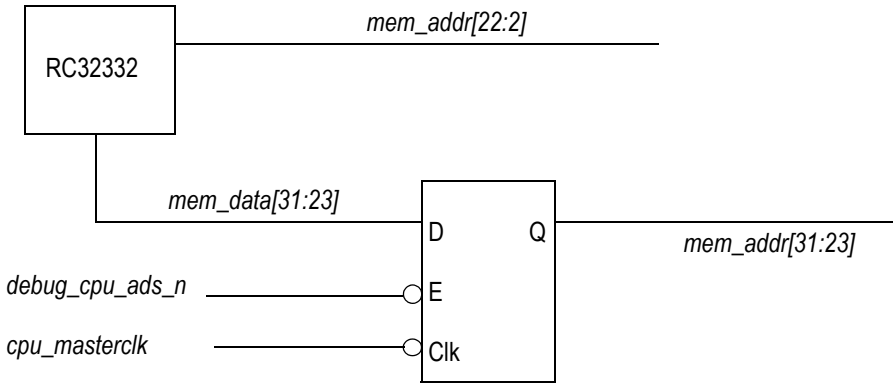

Figure 2 Hardware Implementation Example

To address a device (memory/IO) which requires more than 26 bits (RC32334) or 23 bits (RC32332/RC32333) of address lines, the 32 bits available through the data bus can be used as shown in Figure 2. This diagram is specific to the RC32332/RC32333. However, the RC32334 is nearly identical, requiring three fewer latches. This example is based on a flip-flop enabled by the assertion of the *debug_cpu_ads_n* signal and clocked by the negative edge of the *cpu_masterclk* signal. The resulting newly-created address lines can then be concatenated with the existing address lines to create an address bus of the required width.