Notes

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Introduction

IDT uses the 256 PBGA package for several of its products. Although creating an optimal layout with a PBGA package is more challenging than with peripherally leaded packages such as the PQFP, this extra effort is usually more than offset by the many benefits associated with the package.

- **Superior packaging density:**

  The BGA package is extremely dense. The balls on the BGA package are spaced 1mm on center. The 256 BGA package is composed of a 16 x 16 array of solder balls. The total package measures 17mm square, and it has a maximum installed vertical profile of 3.5 mm.

- **Superior thermal & electrical characteristics:**

  The BGA package has extremely low inductance as compared to leaded chip carriers such as the PQFP. This allows for faster I/O response. The thermal characteristics of the part are also much better. This allows the part to run faster and still maintain a lower junction temperature than other packages such as the PQFP.

- **Lower Profile:**

  The BGA package can be mounted in many places where other chip carriers cannot. The BGA package often allows the designer to mount the components on the backside of the board even when clearance is extremely limited.

Layout Issues

The main issues in the layout arise because of the ball density of the PBGA. The routing under the package is extremely dense, and it requires a large amount of solder in a very tight space to attach the part to the board. The layout designer needs to be very careful when selecting pad geometries, locating vias, and routing the inner signal rows outward to mitigate the risks inherent in working with high density PBGAs such as IDT's.

Pad Layout

The layout feature which most critically impacts the solderability of the part is the pad geometries used. IDT recommends a 22 mil pad with 5 mil traces of 1 ounce copper, and a minimum 5 mil airgap for the PBGA256 part. IDT also strongly recommends using NSMD (non-soldermask defined) pads. It might be possible to use SMD (soldermask defined pads) with the 256 PBGA, but there are significant drawbacks associated with their use. The main difference between the two types of pads is that the copper surface for the SMD pad is much larger. For the perfect case, both methods would produce identical results. However, because of solder mask registration error, i.e. mismatches in alignment between the solder mask and the PCB, the area of the copper pad for the SMD pad must be substantially larger than that of the NSMD pad. In both cases, the target pad size is 22 mils. However, since a typical solder mask registration error is +/- 3 mils, the solder mask must be 3 mils larger than NSMD pads on all sides. This means that the NSMD process requires a 28 mil solder mask opening. Since the SMD pad is defined by the solder mask, and the pad size needs to be 22 mils, the opening in the solder mask for the SMD pad must be exactly 22 mils. However, since there has to be copper under this opening, and the solder mask may miss by 3 mils in any direction, the copper pad must be 22 mils + 3 mils on each side for a total copper pad size of 28 mils. The two methods and the pads that they produce are graphically depicted in Figure 1 for comparison.

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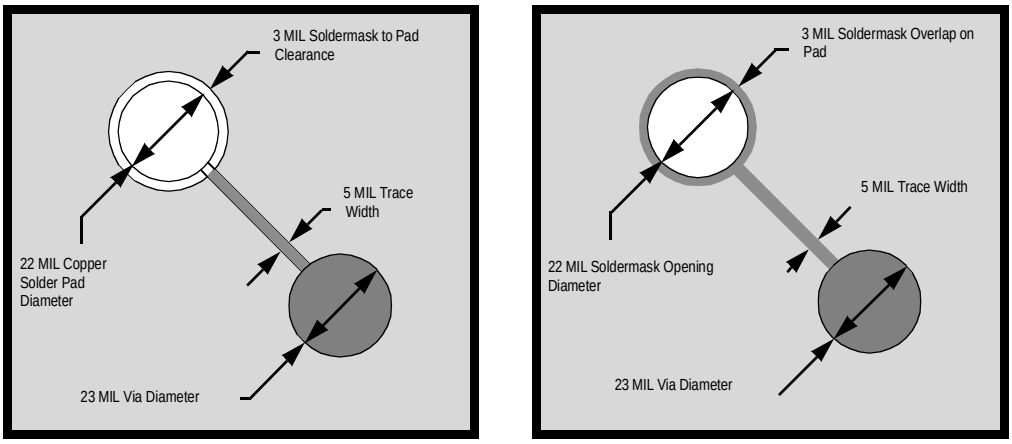


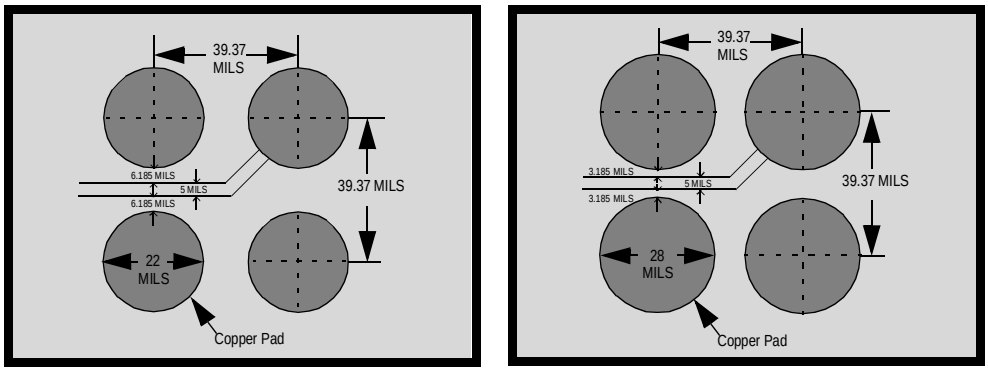
NSMD Solder Pad **SMD Solder Pad**

Figure 1 NSMD Solder Pad

Since the balls on the IDT 256 BGA part are only 1 mm apart (39.37 mils), there is very little room for routing between the pads. As indicated previously, IDT recommends a 5 mil trace with 5 mil airgap on each side.

If we use the NSMD process, the gap between the two pads will be 7.37 mils, calculated as follows: 39.37 mils, minus 22 mils (11 mils for 1/2 of a pad on each side), minus another 10 mils of airgap. This leaves enough room for the 5 mil trace to slip through.

If we use the SMD process, the copper pad for each ball is 28 mils, with each pad having a radius of 14 mils. The gap between the two pads will be 1.37 mils, calculated as follows: 39.37 mils, minus 28 mils for 1/2 of two pads, minus another 10 mils of airgap. There is insufficient routing space for a 5 mil trace. Therefore, it is not possible to route any wires between SMD pads, and more layers are required to escape the PBGA. Both scenarios are depicted in Figure 2.



NSMD Solder Pad **SMD Solder Pad**

Figure 2 SMD Solder Pad

When using NSMD pads, IDT generally tapes out its solder masks and pads with identical dimensions. The PCB manufacturer is then free to enlarge the solder mask opening to account for whatever registration error that manufacturer generally experiences. The end result is an optimal design which is portable between board manufactures.

VIA Layout

IDT recommends the use of 23 mil vias with a 10 mil finished (after plating) diameter. There is no reason why the board manufacturer cannot plate these closed if necessary. The solder mask must completely cover the vias. If it does not, there is a danger of solder wicking up the open via barrel and shorting two PBGA pads together. The vias should be located in the center of an X formed by the four pads which bound

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the via. This layout and the resulting spacing is depicted in Figure 3. Note that this spacing only holds true for the NSMD pads recommended by IDT. The SMD via size will be the same, but the clearances will be reduced by 2 to 3 mills from each of the four adjacent pads to the vias.

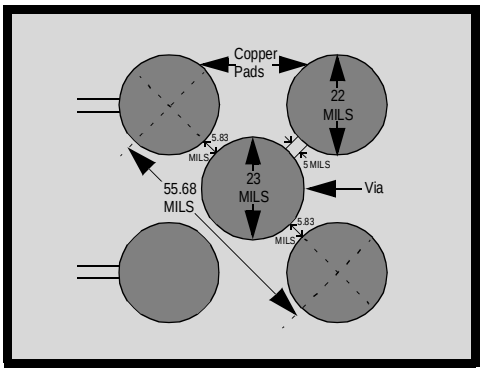

Figure 3

Escape Routing

The ball density and array structure creates a problem because it makes escaping the inner balls a bit challenging. IDT attempts to mitigate the impact of these imbedded balls by restricting active signals to the outer four rows. IDT accomplishes this by assigning all of the inner balls in a 6 x 6 matrix as grounds. The next ring out is comprised of 28 pins, and it forms the power distribution ring. This configuration is depicted in Figure 4.

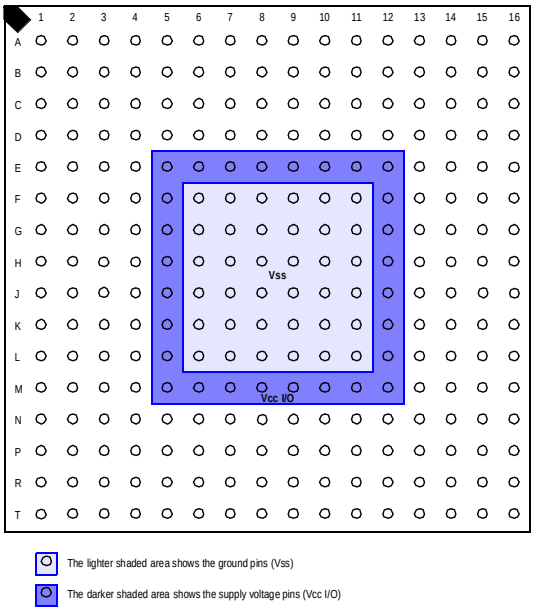

Figure 4

Since the power and ground pins can be connected to the power and ground layers, they do not need to be escaped. This leaves the layout designer with only the outer four signal layers to contend with.

In order to minimize the required layer count for PBGA based designs, the PBGA sections should ideally be hand routed. An autorouter can be used once the PBGA array is successfully escaped. Theoretically, because of the way the signal pins are clustered on the outside four rows, this PBGA can be completely escaped using only two signal layers.

The outer two rows can be escaped on the top layer as depicted in Figure 5. The inner two rows can be dropped down through vias and escaped on a lower layer as depicted in Figure 6.

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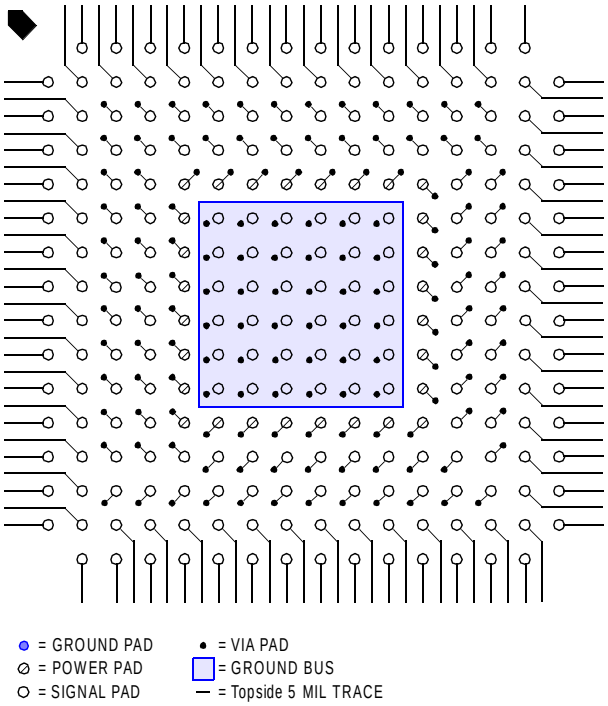

Figure 5 Top Layer Metal

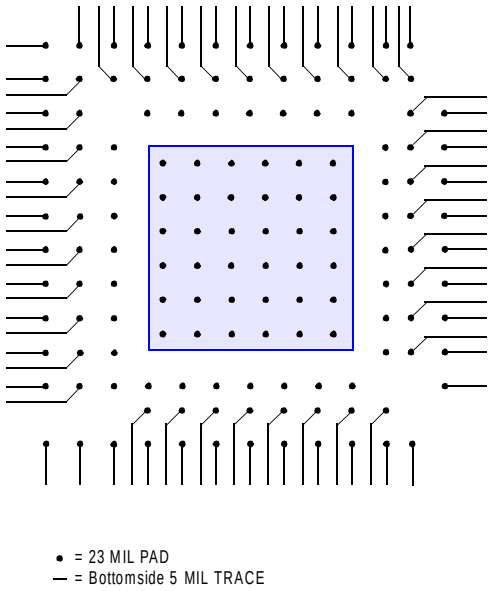

Figure 6 Bottom Layer Metal

Once the signals are all brought to the outside periphery of the PBGA they can then be connected to a via array. From this point onwards, an autorouter should be able to handle the routing. Although the BGA can be theoretically escaped using only these two layers, in actual practice, many of the signals will eventually need to cross. Depending on the application and component placement, it is usually possible to route this board using a six layer stackup-one power, one ground, and four routing layers. However, pushing the layer count to a ten layer stackup--two power planes, two ground planes, and six signal layers, significantly simplifies the task.

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Soldering

The PBGA package is highly reliable if correctly soldered. This package has been widely accepted within the manufacturing community, and most board assemblers have no problem working with it. If a problem occurs, it is usually due to either:

- *incorrectly leveled or contaminated mounting surfaces or*
- *an incorrect thermal profile.*

X-ray techniques are widely used to verify proper soldering and should be used to spot-check the initial runs. There are two types of X-Ray systems in use by manufacturers. The most common type is a vertical system. While this type of X-raying eliminates the possibility of shorts between the individual solder balls, it does nothing to ward against voids and opens. Since the solder balls are attached to the package and are quite dense, they block the X-rays from penetrating through them. As a result, an open or partially soldered pad looks identical to a properly soldered pad when X-rayed from above or below. A vertical X-Ray of a PBGA 256 is depicted in Figure 7.

The other type of X-Ray equipment shoots the package at an angle. It creates a sectional view of the balls. This system can detect opens as well as shorts. However, the system is relatively expensive, and very few manufacturers have this capability.

The vertical X-Ray system is usually sufficient. If there is a persistent problem with opens on a particular type of board, it is usually due to an incorrect thermal profile.

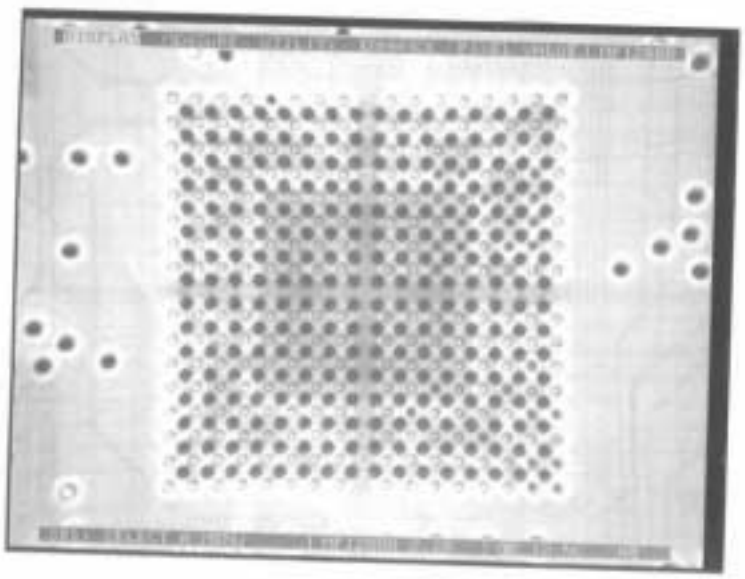

Figure 7 PBGA 256 Package X-ray

The heat for soldering the part must be transmitted through the package because there is no way to directly apply heat to the inner balls of the device. And it is not unusual for the assembly house to be too conservative initially.

In the event that a board fails because of opens, it is often possible for the board house to correct this problem by re-flowing the solder. If reflowing corrects the problem, then the board house's temperature profile is incorrect for the part, and they need to increase the heat applied during the soldering process.

Surface Preparation and Leveling

The PBGA package is not tremendously susceptible to problems with pad leveling as the solder balls on the package place a large amount of solder at the contact point. However, IDT does specify some amount of maximum warpage of the board. Generally, IDT will set the value at .007” of warp per inch. IDT specifies

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that the final manufactured boards be either HASL (hot are soldering leveled) or gold flashed. The HASL method is generally used for low-volume board runs. IDT generally specifies that the thickness be from 0.1 to 1 mil. The gold flash method is used for higher volume production runs. In these cases IDT specifies 2 to 8 microinches of flashed gold.

Device Alignment

The PBGA device is somewhat self-aligning. Once the solder balls all reach the eutectic point, the surface tension of the molten solder will pull the part into alignment even if the balls are up to 50% offset from the center of the pads. This means that the required alignment accuracy for the part is +/- 11 mils. However, in practice, it is best to be as precise as possible.

Since the balls under the device are not visible, it is necessary to put some location markers on the board to help the pick-and-place machinery align the package. These reference marks are called fiducials. All of IDT's evaluation and reference boards have these marks etched on the external board layers to guide the pick-and-place equipment when working with the PBGA.

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