Interfacing the IDT RC32355/ RC32351 to the PCI Bus Using the V3 V320USC

RC32355/RC32351 Application Note AN-262

Notes

By Seroj Babaian

Revision History

April 19, 2001: Initial publication.

December 6, 2001: Added RC32351 to description.

Introduction

The IDT RC32355/RC32351 is a 32-bit high performance integrated communications processor targeted for various embedded communications applications. The RC32355 is capable of operating up to 150 MHz (133 MHZ for RC32351) Pipeline Frequency and 75 MHz (66 MHz for RC32351) System Bus Frequency. The RC32351 is capable of operating up to 133 MHz Pipeline Frequency and 66 MHz System Bus Frequency. Both are IDT's third integrated MIPS processor based on the RC32300 CPU core. The RC32355/RC32351 implements common on-board system peripherals such as an SDRAM Controller, Timers/Counters, DMA, UARTs, I^2C (not available in the RC32351), and General Purpose IOs. It also incorporates four communications-specific peripherals, namely, Ethernet, ATM, USB, and TDM (not available in the RC32351). The RC32355/RC32351 is capable of interfacing directly to external peripherals including Flash, ROM, EPROM, Serial EEPROM, and SRAM.

For embedded communications applications demanding flexibility, support inside the system for a PCI bus interface is essential. It offers direct and easy access to a broad range of graphical, networking, and data storage peripherals. This application note will help the user to achieve this level of system integration with the use of the V3's V320USC (Universal System Controller) and a minimal amount of external (glue) logic. This application note points out special features of the V320USC as well as considerations for a seamless interface to maximize performance of the entire system. It also describes in detail how to interconnect the various control signals on the two devices.

The V320USC

The V320USC is a high integration, low cost PCI system controller.

Features:

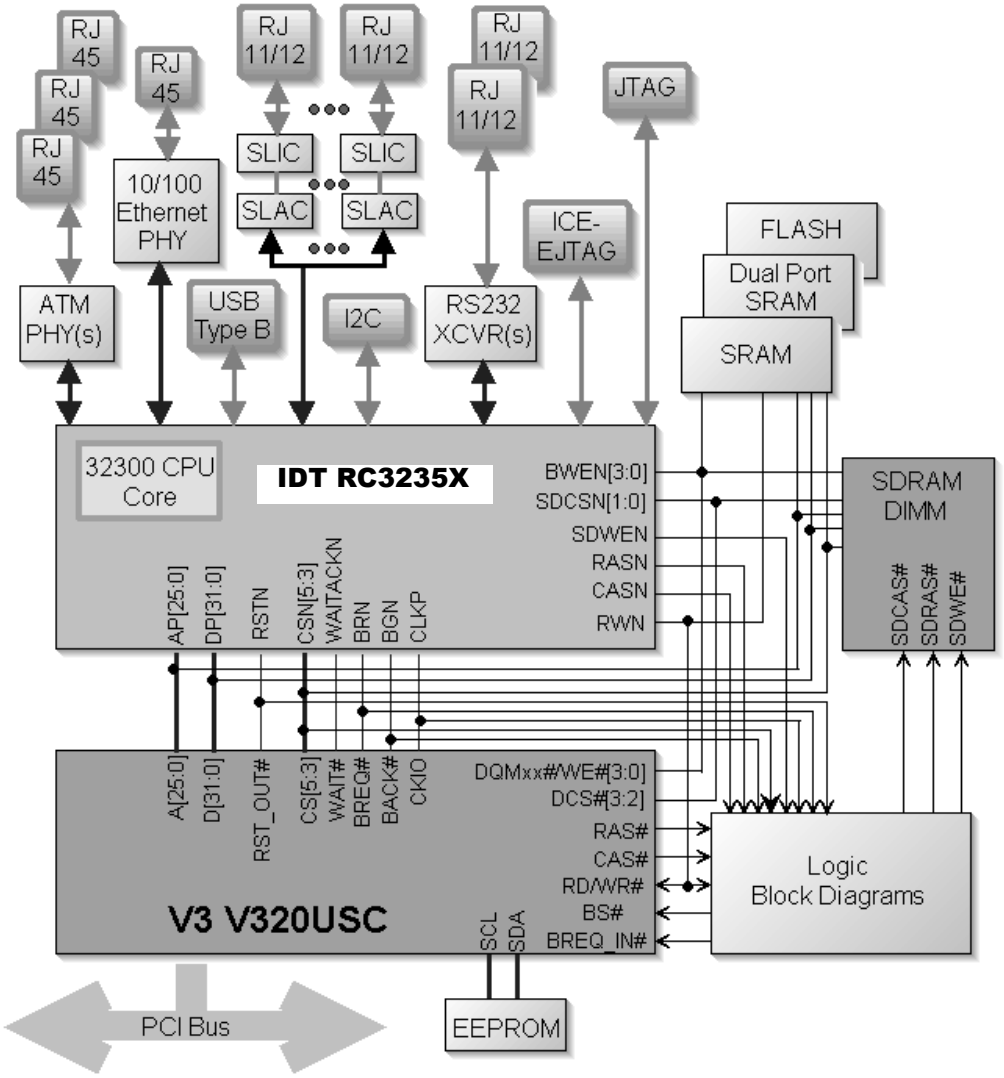
- **Fully compliant with PCI Local Bus Specification v2.2, up to 33 MHz**
- **Configurable for PCI Primary Master, Bus Master, or Target Operation**
- **Hot Swap Ready, including on-chip bias voltage, per PICMG Hot Swap Specification v2.1**
- **PCI Bus Power Management per specification v1.0**
- **Capable of accepting an Expansion ROM**
- **Initialization through local processor, PCI, or serial EEPROM**
- **SDRAM Controller with support for Enhanced SDRAM**
- **Two independent, advanced DMA Controllers**
- **Two 32-bit Timers**
- **CPU Local Bus up to 75 MHz**
- **I_2O Ready Address Translation Unit and Messaging Unit**
- **External Interface to common Non-Volatile Memories**
- **Serial Interface to EEPROM**
- **Up to 1 Kbyte of continuous Burst access to (E)SDRAM from PCI bus**

Notes

- Industrial Temperature range (-40C to +85C)
- 208 PQFP package

Block Diagram

Note: TDM and I^2C are not available on the RC32351.



Special Features

Two special features are worthy of note. First is the direct access from the V320USC to the RC32355/RC32351 local SDRAM. The RC32355/RC32351 and the V320USC share the memory and peripheral interfaces which are referred to as the External Interface in this application note. Even though the RC32355/RC32351 is the device with the highest priority on the External Interface, the architecture is designed such that both devices may burst from/to the SDRAM directly. Other peripherals may also be accessed, independently, from both devices. Therefore, while the RC32355/RC32351 and the V320USC both implement powerful DMA Controllers, they are not necessary for transactions between each other. The RC32355/RC32351 may DMA from the SDRAM to the V320USC. But another option, with higher performance results, would be to request the V320USC itself to move the data from/to the SDRAM. This would alleviate approximately half of the cycles associated with an external DMA operation between the RC32355/RC32351 and the SDRAM/V320USC.

Notes

The V320USC has two powerful DMA Controllers and they both are capable of moving PCI data to/from the SDRAM. While in Master Mode on the PCI Interface, the V320USC may write and read from the PCI Interface directly to/from the SDRAM. While in Target Mode on the PCI Interface, the external PCI Master may conduct Target Reads/Writes directly through the V320USC to/from the SDRAM.

The second special feature of the V320USC is the FIFOs used to accommodate Burst Transactions on the External and PCI Interfaces. These FIFOs can simultaneously fill and drain, allowing for long sustained Burst lengths that exceed the size of the memory buffer.

Special Considerations

The IDT RC32355/RC32351 and the V3 V320USC combine to provide a powerful communications based PCI system solution. Specific functions, such as arbitration and SDRAM control, require special consideration when coupling the RC32355/RC32351 and the V320USC.

Arbitration

The V320USC is capable of emulating multiple CPU bus architectures, such as the SH3/4. The SH3/4 mode is best suited to the RC32355/RC32351's External Interface. The V320USC, while in the SH3/4 mode, is capable of multiple arbitration methods.

The first approach involves interfacing to a CPU with a three-signal arbitration system. The three signals are described as "Bus Request", "Bus Grant", and "Bus Interrupt Request". The actual signal names will be discussed later in this application note.

The Bus Request signal is used to begin the arbitration cycle. The V320USC will request the External Interface from the CPU by asserting the Bus Request. If the CPU has a pending transaction on the External Interface, it will complete it before granting the bus to the V320USC. Otherwise, it will grant it immediately.

The CPU will grant the External Interface by asserting the Bus Grant. The V320USC will wait until the Bus Grant is asserted before conducting any transactions on the External Interface. The V320USC will conduct transactions on the External Interface once it has been granted.

If the CPU requires access while it has granted it to the V320USC, it will request back the External Interface via the Bus Interrupt Request signal. The V320USC will end whatever transaction it was conducting, prior to the Bus Interrupt Request, and relinquish the External Interface back to the CPU. The V320USC will relinquish the External Interface by de-asserting the Bus Request. The CPU will respond by de-asserting the Bus Grant, followed by de-asserting the Bus Interrupt Request.

The second approach involves interfacing to a CPU with a two-signal arbitration system. The two signals are described as "Bus Request" and "Bus Grant". The actual signal names will be discussed later on in this application note. The Bus Request and Bus Grant is identical to the approach discussed in the previous paragraph, but the bus interrupt arbitration is different. In this approach, the CPU will request back the External Interface if it requires access by de-asserting the Bus Grant. The V320USC's state machine can only relinquish the External Interface if the CPU asserts Bus Interrupt Request (refer to stepping information on V320USC). A small amount of Logic is required to generate the Bus Interrupt Request signal to the V320USC from the Bus Grant being de-asserted. The V320USC will end whatever transaction it was conducting, prior to the Bus Interrupt Request, and relinquish the External Interface back to the CPU. The V320USC will relinquish the External Interface by de-asserting the Bus Request. The Logic will de-assert the Bus Interrupt Request a clock cycle after the V320USC de-asserts the Bus Request.

The RC32355/RC32351 incorporates a two-signal arbitration method. Therefore, the two-signal approach is implemented in this application note.

SDRAM Controller

Both the RC32355/RC32351 and the V320USC incorporate SDRAM Controllers. They share a number of control lines as well as generating refresh cycles. The specific control signals are discussed later in this application note. Special consideration is required for the two devices to share the SDRAM interface. That

Notes

is in relation to three control signals; Column Address Strobe, Row Address Strobe, and Read/Write Enable. The three signals have critical timing requirements and, therefore, require some logic to allow both devices to access the SDRAM without affecting the overall performance of the system.

The Column Address Strobe and Row Address Strobe should be isolated from the two devices to the SDRAM to insure proper high-speed operation.

The Read/Write Enable to the SDRAM is unique from the RC32355/RC32351 and shared on the V320USC. The RC32355/RC32351 sources a Read/Write Enable to all the devices on the External Interface, including the V320USC, as well as a separate one to the SDRAM. The V320USC contains only one Read/Write for all devices on the External Interface, including the RC32355/RC32351, as well as the SDRAM. It is recommended that a small amount of Logic be incorporated to isolate the two devices from the SDRAM with respect to this signal. The Logic and the control signals are all outlined in this application note.

SDRAM Controller Refresh

The SDRAM requires refresh on a periodic basis. Both the RC32355/RC32351 and the V320USC is capable of conducting the refresh cycles. It is preferable, with respect to the complexity of the design, to have only one device control the refresh of the SDRAM. That device will be the RC32355/RC32351 because it is the predominant user of the SDRAM interface. Therefore, the RC32355/RC32351 will be required to have a method of interrupting the V4320USC when a pending SDRAM refresh is required. This interrupt method is outlined in the section “BREQ_IN#-Bus Request Input-Input” on page 13.

Architecture

The IDT RC32355/RC32351 is a high performance MIPS based 32-bit CPU with many peripherals integrated on-chip. The device incorporates a highly intelligent DMA engine that can move data between any on-chip or off-chip peripherals and the main memory without any restrictions on data alignment, endianess, or size.

The V3 V320USC shares the External Interface with the Flash/ROM/SRAM/SDRAM or any other device the user chooses. It is a high performance PCI adapter that can accommodate a 32-bit, 33 MHz PCI Interface along with a 32-bit CPU interface and memory devices. The V320USC is also capable of moving data from/to the External Interface to/from the PCI Interface with its on-chip DMA Controllers. The advantages and features of both devices can be fully realized, when necessary steps and precautions are taken. This section of the application note dives into the details of the implementation and the control signal connections between the RC32355/RC32351, V320USC, and the SDRAM.

V320USC Bus Mode Used

The V320USC is capable of multiple bus modes of interconnect to a 32-bit CPU interface. The particular interface chosen for the RC32355/RC32351 is the “SuperH Local Bus Mode-SH3”. This bus mode allows the RC32355/RC32351 to closely match the interface of the V320USC except for some signals that require special attention, in regards to the SDRAM and inter-device transactions. The difference between the SH3 and SH4 Modes are how the WAIT#/RDY# signal is implemented. The SH3 Mode uses WAIT# and the SH4 Mode uses RDY#. *(See the section* “V3 V320USC Control Signal Connections” on page 12*.)*

Signal Name	Signal Description
AP[25..0]	Address Bus
DP[31..0]	Data Bus
BWEN[3..0]	Byte Write Enables
OEN	Output Enable
RWN	Read-Write Enable

Table 1 IDT RC32355/RC32351 Local Bus Tri-State Signal List (Page 1 of 2)

Notes

Signal Name	Signal Description
CSN[5..0]	Chip Selects
RASN	SDRAM Row Address Strobe
CASN	SDRAM Column Address Strobe
CKENP	SDRAM Clock Enable
SDWEN	SDRAM Write Enable
SDCSN[1..0]	SDRAM Chip Selects
BOEN[1..0]	Buffer Output Enables
BDIRN	Buffer Direction

Table 1 IDT RC32355/RC32351 Local Bus Tri-State Signal List (Page 2 of 2)

Local Bus Arbitration

Introduced earlier in the "Special Considerations" section of this application note but going into more detail here, the RC32355/RC32351 and V320USC arbitrate for the External Interface via a "Request/Grant" arbitration. The RC32355/RC32351 is the Master of the bus unless the V320USC requests it. If the RC32355/RC32351 has no pending transactions of higher priority, it will respond to the assertion of the Bus Request signal (BRN) by relinquishing ownership of the memory (SDRAM) and peripheral bus (External Interface) by asserting the Bus Grant signal (BGN) and simultaneously tri-stating the SDRAM and External Interfaces. Once the V320USC has been granted the interface, it is then considered the Master of the External Interface and may conduct transactions directly to the peripherals on the External Interface, including the SDRAM/ Flash/ ROM/ SRAM or any other device residing on the External Interface. *(*See Table 1.*)*

V320USC Configuration Pins

The Mode pins for the V320USC are set to "HLL" ("Modes[3..0]") in order to select a "SH3" Mode of operation. The Mode Configuration pins are strapped to either Vcc or GND and cannot be modified during operation. *(*See Table 2.*)* These values are sampled during Reset and are used to configure the internal State Machine of the V320USC.

CPU Interface Modes of V3230USC			
Mode bit 2 Pin 55	**Mode bit 1 Pin 54**	**Mode bit 0 Pin 202**	**Description**
SYSCMD7	SYSCMD8	H	MIPS with 9 bit SYSCMD
H	H	L	MIPS with 5 bit SYSCMD
H	L	L	SH3, **RC32355/RC32351 Mode**
L	L	L	SH4
Others			Reserved

Table 2 V3 V320USC Configuration Pins

The V320USC has three buses (PCI, Local, and M) to enable it to communicate to a number of devices. The PCI Bus signals are, by their names, the ones that are required to conduct transactions on the PCI bus and heretofore addressed as the PCI Interface. The Local Bus is the interface to the Local Processor (79 RC32355/RC32351). The M Bus is the interface for all peripherals and Memory. For the SH3 Mode of Operation, the M Bus and the Local Bus are combined into one bus, heretofore addressed as the External Interface, which is common to both the RC32355/RC32351 and the V320USC.

Notes

V320USC Initialization

The Initialization Mode, of the V320USC, is selected by setting the appropriate Mode Pins of the device. The internal registers are configured by one of these initialization modes. The initialization of the internal registers is conducted after reset. The V320USC may be initialized by one of three ways: via the PCI Interface, via the External Interface (RC32355/RC32351), or via a Serial EEPROM. The initialization mode is accomplished by strapping certain pins on the V320USC to given states. *(*See Table 3*).*

V320USC Local Processor Initialization

The Local Processor Mode is selected when the SDA pin (pin number 197 in the *V320USC Datasheet*) is sensed as being high and not connected to a Serial EEPROM.

When this mode is selected, the CFG_RETRY bit in the PCI_BUS_CFG Register (Offset 05Ch in the V320USC User's Manual) will be set until the V320USC is finished being initialized by the Local Processor (RC32355/RC32351). This bit is set in order for PCI transactions to be retried until the V320USC is finished being initialized. Once the initialization is complete, the bit is cleared so that PCI transactions may be conducted.

The RST_OUT bit in the System Register (Offset 073h in the *V320USC User's Manual*) is set while in this mode. This will allow the V320USC to complete its initialization by the Local Processor. This application note assumes that the V320USC sources RSTOUT# to the Local Processor (RC32355/RC32351). If the RST_OUT bit is set, then the RSTOUT# signal is de-asserted. And therefore, the Local Processor (RC32355/RC32351) is not in Reset. (See Note 1 in "Notes" on page 15.)

The Chip Selects of the V320USC are an extension of the Address Bus (A[25..0]) where CS[5..0]# is equivalent to A[31..26]. This correlation must be taken into consideration during the Local Processor Initialization, without an EEPROM. The V320USC decodes the full Address Bus (A[31..0]) and determines if it matches the address 0x1D00XXXXh. This is the default address of the V320USC's Internal Registers *(*see the *V320USC User's Manual*, Section 5.2.3.1 "Special Considerations for Systems Without Serial EEPROMs"). The five most significant bits are the Chip Select signals (CS[5..0]#) and thus must be either sourced from the RC32355/RC32351 or be terminated. Table 4 contains the mapping of the Chip Select signals to the address of the V320USC for initialization of its Internal Registers. The CSIR# signal is the only Chip Select signal to be asserted during initialization while the other unused Chip Selects are terminated to Ground or Vcc.

EEPROM Port Connection	CFG_RETRY	RST_OUT	Description
SDA pulled high	1 until V3230USC is initialized	1	Typically used for initialization via local processor (IDT RC32355/ RC32351) (See Note 1 in "Notes" on page 15)
SDA tied low	0	0 until V320USC is initialized	Typically used for initialization via PCI Interface
SDA and SCL connected to valid EEPROM device and SDA pulled high	Value from EEPROM	Value from EEPROM	Initialization from EEPROM

Table 3 V3 V320USC EEPROM Initialization Modes

Signal Name	Termination	Comments
CS5#	CSN5	New Signal: CSIR#. Access to V320USC's Internal Registers.
CS4#	Pull down to Ground	Resistor Termination
CS3#	Pull down to Ground	Resistor Termination

Table 4 V320USC to RC32355/RC32351 Chip Select Mapping (Page 1 of 2)

Notes

Signal Name	Termination	Comments
CS2#	CSN4	New Signal:CSA2#. Access to V320USC's Local to PCI Aperture 2.
CS1#	CSN3	New Signal:CSA1#. Access to V320USC's Local to PCI Aperture 1.
CS0#	Pull up to Vcc	Resistor Termination

Table 4 V320USC to RC32355/RC32351 Chip Select Mapping (Page 2 of 2)

PCI Initialization of the V320USC

The PCI Interface Mode of initializing the V320USC is selected when the SDA pin (pin number 197 in the *V320USC Datasheet*) is sensed as being low and not connected to a Serial EEPROM.

When this mode is selected, the CFG_RETRY bit in the PCI_BUS_CFG Register (Offset 05Ch in the *V320USC User's Manual*) will be cleared. When cleared, the PCI Interface may conduct transactions to the V320USC without a retry condition.

The RST_OUT bit in the System Register (Offset 073h in the *V320USC User's Manual*) is cleared until the V320USC is finished being initialized by the PCI Interface, thus issuing a reset on the RSTOUT# signal to the RC32355/RC32351. This will allow the V320USC to complete its initialization while the Local Processor is in a condition of Reset (this approach assumes that the V320USC sources RSTOUT# to the RC32355/RC32351). Once the initialization is completed, the bit is set so that the RSTOUT# signal may be de-asserted and the RC32355/RC32351 may begin it's own initialization. (See Note 1 in "Notes" on page 15.)

EEPROM Initialization of the V320USC

This mode is selected when the SDA pin (pin number 197 in the *V320USC Datasheet*) is sensed as being pulled high and connected to a Serial EEPROM. The V320USC will begin reading the Serial EEPROM in order to initialize all of its internal registers.

There are two bits in the V320USC that are initialized during a Reset state, which are the RST_OUT and CFG_RETRY bits.

The RST_OUT bit in the System Register (Offset 073h in the *V320USC User's Manual*) is cleared when the V320USC comes out of a Reset state. This will put the RC32355/RC32351 into a Reset state and will not conduct transactions on the External Interface. During the initialization by the EEPROM, the RST_OUT bit is set, but will not immediately de-assert the RSTOUT# signal to the RC32355/RC32351 until the initialization has completed. When the initialization has completed, the V320USC will de-assert the RSTOUT# signal to the RC32355/RC32351 and thereby allow the RC32355/RC32351 to conduct transactions on the External Interface.

The CFG_RETRY bit in the PCI_BUS_CFG Register (Offset 05Ch in the *V320USC User's Manual*) is set when the V320USC comes out of a Reset state. While set, this bit will force PCI transactions to be retried. This effectively disables any PCI transactions until the initialization has completed. This bit is cleared during the EEPROM initialization but does not take effect until initialization has completed. Once initialization has completed, the PCI Interface is allowed to conduct transactions without retries. (See Section 3.2.4.3, "Determining that Initialization via EEPROM is Complete," in the *V320USC User's Manual*.)

IDT RC32355/RC32351 Control Signal Connections

The configuration signal connections between the IDT RC32355/RC32351 and the V3 V320USC are documented in this Section. Most of the signals are one to one connections between the two devices, and the SDRAM control signals, except for BS# and RD/WR#, which are discussed in Section "V320USC Control Signal Connections".

The format of the signals, documented below, is "Signal Name" of the RC32355/RC32351- "Signal Description"- Direction of signal with respect to the RC32355/RC32351, "Input or Output or Input/Output".

Notes

RSTN-Reset Input-Input

The RSTN signal is asserted, to the RC32355/RC32351, during the Reset cycle. During reset, the RC32355/RC32351 will sense the strapping resistors to determine what mode to boot-up in. Once RSTN is de-asserted, the RC32355/RC32351 will proceed booting from an external device, ROM/FLASH/other.

The signal that correlates to the RC32355/RC32351's RSTN signal is RSTOUT# from the V320USC. The V320USC is reset by the signal RSTIN#. While RSTIN# is asserted, the V320USC will clear the RST_OUT bit in the System Register of the V320USC (Offset 073h in the *V320USC User's Manual*). The RST_OUT bit will be set/cleared depending on the initialization mode. Clearing this bit results in the RSTOUT# signal being asserted to the RC32355/RC32351. The V320USC begins it's initialization after RSTIN# is de-asserted. (See the *V320USC User's Manual.)* (See Note 1 in "Notes" on page 15.)

CLKP-Clock-Input

The RC32355/RC32351's system clock is used to derive the pipeline, External Interface, and SDRAM clocks.

The V320USC correlates the signal LCLK to this signal. LCLK is the clock that the External Interface is synchronized to, including the SDRAM and the other peripherals on the External Interface.

CLKP is also used to generate the Serial EEPROM's serial data clock. (See the *V320USC User's Manual,* Section 3.2.4.2 "Timing Considerations when Initializing via the Serial EEPROM.")

BRN-Bus Request-Input

The RC32355/RC32351 senses the Bus Request signal (BRN) to determine whether the V320USC wants ownership of the interface. If the V320USC wants ownership, it will assert the Bus Request signal and then the RC32355/RC32351 will respond with the Bus Grant signal (BGN). The V320USC will hold the Bus Request signal as long as it needs to complete the current transaction. Once it is done with the transaction, it will de-assert the Bus Request signal and the RC32355/RC32351 will respond with de-asserting the Bus Grant signal.

The V320USC equates this signal to BREQ#. The V320USC uses this signal to request the External Interface from the RC32355/RC32351.

There are provisions to guarantee that the RC32355/RC32351 does not starve for access to the External Interface. These provisions are outlined in the "BREQ_IN#- Bus Request Input- Input" section.

BGN-Bus Grant-Output

The RC32355/RC32351 will assert the Bus Grant signal in response to the V320USC requesting ownership. The RC32355/RC32351 will de-assert the Bus Grant signal when the V320USC de-asserts the Bus Request signal.

The V320USC correlates BACK# to this signal. It senses this signal to determine when it has Master rights so as to conduct it's own transactions onto the External Interface. (See the BREQ_IN#- Bus Request Input- Input" section.)

AP[25:0]-Address Bus-Input/Output

The Address Bus of the RC32355/RC32351 is 26 bits and 4 of the higher order bits are comprised of GPIO pins. The GPIO pin designated by AP[25] is GPIOP[30], AP[24] is GPIOP[29], AP[23] is GPIOP[28], and AP[22] is GPIOP[27]. The Address and Data Buses are de-multiplexed, meaning that they do not share the same signal pins.

When the RC32355/RC32351 is Mastering the External Interface, it will assert a valid address onto the Address Bus as long as the Chip Select (one of CSN[5..0] signals) of the particular device is selected.

When the RC32355/RC32351 is not the Master of the External Interface, it will tri-state all of the peripheral signals except the Bus Grant signal. (See Table 1.) The V320USC may assert a valid address onto the Address Bus as long as it maintains asserting the Bus Request (BRN) signal to the RC32355/RC32351 and senses the assertion of the Bus Grant (BGN) signal from the RC32355/RC32351.

Notes

The V320USC correlates A[25..0] to this bus. It will sense this bus when the RC32355/RC32351 is conducting transactions on the External Interface and source it when the V320USC is granted the External Interface.

DP[31:0]-Data Bus-Input/Output

The Data Bus of the RC32355/RC32351 is 32-bits but it can be configured to be 8-, 16-, or 32-bits wide.

While the RC32355/RC32351 is the Master of the External Interface, the Data Bus will contain valid data as long as the particular Chip Select for the external device is asserted, a valid address is on the Address Bus, and no "Wait" cycle is being asserted. The "Wait" cycle is asserted by another device on the External Interface to insert Wait States into the current transaction. The data valid time is determined by the particular cycle, Read or Write. In a Read cycle, data must be valid when clock transition occurs just before the de-assertion of the Output Enable signal (OEN).

While the V320USC is the Master of the External Interface, the RC32355/RC32351 will tri-state all the signals on the External Interface with the exception of the Bus Grant signal. (See Table 1.) The Bus Request signal (BRN) will be asserted by the V320USC and sensed by the RC32355/RC32351, while the Bus Grant signal (BGN) will be asserted by the RC32355/RC32351 and sensed by the V320USC. The V320USC will terminate the transaction by de-asserting the Bus Request signal and then, in response, the RC32355/RC32351 will de-assert the Bus Grant signal.

The V320USC correlates D[31..0] to this bus. It will sense this bus when the RC32355/RC32351 is conducting transactions on the External Interface and source it when the V320USC is granted the External Interface.

OEN-Output Enable- Output

The Output Enable signal from the RC32355/RC32351 may be used as an "Intel" style Read control signal. It is asserted by the RC32355/RC32351 when it is the Master during a Read transaction on the External Interface. It is asserted in conjunction with the Chip Select signal to enable the Target device on the External Interface to output its data.

The V320USC does not sense this signal.

CSN[5:0]-Chip Select-Output

The Chip Select signals are comprised of some GPIO signals as well as dedicated ones from the RC32355/RC32351. The dedicated Chip Select signals are CSN[3:0] and the others would be assigned to any available GPIO pin not being used for another purpose. The Chip Select signals from the RC32355/RC32351 are used to select a particular device on the External Interface. They are used with the Output Enable and Read/Write signals to access data on the Data Bus.

The V320USC correlates these signals to CS[5..0]#. It also correlates these signals to the Address, where CS[5..0]# are equivalent to A[31:26] (see the *V320USC User's Manual*, Section 5.2.3.1, "Special Considerations for Systems Without Serial EEPROMs"). The decoding of the Chip Select signals into Address is very important when the system is designed to be initialized from the RC32355/RC32351, without an EEPROM (see the section "V320USC Local Processor Initialization"). The V320USC senses these signals when the RC32355/RC32351 is conducting transactions to it.

For the purpose of this application note, 3 Chip Selects are required for the interface between the RC32355/RC32351 and the V320USC. Less may be used, for your specific design, but all three were designated for full implementation of the V320USC device capabilities. These signals and logic are documented in the Logic Block Diagram. One Chip Select was chosen to access the Local to PCI Aperture 1 (CSA1# in the Logic Block Diagram). The second Chip Select was chosen for the Local to PCI Aperture 2 (CSA2# in the Logic Block Diagram). The third, and last, Chip Select was chosen for the Local to Internal Registers (CSIR#). All three Chip Selects are sourced from the RC32355/RC32351 to the V320USC.

Notes

RWN-Read/Write-Output

The Read/Write signal (RWN) is a Read when it is High and a Write when it is Low. It is used to access Data on the External Interface's Data Bus in conjunction with the Output Enable, Chip Select, and Byte Write signals.

The V320USC correlates RD/WR# to this signal. This signal is sensed by the V320USC when the RC32355/RC32351 is the Master and conducting transactions on the External Interface. The V320USC sources this signal when it is the Master. This signal is also sourced to devices on the External Interface such as Flash. For connections to the SDRAM, this signal must be qualified. The logic for this signal is in the "SDRAM Control Signal Connections" section.

BWEN[3:0]- Byte Write Enables-Output

The RC32355/RC32351 asserts the Byte Write Enable signals when it is the Master of the External Interface, to control which Byte, out of a total possible 4 Bytes, to Write to the external Target device. It is used in conjunction with the Chip Select and Read/Write signals to control write accesses for the Data Bus on the External Interface.

The V320USC correlates WE[3..0]# to these signals. These signals are sensed by the V320USC when the RC32355/RC32351 is conducting transactions on the External Interface and sources these signals when it is granted the External Interface. These signals are also sourced to devices on the External Interface such as SDRAM and Flash.

WAITACKN-Wait/Acknowledge-Input

Wait is used by the RC32355/RC32351 in accordance with standard "Intel" style bus protocols. It is specifically used to hold off the data access by the external device on the External Interface for whatever number of clock cycles that the external device wants.

Acknowledge is used by the RC32355/RC32351 in accordance with standard "Motorola" style bus protocols. It is specifically used to notify the RC32355/RC32351 that the data access has completed. "Burst device read transactions do not support WAITACKN configured as a transfer acknowledge input. (See Chapter 6, "Burst Device Write Transaction," in the User Reference Manual.)

In a Burst transfer, WAITACKN can only be configured as a Wait signal. If it is being implemented during a Read Burst transfer, it constrains the Read Wait State timing to be greater than or equal to 3 clock cycles. If it is being implemented during a Write Burst transfer, it constrains the Write Wait State timing to be greater than or equal to 3 clock cycles. (See Chapter 6, "Burst Device Write Transaction,"in the User Reference Manual.)

The V320USC correlates this signal to WAIT#. The V320USC uses this signal to insert Wait States into transactions on the External Interface from the RC32355/RC32351. (See Note 2 in "Notes" on page 15.)

BOEN-Buffer Output Enable-Output

The RC32355/RC32351 supports an external buffer on the External Interface. The Buffer Output Enable signal should be asserted whenever an external access is conducted. It is asserted along with the Chip Select, Output Enable (for read accesses), Read/Write (for read or write accesses), Byte Write (for write accesses), and the Buffer Direction Control signal.

The V320USC does not use this signal, unless an external Buffer is utilized.

BDIRN-Buffer Direction-Output

The RC32355/RC32351 asserts the Buffer Direction signal High when it is in the direction of a write access on the External Interface, and Low when it is in a read access. "The BDIRN output is always in the opposite state of the RWN pin" (See Chapter 6 in the User Reference Manual).

The V320USC does not use this signal, unless an external Buffer is utilized.

Notes

DMAREQN-DMA Request-Input

The DMAREQN signal is an alternative function on the General Purpose I/O pins and it is specifically GPIOP[18]. The RC32355/RC32351 senses the DMA Request signal to determine when a Master on the External Interface wants to conduct a DMA transaction. The RC32355/RC32351 will respond by asserting the Chip Select signal, for that particular device, and conduct the DMA transaction to/from the required device. The external device will then de-assert the DMA Request signal, until it needs to request it again.

In the case of a Burst DMA transaction, the initial DMA Request will notify the RC32355/RC32351 (via the Transfer Size field in the first word of four words of the DMA Descriptors, in RC32351 User Reference Manual) that a burst will be conducted. The Chip Select signal, for that particular device, will be asserted by the RC32355/RC32351 shortly after the DMA Request signal is sensed. Once the Master on the External Interface senses the Chip Select it will then respond by de-asserting the DMA Request signal. The RC32355/RC32351 will continue generating Chip-Selects for the burst transactions, without the use of the DMA Request signal, until the number of accesses has completed. (via the number of Bytes in the Count field in the first word of four words of the DMA Descriptors, in the User Manual).

The V320USC does not use this signal, because a DMA operation does not need to be requested by the V320USC.

DMADONEN-DMA Done-Input

The DMADONEN signal is an alternative function on the General Purpose I/O pins and it is specifically GPIOP[19]. The signal is used to notify the RC32355/RC32351 that the DMA transaction is done. It is asserted during a Read access, by the external device on the External Interface, when data on the Data Bus is actually valid. During a Write access, the DMA Done signal is asserted one clock before the Byte Write signal is de-asserted and the DMA Done signal is de-asserted on the same clock as when the Byte Write signals are de-asserted.

The V320USC does not use this signal, because a DMA operation does not need to be requested by the V320USC.

DMAFIN-DMA Finish-Output

The DMAFIN signal is an alternative function on the General Purpose I/O pins and it is specifically GPIOP[31]. The signal is used to signify that the DMA transaction is finished and that the current access is the last one. For a Read or Write access, it will be asserted by the RC32355/RC32351 onto the External Interface to a particular device before the Chip Select signal is asserted. It will de-asserted after the de-assertion of the Chip-Select signal, as long as, that is the access by which the Count field is zero. This signifies that the DMA transaction is done and that the particular access is the last one.

The V320USC does not use this signal, because a DMA operation does not need to be requested by the V320USC.

SDRAM Control Signal Connections

The control signals for the SDRAM are critical to the performance of the subsystem. The System Clock is the same frequency as the SDRAM Clocking structure. The SDRAM is expected to operate at the full bandwidth of the System Clock and, therefore, careful attention must be administered to the handling of these critical signals. This section will outline which signals they are and recommend a method of interconnect.

SDRAM Write Enable

The RC32355/RC32351 implements a separate Write Enable signal for the SDRAM, SDWEN. The RC32355/RC32351's Read/Write signal, RWN, is used for all other peripherals on the External Interface, including the V320USC. The RWN signal, from the RC32355/RC32351, is a direct-connect to the V320USC's Read/Write signal, RD/WR#. The V320USC does not have a separate read/write control signal for SDRAM. The V320USC must drive the SDRAM Write Enable by qualifying it with the Bus Grant signal, BGN from the RC32355/RC32351 (See the section "BGN-Bus Grant-Output" on page 8). The timing asso-

Notes

ciated with the SDWEN signal, from the RC32355/RC32351, is of critical nature and must be treated as such. The “SDRAM Control Logic Diagram” depicts the approach, by which, the signal should be connected.

SDRAM Column Address Strobe

The RC32355/RC32351 sources a Column Address Strobe, CASN, as well as the V320USC, CAS#. Since the timing to the SDRAM is critical, these signals must also be qualified. The “SDRAM Control Logic Diagram” depicts the approach, by which, the signal should be connected.

SDRAM Row Address Strobe

The RC32355/RC32351 sources a Row Address Strobe, RASN, as well as the V320USC, RAS#. Since the timing to the SDRAM is critical, these signals must also be qualified. The “SDRAM Control Logic Diagram” depicts the approach, by which, the signal should be connected.

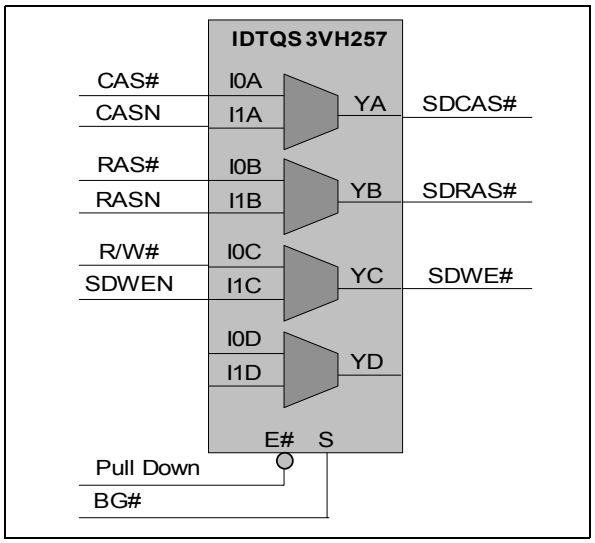


Figure 1 SDRAM Control Logic Diagram

V3 V320USC Control Signal Connections

There are certain signals that do not have a direct correlation to the IDT RC32355/RC32351. These signals need to be modified by external logic devices to interface to the RC32355/RC32351 and other devices on the External Interface.

BS#-Bus Cycle Start-Input

This signal is used by the V320USC to determine when the RC32355/RC32351 has begun a new transaction on the External Interface.

The RC32355/RC32351 does not support this signal directly. This signal is derived from the Chip Selects (CSN[5:3]) and the Clock (CLKP) signals from the RC32355/RC32351. The logic and timing for this signal is shown in the “Bus Cycle Start Logic Diagram” and the “Bus Cycle Start Timing Diagram”. The BS# signal is generated whenever a transaction has begun from the RC32355/RC32351 to the V320USC and, specifically, when the Chip Select signal is asserted. **The V320USC is not capable of Bursts to non-SDRAM regions while in SuperH Mode** (See the *V320USC User’s Manual*, Section 5.4.2, “Local Read from PCI”). **Therefore, the RC32355/RC32351 cannot conduct burst transactions to and from the V320USC device.** This is a minimal limitation, because the RC32355/RC32351 would rarely be required to burst to the V320USC. The predominant number of transactions, between the RC32355/RC32351 and the V320USC, are single cycle. Each device is capable of conducting transactions directly to all the devices that are on the External Interface. Both, the RC32355/RC32351 and the V320USC independently, incorporate powerful DMA Controllers to move large blocks of data, in a single cycle burst mode fashion. This direct access capability increases performance and also alleviates the need for bursting between the RC32355/RC32351 and the V320USC.

Notes

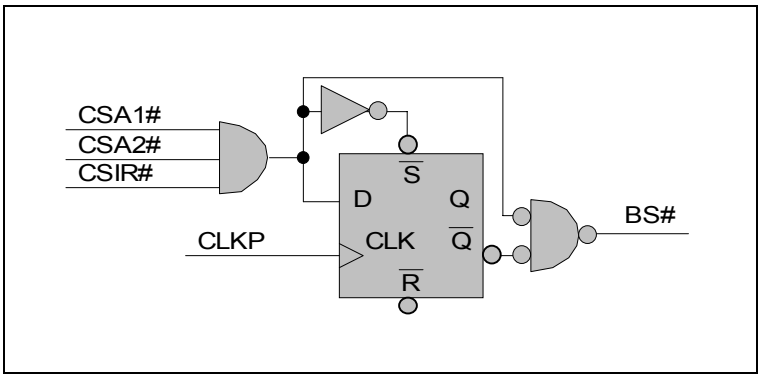


Figure 2 Bus Cycle Start Logic Diagram

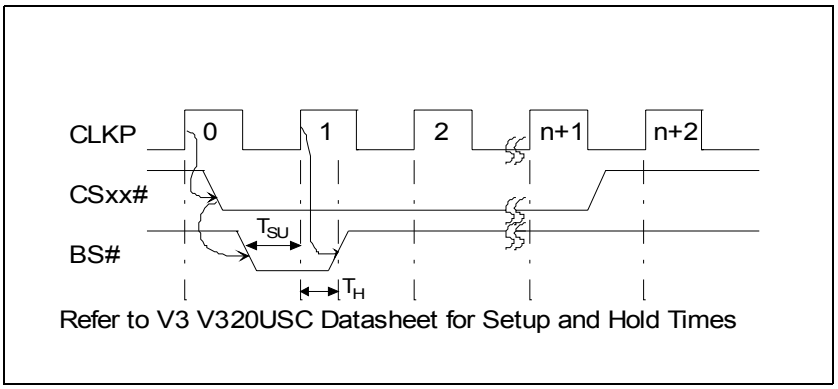


Figure 3 Bus Cycle Start Timing Diagram

Note: Refer to the V3 V320USC Data Sheet for setup and hold times.

BREQ_IN#-Bus Request Input-Input

The RC32355/RC32351 is the only device on the External Interface that can grant access to the V320USC. It is responsible for arbitrating the External Interface for all devices. It is also the highest priority device on the External Interface. It is necessary for the RC32355/RC32351 to have a process of terminating a Bus Grant condition on the External Interface away from the V320USC. The V320USC has two methods of accomplishing this.

The first approach is for the highest priority device, the RC32355/RC32351, to source a signal to the V320USC's BREQ_IN# pin. This signal will notify the State Machine of the V320USC to relinquish the External Interface to the RC32355/RC32351.

The second approach involves programming the Bus Mastering Latency Timer inside the V320USC. This timer is programmed for the amount of time the V320USC may occupy the External Interface. This allows the RC32355/RC32351 to avoid starvation of the External Interface. The Bus Mastering Latency Timer is enabled through the MB_LT bits of the LB_BUS_CFG register (Offset 07Ch). (See the *V320USC User's Manual*, Chapter 10, "I/O Controller" and Chapter 13, "Register Descriptions.") Whenever the V320USC is occupying the External Interface, the Bus Mastering Latency Timer begins counting down from its initial value. When the count reaches zero, the burst in progress will be finished and the V320USC will release control of the External Interface.

In both approaches, the V320USC will relinquish the External Interface by de-asserting the BREQ# signal (BRN is tied to this signal from the RC32355/RC32351). The RC32355/RC32351 will sense that signal on its BRN pin and will respond with de-asserting the BGN signal (BGN is tied to the V320USC's BACK# signal). The V320USC will sense the BACK# pin to close out the arbitration.

Notes

In the first approach, the CPU will request back the External Interface if it requires access by de-asserting the Bus Grant. The V320USC's state machine can only relinquish the External Interface if the CPU asserts Bus Interrupt Request *(refer to stepping information on V320USC)*. A small amount of Logic is required to generate the Bus Interrupt Request signal to the V320USC from the Bus Grant being de-asserted. The V320USC will end whatever transaction it was conducting, prior to the Bus Interrupt Request, and then relinquish the External Interface back to the CPU. The V320USC will relinquish the External Interface by de-asserting the Bus Request and the Logic will de-assert the Bus Interrupt Request a clock cycle after the V320USC de-asserts the Bus Request.

For the second approach, no signal would be added to the design, only programming of the internal registers of the V320USC.

The first approach is incorporated into this Application Note, where a BREQ_IN# signal is generated from external logic. It provides an optimal arbitration method between the two devices in instances of bus starvation and SDRAM refresh. (See the Bus Request Logic Diagram, Bus Request Timing Diagram, Section 3.1.1 "Arbitration," *V320USC User's Manual*, Section 5.2.1.1 "Bus Preemption," and the RC32355 User Manual or the RC32351 User Manual, Chapter 8, "Bus Arbitration".) (See Note 3 in "Notes" on page 15).

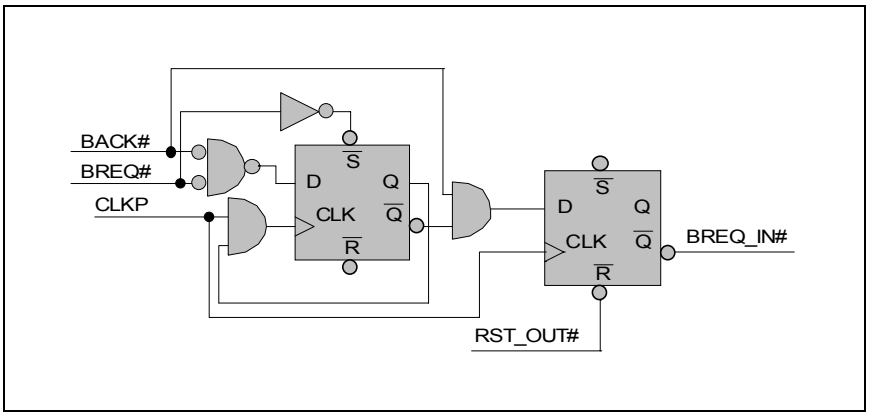


Figure 4 Bus Request Logic Diagram

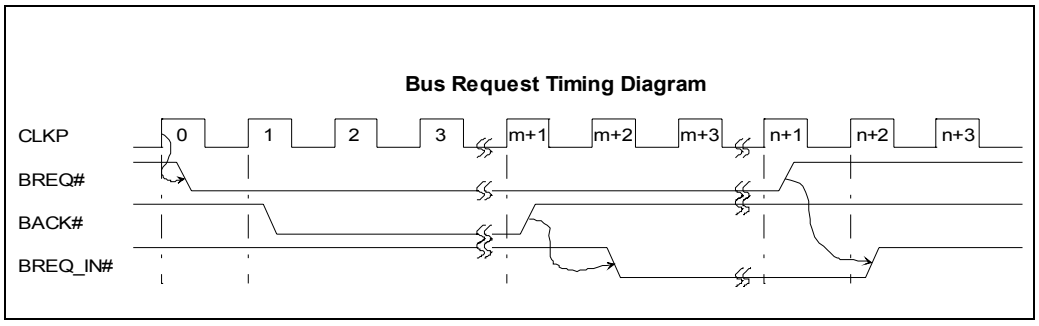


Figure 5 Bus Request Timing Diagram

RBE[3..0]#-Byte Read Enables-Input

The V320USC has provisions for the CPU, on the External Interface, to conduct Read transactions with the added benefit of Byte Enables. This allows the CPU to Read only the Bytes that are applicable.

This feature is not supported on the RC32355/RC32351. The next Section will provide information on how to disable this feature in the V320USC.

Notes

RBEN#-Read Byte Enable-Input

The V320USC's RBEN# is the signal that either enables or disables the Byte Read Enable feature. The signal may be terminated to the Vcc of the V320USC in order to disable the Byte Read Enables or to Ground to enable them.

The RC32355/RC32351 has no provisions for Byte Read Enables. Therefore, the Read Byte Enable signal should be terminated to the Vcc of the V320USC.

Assumptions

The specific responsibility of incorporating board level components such as resistors, capacitors, and inductors were intentionally left out of this Application Note and left for the reader to determine value and location. Although the IDT RC32355/RC32351 and V3 V320USC are capable of interfacing to all the devices on the block diagram, the reader may choose to only populate some, all, or other components onto the External Interface.

Although every effort was made for the accuracy and validity of the information in this document, this application note should be used as a guide and not as a specific reference only.

References

The following list contains all the documentation used to complete this application note. Every effort was made to incorporate the most up to date and accurate documents. The particular revisions are listed for your reference.

IDT RC32355 or RC32351 Data Sheet

IDT RC32355 or RC32351 User Reference Manual

V3 V320USC Datasheet, Rev 1.02 DS-UC01-0102

V3 V320USC User's Manual, Rev. 1.10 UM-UC01-0110

V3 V320USC Tsunami II Evaluation Board Rev 1.00 UM, Filename on Web: "UM-TN01-0100.V320USC" (This document includes the schematics for the SH processor to the V3 V320USC).

V3 V320USC Universal System Controller Revision B0 to Revision B1 Stepping Change Notification.

V3 V320USC B1 Step Errata Technical Note

Notes

1. At the time of writing this Application Note, the B1 stepping of the V320USC contained an errata in relation to the RST_OUT# signal. The stepping (B1-1) mentions that although the V320USC may be configured for an EEPROM initialization, it will not set the RST_OUT bit in the System Register. This will cause the RST_OUT# to be de-asserted and thus the RC32355/RC32351 would not see a reset. The workaround is noted in the stepping.

2. At the time of writing this Application Note, the B1 stepping of the V320USC contained an errata in relation to the WAIT# signal. The original operation, B0 step, of this signal involved assertion and de-assertion in the following manner, Z-L-H-L-Z. The new, B1 step, allows for operation that would closely match the RC32355/RC32351 and that is, Z-L-H-Z.

3. At the time of writing this Application Note, the B1 stepping supports the function whereby the RC32355/RC32351 may request the termination of the V320USC's Bus Grant. The B1 stepping information refers to a signal, called out as "PREEMPT#", that directly correlates to the BREQ_IN# signal in the *V320USC User's Manual* and the data sheet. (See the *V320USC User's Manual*, Section 5.2.1.1, "Bus Preemption" and the V320USC data sheet's Table 5: Signal Description-Local Bus Interface, SH3/4 Mode)

   The B0 stepping of the V320USC does not support the BREQ_IN# signal. (See the *V320USC User's Manual*, Section 5.2.1.1, "Bus Preemption," and the V320USC data sheet, "Table 5: Signal Description-Local Bus Interface, SH3/4").

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.