1893 ETHERNET PHYCEIVER USER DESIGN GUIDE

Introduction

This guide explains best design practices for designing the ICS1893 10/100 Ethernet Phys into applications. These practices apply to all ICS1893 3.3V 10/100 Ethernet Phys which include the part numbers listed below. IDT supplies both Commercial temp and Industrial temp Phys and all Phys are available in lead free packages.

Single Phy (non MDIX)	Application	Package
ICS1893AF, AFI, AFLF, AFILF	MII, Node	48-pin SSOP
ICS1893Y-10, YI-10, Y-10LF, YI-10LF	MII, 5bit stream, 7wire, HW	64-pin 10x10 TQFP

Single Phy (with MDIX)	Application	Package
ICS1893BF, BFI, BFLF, BFILF	MII, Node	48-pin SSOP
ICS1893BK, BKI, BKLF, BKILF	MII, Node	56-pin 8x8 MLF2
ICS1893BY-10, BYI-10, BY-10LF, BYI-10LF	MII, 5bit stream, 7wire, HW	64-pin 10x10 TQFP

Single Phy (with MDIX Latest Silicon)	Application	Package
ICS1893CF, CFI, CFLF, CFILF	MII, Node	48-pin SSOP
ICS1893CK, CKI, CKLF, CKILF	MII, Node	56-pin 8x8 MLF2
ICS1893CY-10, CYI-10, CY-10LF, CYI-10LF	MII, 5bit stream, 7wire, HW	64-pin 10x10 TQFP
ICS1893CK-40	MII, Node	40-pin MLF

** **I** = I-temp; **LF** = lead free package

Phy Selection

Selecting the correct ICS1893 10/100 Ethernet Phy for your application is a fairly simple task. The above product table looks complicated but there are two broad categories of ICS1893 Ethernet Phys, those with Auto-MDIX and those without. The Auto-MDIX feature removes the need to determine if an application uses a "straight" or "crossed" cat5 cable and is targeted towards consumer applications. The next choice depends on whether the application requires special hardware configuration, is used in a Repeater application or needs to be interfaced with a legacy MAC interface. For these applications the higher cost 64-pin TQFP package is optimal. The 1893C family is recommended for all new designs.

All IDT 10/100 Phys support the standard IEEE 4bit parallel MII interface. All support the NODE mode operation and Auto-Negotiation. The vast majority (95%) of IDT PHY applications are satisfied with 1893CF. If small physical package size is important we recommend using ICS1893CK-40 (available in 6x6 MLF package). For applications requiring hardware speed / duplex configuration or the 5bit stream MAC interface/ 7wire 10base MAC interface we recommend using 1893CY-10. IDT Phys do not support 2 bit RMII or 3 bit Intel proprietary CNR interfaces. The last choice involves temperature range and lead free package. All IDT10/100 Phys are available in I-temp range and lead free packages. Standard commercial temperature range is 0°C to 70°C and the I-temp range is -40°C to 85°C.

Ordering information and package drawings are provided at the end of the IDT datasheet. All IDT Phy datasheets are available for download at www.idt.com. Search for part number without ICS. For example, "1893CF".

MAC interface

ICS1893 Phys support three types of MAC interface. The most common is the 4bit IEEE MII standard interface. The second MAC interface is the 5 bit 100baseTX stream mode. The third is the serial 10base or 7 wire 10baseT. The 5 bit 100baseTX stream MAC is seldom seen today where the MAC provides 5 bits symbols which include all encoding. The Phy simply serializes the 5 bits data and transmits or receives the 5 bits with no change. The 10baseT 7 wire serial 10baseT interface is seen in some controller products. Both the 5 bit stream and 10baseT 7 wire MAC interfaces are supported by the 64-pin TQFP package (1893Y-10, 1893BY-10 and 1893CY-10). The 1893Y-10, 1893BY-10 and 1893CY-10 provide the MII/SI hardware pin to select these MAC protocols. When present, the MII/SI pin must be tied high for the 5 bit Stream/ 7 Wire serial MAC interfaces or low for the MII interface.

TXCLK and RXCLK Pins

The Phy sources both TXCLK and RXCLK. These clocks are 25 MHz, 2.5 MHz or 10 MHz depending on the MAC interface type and Speed. These signals are sent by the Phy to the MAC to provide a clock reference for data setup and hold time between the MAC and Phy. These signals should have a 33 ohm series termination resistor to match the 50 ohm PCB trace impedance.

RXdata, TXdata, RXDV, TXEN, TXER, RXER, CRS and COL Pins

The Phy data signals connect to the corresponding signals on the MAC. These pins do not require a series terminating resistor. The RX Data Valid signal, RX Error signal and RX receive data bits are sourced by the Phy to the MAC. These signals are clocked by the Phy RXCLK. The TX Enable signal and TX Transmit Data bits are sourced by the MAC to the Phy. These signals are clocked by the Phy TXCLK. ICS1893 Phys have robust data setup and hold time margins with little board layout concern. The TXER and RXER Error signals are meaningful in 100baseTX mode only. In 100baseTX, 5 bit code symbols are transmitted for each 4 bit data nibble. This allows idles, start of frame, end of frame and halt symbols to be added to the 4 bits of data. Of the 32 possible code symbols 10 are invalid. ICS Phys will pulse the RXER pin high for each invalid code bit group received. The TXER pin allows the system to generate transmit error symbols for testing purposes. All ICS 1893 Phys support the RXER pin but only the 64-pin TQFP package parts support the TXER pin. Most applications tie the TXER pin to VSS. Do not let the TXER pin float. The TXER pin if present is connected to the MAC.

TXER pin or VSS. The Carrier Sense (CRS) pin is used in repeater applications to indicate packet transmission OR receive. Node applications do not typically use the CRS information. Connect the Phy CRS pin to the corresponding MAC CRS pin. The Collision (COL) signal is only asserted in Half Duplex mode and is high when a simultaneous transmit and receive condition is detected by the Phy. Connect the COL pin to the MAC COL pin.

Hardware Configuration Pins Available on the ICS1893Y-10, ICS1893BY-10 and ICS1893CY-10

The lower cost 48-pin SSOP and 56-pin MLF packages are pre-configured for Node, Software mode with Auto-Negotiation enabled. No further configuration is needed with the 48-pin and 56-pin Phys. The 64-pin TQFP packaged ICS1893 Phys bring out several additional pins to allow hardware pin configuration. Hardware configuration can be tricky and can result in conditions where no link is possible. Be careful when using hardware configuration mode.

Node/Repeater Selection Pin

Most single Phy applications are Node applications. However the 64-pin TQFP package parts can be configured to support Repeater applications by connecting the Nod/Rep pin high (this pin is tied to VSS for Node applications). Repeater mode changes the CRS and COL behavior for repeater applications. The Nod/Rep pin must be tied high or low.

HW/SW, 10/100, DUPSEL and ANSEL Pins

Connecting the HW/SW pin low selects hardware configuration setup. The HW/SW pin works in conjunction with the 100SEL, DUPSEL and ANSEL pins. When the HW/SW pin is held low these three pins are inputs. When the HW/SW pin is held high the Phy is set in Software mode and these three pins are outputs to indicate chip status. The HW/SW pin must be tied high or low. The following table indicates the mode for all conditions when in HW mode is enabled by connecting the HW/SW pin low:

HW/SW	10/100	DUPSEL	ANSEL	Mode
GND	GND	GND	GND	Fixed 10base, HD no Auto-Negotiation
GND	GND	VDD	GND	Fixed 10base, FD no Auto-Negotiation
GND	GND	VDD	VDD	Auto-negotiation but only 10base FD advertised
GND	VDD	GND	GND	Fixed 100base, HD no Auto-Negotiation
GND	VDD	GND	VDD	Auto-negotiation but only 100base HD advertised
GND	VDD	VDD	GND	Fixed 100base, FD no Auto-Negotiation
GND	VDD	VDD	VDD	Auto-negotiation but only 100base FD advertised

Note the restricted cases when ANSEL is enabled. Only one of the four possible speed/duplex combinations is advertised. This is a very restricted advertisement and can result in a NO link condition. The IEEE specification states that if a part auto-negotiates with a non-auto negotiation partner is must come up in Half Duplex. This can cause conflicts in some of the cases shown above. Be weary of these potholes when using Hardware configuration mode. A safe hardware mode would be to select the hardware auto-negotiation enabled mode advertising 10baseT/ HD. This configuration will result in a valid link with partner Phy's supporting auto-negotiation and those that do not. Both Phys will always connect in 10baseT/ HD. If you don't need the hardware configuration or the extra features, use the lower cost SSOP or MLF2 packaged products. The 10/100 pin is available on SSOP packages as an output and can be used to drive a speed indicator LED. 10/100 select pin High indicates 100baseTX mode and Low indicates 10baseT mode. If the part is in software mode (HW/SW pin=high) then the 10/100, Duplex Select and ANSEL are all outputs capable of driving LEDs. Two additional status pins are available on the 64-pin TQFP. The LSTA pin provides Link status. (High=Link Valid). The LOCK pin indicates that the receive PLL is locked on to the incoming signal.

Serial Management Interface, MDIO and MDC Pins

All ICS phys support the serial MDIO management interface. The MDIO pin is a bidirectional shared serial bus. Up to 31 Phys can share this bus. In reality usually only one Phy is connected to the bus. The MDIO pin connects directly to the MAC MDIO pin. The MDC is a free running clock supplied by the MAC which can be 50 kHz to 2.5 MHz. The selection of which Phy of the 31 is being addressed is by an assigned Phy address. See section on LED/Phy address for setting the Phy address. Not all applications will use the MDIO interface. Thus the term managed and unmanaged Phys. The MDIO interface allows the Phy to be configured and status to be read by the MAC. The MDIO protocol and public register bit assignments are all IEEE defined. All ICS Phy's follow the IEEE standard. The MAC always initiates the transaction which is either a register read or register write. The register space is 32 words of 16 bits each. Not all 32 registers are used and only the group described in the datasheet are public. Non-listed register may exist and writing a non-public register can result in detrimental effects. When a MDIO read/write transaction is initiated the MAC sends the PHY address (0-32), a read/write bit followed by 16 bits of data. If the transaction is a write, the initial command includes the data. For a read, the MAC tri-states the MDIO bus after the R/W bit and the Phy returns the 16 bit register contents. From an application standpoint just connect the MDC and MDIO pins directly to the MAC MDC and MDIO.

Important*: The MDIO pin is IEEE specified to have a 1.5K Ohm pullup resistor to VDD (included on the evaluation board). The MDIO is a shared bus which can be tri-stated between transactions. Not having the required 1.5K Pull-up can result in spurious writes to the Phy control registers due to the free running MDC clock. For applications not using the MDIO tie both MDIO and MDC to VDD.*

REG Pin (only on ICS1893Y-10, ICS1893BY-10 and ICS1893CY-10 products)

The 64-pin TQFP package has a REG pin (pin 20) that is designated "no connect" in the datasheet. This pin has a built-in 50k pull-up resistor so the pin will be held high for the no connect. The purpose of this pin is to allow access to internal proprietary registers in the ICS1893 Phy. ICS suggests adding artwork for a "No stuff" resistor to GND just in case you need to access the proprietary registers. The public registers described in the datasheet do not need the REG pin held low for access. Note, on the 48-pin SSOP, 56-pin MLF2 and 40-pin MLF package products, the REG pin is hardwired to GND inside the package.

LED /Phy Address Pins P4RD, P3TD, P2LI, P1CL & P0AC

All ICS1893 Phys have five hardwire pre-configured LED pins which serve the dual function of capturing the PHY address and driving LED status information. The LEDs indicate Phy Receive, Transmit, Link, Collision and Activity status. Most application only use the Valid Link and Activity LEDs. The Activity LED is simply the OR of Receive LED and Transmit LED. There are three ways to reset IDT Phy's. The external hardware pin reset (Resetn), a built-in reset on Power-on and a software reset. ICS Phys capture the Phy address with a Hardware Reset or Power-on reset. The software reset in control register 0 does not capture the Phy address. During Hardware or Power-on reset the five LED pins are briefly tri-stated and the voltage on the LED pins is captured to assign the PHY address. A high on the LED pin is captured as a 'one' for that Phy address bit. Most Phy application use 00001 for the Phy address (Phy address on evaluation board is defaulted to 00001). As mentioned above, simply powering up the Phy will capture the Phy address. A slow 3.3V power ramp (<1V/50mS) can result in a false Phy address. When an LED is connected in series to VDD or GND the LED voltage drop can be significant resulting in an indeterminate LED pin voltage during power up. Therefore you need to add a 10Kohm resistor across the LED to ensure the LED pin will be at the full VDD or GND rail during power-up sequence. This ensures correct address capture on power up. If the Phy captures the wrong address, the MDIO can not address the Phy. A current limiting resistor of 1Kohm is usually added in series with the LED. The LED pins are driven strongly in the opposite sense from the sense sampled during power-up to indicate a true condition. As an example, if the P0AC LED is reset to "0" then that pin will drive strongly to VDD to indicate Activity. Conversely is the POAC LED is reset to "1" then that pin will drive strongly to GND to indicate Activity. Although the LED pin drives strongly to indicate a true condition it does not drive strongly for the non-true condition. Some applications combine the Activity and Link LEDs to blink off for Activity. Make sure to use external resistors or a simple transistor circuit that handles the non-driven condition. Remember the LED pin only drives in the true direction and tri-states for the non true condition. Even if not all the LED pins are used in an application it is recommended to configure them with a simple resistor to a known voltage rail on power-up.

***Important**: All ICS Phys have a special meaning for Phy address 00000 as a tri-state MII address setting. Address 00000 will tri-state the RXD bits, TXCLK and RXCLK Output of ICS1893. Never use '00000' Phy address for normal Phy operation.*

Resetn Pin

The Resetn pin is an external hardware reset pin. It is active low and must be configured high for the PHY to work. When the Resetn pin is held low, the PHY is in low power state with MII and LED pins tri-stated. Some board designs just use a simple RC circuit of a 1K Ohm resistor to VDD and a 0.1uF cap to GND on the Resetn pin to provide a simple RC time delay reset on power ramp. Most designs connect the Resetn pin to the system hardware reset.

Clocking the ICS1893 with a Crystal, REF_IN & REF_OUT Pins

Most Phy applications use the built in 1893 crystal oscillator with a simple 25MHz parallel resonant crystal. Connect the 25 MHz parallel resonant crystal across REF_IN and REF_OUT pins along with load capacitors (according to crystal manufacturer datasheet specifications) on either side of the crystal to ground. The effects of board layout parasitics must be taken into account when selecting the load capacitors. To determine the correct load capacitor values, use a frequency counter and probe at the TXCLK output (not REF_OUT) so as not to load the crystal. Set the counter for a 10 second sample and measure the TXCLK which should be 25 MHz in 100baseTX mode. The crystal frequency must be within +/- 50ppm over the life of the Phy. The series crystal current limit resistor is already built into the REF_OUT pad. No external series resistor is required.

Clocking the ICS1893 with an Oscillator, REF_IN Pin

A second means of clocking ICS1893 is to use a 25MHz CMOS clock source on the REF_IN pin. Suggestions here are to use a 25 MHz oscillator or the 25 MHz Reference output of a PLL clock synthesizer IC (with a crystal input source). It is not recommended to use a PLL synthesized 25 MHz output. The long term period jitter on the clock output generated by the PLL could result in high Bit Errors. The transmitted MLT-3 Jitter has a maximum 1.4nS IEEE specification. Clock input swing is 3.3V with 1893 Phys. The REF_IN switch point is at 50% VDD. The ICS1893 is insensitive to duty cycle on the REF_IN clock. The board layout could have a low pass filter in series with the clock signal consisting of a 33 ohm series resistor and a 10pF cap to GND at Phy REF_IN pin. This prevents high frequency noise from triggering the single sided clock input. Be cautious using ASIC generated REF_IN clocks as they tend to be noisy. A good design practice is to include artwork for a crystal backup just in case the intended clock source turns out to be noisy.

Current Setting Resistors 10TCSR and 100TCSR Pins

ICS1893 Phys have two band gap regulators that allow fine adjustment of the 10baseT and 100baseTX transmitted amplitudes. The transmitted output amplitudes are related to the current flowing out of these pins. The 10TCSR current adjusts the 10baseT amplitude and the 100TCSR current adjusts the 100baseTX MLT-3 amplitude. More current equates to higher amplitude.

Typical Values for 10TCSR and 100TCSR resistors for ICS Phy's:

Resistor Hookup	ICS1893A,Y and B	ICS1893C
10TCSR Resistor to VSS	2.00 Kohm	2.43 Kohm
100TCSR Resistor to VSS	1.54 Kohm	1.82 Kohm
100TCSR Resistor to VDD	12.1 Kohm	18.2 Kohm

The 12.1K (18.2K in the case of 1893C) pull-up resistor on the 100TCSR is to further regulate the current pulled out of the 100TCSR pin with negative feedback for variations in VDD. No bypass capacitors are used with ICS1893 Phys on these pins. Capacitors can cause the band gap circuits to oscillate resulting in unusual operation.

General Guideline:

Increasing the value of 100TCSR resistor to VDD will increase the MLT-3 amplitude and vice versa.

Increasing the value of 100TCSR resistor to GND will decrease the MLT-3 amplitude and vice versa.

Increasing the value of 10TCSR resistor to VSS will decrease the 10BaseT amplitude and vice versa.

The precise resistor values for setting the signal amplitude should be determined after the board design is completed and the magnetics are selected. The 100baseTX MLT-3 amplitude is more closely specified at 2.0V +/- 0.1V (differential). The 10baseT amplitude has a much relaxed specification of 4.4V to 5.6V differential. These amplitudes are measured differentially at the RJ45 connector with a 100 Ohm load.

Magnetics

It is recommended to use ICS1893 Phys with 1:1 turns ratio magnetics. The use of chokes is optional and the ICS1893 Phys are not sensitive to choke placement (cable side Vs chip side). It is important that the magnetics have separate chip side center tap capacitors to ground for transmit and receive side. The reason for this is that the ICS Phys power the chip side magnetics to slightly different bias points for transmit and receive functions. Shorting the center taps together can effect biasing of the receive circuit and result in poor performance. The cat5 cable is a balanced transmission line with four 100 Ohm characteristic impedance twisted pairs. 10/100 Ethernet systems typically use only two of the four twisted pairs. The 100baseTX signal is a scrambled signal with signal energy from 50 kHz to 125 MHz. Proper termination is required to maintain transmission line impedance matching. The IEEE TP-PMD specifies the RF return loss or SWR for an Ethernet system. Using the external schematic shown in the datasheet for the twisted pair will ensure a matched transmission line and low return loss. Twisted pair traces on the board should be length matched. Short leads are best and avoiding vias in the signal path is desirable for better matching. The magnetics help isolate the Phy from ESD events and prevent cable EMI radiation. The magnetics provide the isolation between the chip GND and the chassis ground. Keep all chip side connections bypassed to chip GND. Keep all cable side bypass connections including the RJ45 housing and Bob Smith network bypassed to the chassis ground. The chassis ground is separate and isolated from the circuit board GND. The ground plane should be removed under the magnetics. The board GND ground planes and Chassis ground planes should be broken through the magnetics. Please refer to the datasheet for exact components and schematics used with ICS1893A, ICS1893B and ICS1893C devices.

Note:

The external schematic is different for non-MDIX compared to MDIX Phys. MDIX Phys do not have an assigned transmit pair and the chip can swap it's transmit and receive pairs as needed to achieve link. The magnetics used with MDIX Phys are symmetric with respect to the chokes. Pay close attention to the polarity of each twisted pair keeping it constant from the ICS1893 twisted pair pins through the magnetics to the RJ45. Pin 1 on the RJ45 is the positive polarity for pair 1 & 2. Likewise Pin 3 is the positive polarity for the pair pins 3 & 6. Pins 4, 5 and 7, 8 are unused in most 10/100 systems. However since the plant wiring Cat5 will connect all twisted pairs, a Bob Smith damping termination is used on RJ45 pins 4, 5 and 7, 8 to help terminate coupled noise. Some Ethernet systems apply power on these unused twisted pairs. Gigabit systems use all four twisted pairs actively whereas 10/100 systems use only two of the twisted pairs for data transfer.

AMDIX_EN Pin on ICS1893B and 1893C MDIX Phys

The AMDIX_EN pin on the MDIX Phys allows these parts to be forced into non-auto MDIX mode. The ICS1893B/C products have a built in 50 Kohm Pullup resistor to VDD on this pin. Normally this pin would be left floating for Auto-MDIX enabled operation. Pulling the AMDIX_EN pin low can be used for system test to disable the Auto-MDIX function. IDT suggests a "No Stuff" resistor to GND in the artwork.

Bypassing the ICS1893 VDD Pins and Other Board Suggestions

The VDD Power pins of ICS1893 Phys should each be bypassed at the package pin with 0.1µF caps. Keep the trace lengths as small as possible for the bypass caps. ICS1893 Phys are not sensitive to low frequencies power noise caused by switching power supplies. IDT uses simple 4 layer boards with good results. The 2nd layer is the ground/GND plane and the 3rd level the 3.3V power plane. Be sure to break the Ground plane and VDD plane through the magnetics.

Special note about ICS1893BK MLF2 package and ICS1893CK-40 MLF package

These packages have an exposed GND paddle on the bottom of the package. This paddle can be soldered to GND but more importantly make sure to not route any power or signals under the package as they could get shorted to GND.

Software Consideration

The Phys do not require a software driver. The MAC supplies the MDIO interface pins and the MAC driver is used to configure the PHY. In most cases the Phy will come up with the default reset condition and be ready to go. Reset (hardware, software and power-up) resets all control registers in the PHY to their default settings.

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