

## Renesas RA Family

**16-Bit A/D Converter Performance for RA2A1****Introduction**

This application note describes the performance and calibration functions of the 16-bit A/D converter integrated into the RA2A1.

**Target Device**

RA2A1 MCU Group

**Conditions**

Unless otherwise specified, typical data are based on  $VCC = AVCC0 = AVCC1 = VREFH0 = 3.3\text{ V}$ ,  $VSS = AVSS0 = AVSS1 = VREFL0 = 0\text{ V}$ ,  $T_a = 25\text{ }^\circ\text{C}$

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### 1. Overview

A 16-bit A/D converter with digital calibration function is built into the RA2A1 MCU Group. The input mode can be selected as differential input mode or single-ended input mode. Digital calibration allows high-precision A/D conversion by calculating the offset error correction value and gain error correction value under the conditions of use.

This application note explains the 16-bit A/D converter timing parameters, linear characteristics, dynamic characteristics, A/D conversion current consumption, and how to perform calibration.

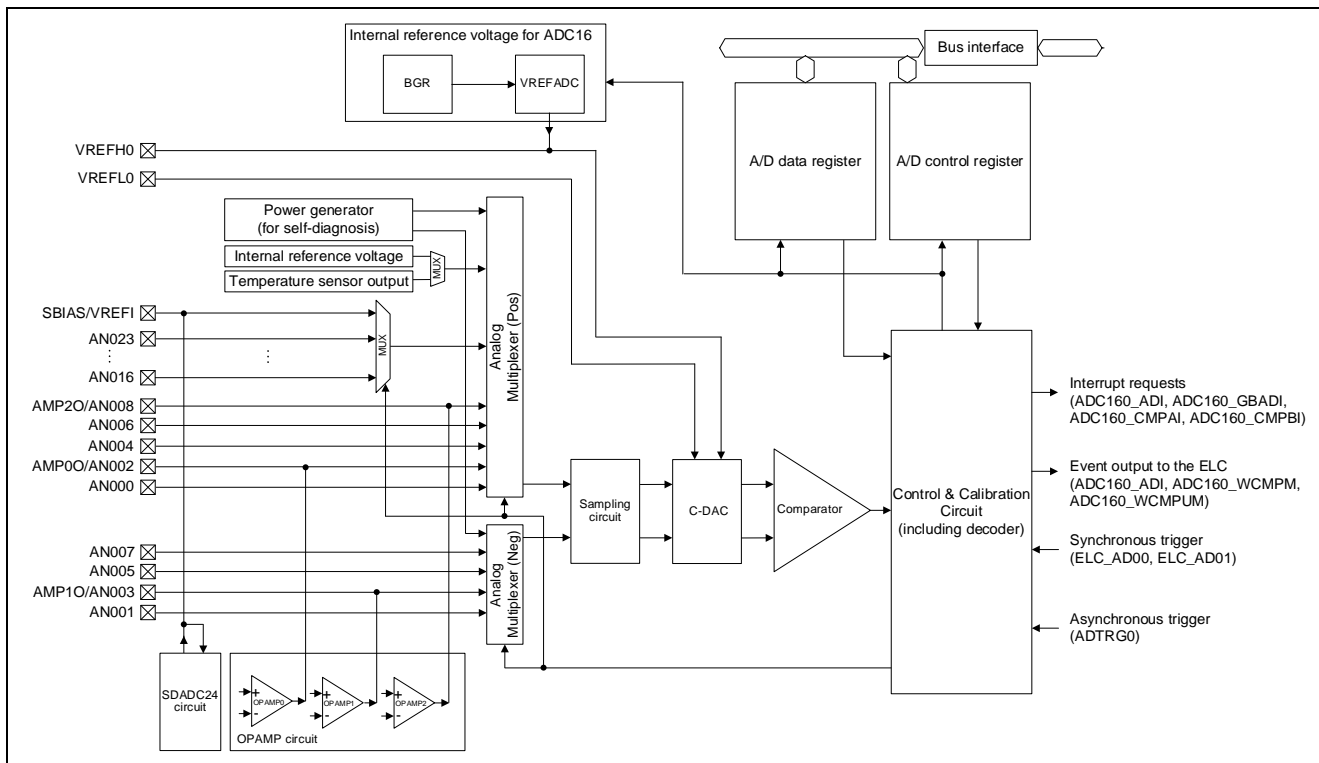


Figure 1. ADC16 Block Diagram

Table 1 ADC16 I/O Pins

Pin name	I/O	Function
AVCC0	Input	Analog block power supply pin
AVSS0	Input	Analog block power supply ground pin
VREFH0	Input*1	Reference power supply pin
	Output*2	VREFADC output voltage
VREFL0	Input	Reference power supply ground pin
AN000 to AN008, AN016 to AN023	Input	Analog input pins 00 to 08, 16 to 23
ADTRG0	Input	External trigger input pin for starting A/D conversion
SBIAS/VREFI	I/O	Power supply pin for sensor or external VREF input pin for the SDADC24

Notes:

1. When VREFH0 is used to supply the high potential reference voltage.
2. When VREFADC is used to supply the high potential reference voltage.

## 2. Utilizing Data Sheet Parametric Values

This section describes the electrical characteristics of the 16-bit A/D converter.

### 2.1 Analog Input Parameters

The 16-bit A/D converter has the following features:

- Analog input voltage is up to VREFH0 at  $VREFH0 \leq 5.5\text{ V}$ .
- Analog input common voltage range (Acm) in differential input mode is from VREFL0 to VREFH0.

Examples of input analog signal are shown in Figure 2.

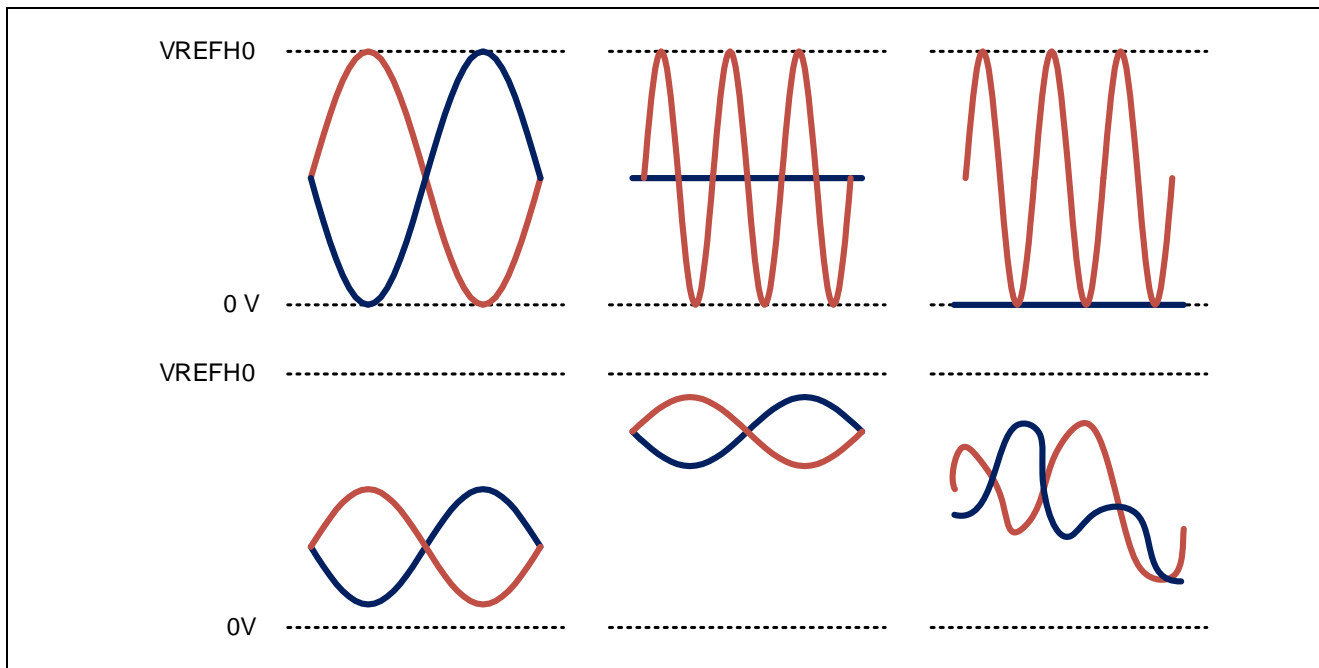


Figure 2. Examples of Input Analog Signal in Differential Input Mode

### 2.2 Timing Parameters

Table 2 shows the timing parameters of the 16-bit A/D converter.

Table 2. 16-bit A/D Conversion, Timing Parameters

Conditions:  $VCC = AVCC0 = AVCC1 = 1.7\text{ to }5.5\text{ V}$ ,  $VREFH0 = 1.7\text{ to }5.5\text{ V}$ ,  $VSS = AVSS0 = AVSS1 = VREFL0 = 0\text{ V}$ , Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Frequency	ADCLK <sup>*2</sup>	1	-	32	MHz	$3.0\text{ V} \leq AVCC0 \leq 5.5\text{ V}$ , $3.0\text{ V} \leq VREFH0$
		1	-	24		$2.7\text{ V} \leq AVCC0 \leq 5.5\text{ V}$ , $2.7\text{ V} \leq VREFH0$
		1	-	16		$2.4 \leq AVCC0 \leq 5.5\text{ V}$ , $1.5\text{ V} \leq VREFH0$
		1	-	8		$1.8\text{ V} \leq AVCC0 \leq 5.5\text{ V}$ , $1.5\text{ V} \leq VREFH0$
		1	-	4		$1.7\text{ V} \leq AVCC0 \leq 5.5\text{ V}$ , $1.5\text{ V} \leq VREFH0$
Conversion rate	Fs	-	-	$1/(t_{SPL}+18/ADCLK)$	S/s	-
Sampling time <sup>*1</sup>	t <sub>SPL</sub>	0.25	-	-	μs	High-precision channel, $2.7\text{ V} \leq AVCC0 \leq 5.5\text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
		3	-	-		High-precision channel, $1.7\text{ V} \leq \text{AVCC0} < 2.7\text{ V}$
		3	-	-		Normal-precision channel, $2.7\text{ V} \leq \text{AVCC0} \leq 5.5\text{ V}$
		10	-	-		Normal-precision channel, $1.7\text{ V} \leq \text{AVCC0} < 2.7\text{ V}$
Settling time	$t_{\text{START}}$	-	-	1	$\mu\text{s}$	$2.7\text{ V} \leq \text{AVCC0} \leq 5.5\text{ V}$
		-	-	3.2		$1.8\text{ V} \leq \text{AVCC0} < 2.7\text{ V}$
		-	-	8.9		$1.7\text{ V} \leq \text{AVCC0} < 1.8\text{ V}$

Notes: 1. Permissible signal source impedance Max = 0.5 k $\Omega$ .

2. The ADCLK clock is identical to the PCLKD clock. It must not exceed 32 MHz for the proper operation of ADC16. Since ICLK (CPU Clock) and PCLKD share the same clock source, getting the maximum ADC16 conversion rate requires that the CPU also runs at 32 MHz. Additionally, in this scenario, the UCLK (the USB clock) does not meet the required 48 MHz and so this interface cannot be used. If the users require running the CPU at its maximum clock rate or utilizing the USB interface, then the PCLKD must be set to 24 MHz, affecting the ADC16 conversion time accordingly.

The conversion rate ( $F_s$ ) consists of input sampling time ( $t_{\text{SPL}}$ ) and time for conversion by successive approximation ( $t_{\text{SAM}}$ ). The A/D conversion processing time (output rate of the conversion result) is the sum of the conversion rate and the gain correction time. However, because gain correction occurs concurrently with sampling, the gain correction time affects the A/D conversion processing time only in the first cycle of single scan, continuous scan, and group scan. Gain correction time ( $t_{\text{GAIN}}$ ) does not affect the second and later cycles. The  $t_{\text{SPL}}$  is used to charge sample-and-hold circuits in the A/D converter. Minimum  $t_{\text{SPL}}$  is defined only at signal source impedance 0.5 k $\Omega$  in Table 2.

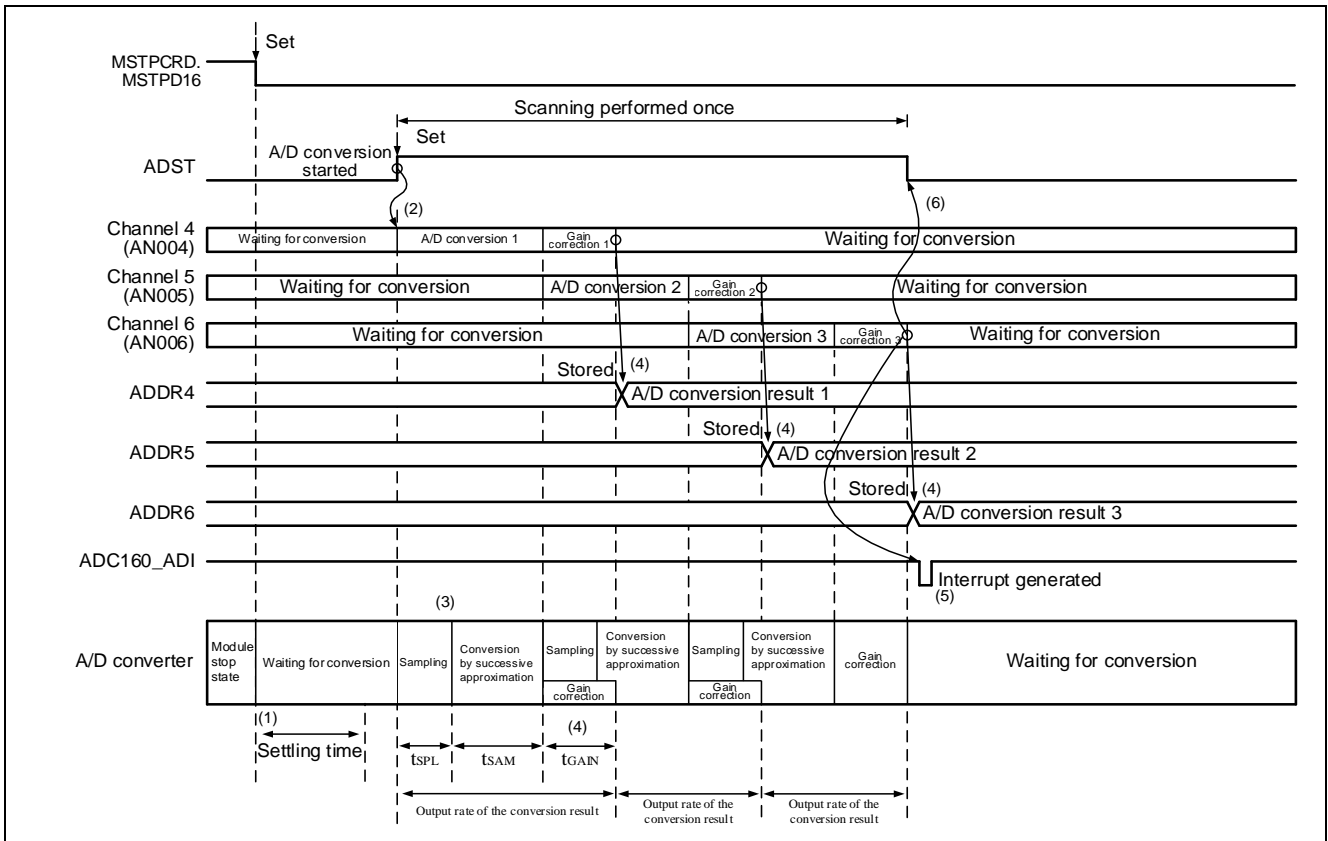
If the sampling time is not sufficient due to the high impedance of an analog input signal source, the sampling time can be increased by adjusting the ADSSTRn register. Similarly, if the A/D conversion clock (ADCLK) is slow, sampling time can be adjusted by decreasing value in the ADSSTRn register.

The  $t_{\text{SAM}}$  is 18 ADCLK states and the  $t_{\text{GAIN}}$  is 10 ADCLK states.

Settling time is the wait time required from the time of releasing the module-stop state until A/D conversion is started. If you want to wait for settling time by hardware, set the value obtained by adding the sampling time and settling time to the ADSSTR register.

Figure 3 shows an example of operation of the A/D converter when AN004 to AN006 are selected in single scan mode.

1. Wait for settling time to start A/D conversion after release from the module-stop state. If you want to wait for settling time by hardware, set the value obtained by adding the sampling time and settling time to the ADSSTR register.
2. When the ADST bit in ADCSR register is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. The A/D converter samples the analog input for the time set by ADSSTRn register, and conversion by successive approximation. Then, gain correction is performed.
4. Each time A/D conversion and the gain correction is complete, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy). The same storing operation is also performed in continuous scan mode and group scan mode. Gain correction occurs concurrently with sampling, and the gain correction time affects the A/D conversion processing time only in the first cycle of single scan, continuous scan, and group scan. Gain correction time ( $t_{\text{GAIN}}$ ) does not affect the second and later cycles.
5. When A/D conversion and the gain correction of all the selected channels completes, an ADC160\_ADI interrupt request is generated.
6. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically set to 0 when A/D conversion and the gain correction of all the selected channels completes. The ADC16 then enters a wait state.



**Figure 3. A/D Converter Operation Example When AN004 to AN006 are Selected in Single Scan Mode**

### 2.3 Linearity Parameters

INL, DNL, offset error, and gain error are used as representative indicators for accuracy and error of the A/D converter.

**INL: Integral non-linearity (LSB)**

The maximum deviation between the ideal line and the actual output code when the measured offset and full-scale errors are zeroed.

**DNL: Differential nonlinearity (LSB)**

The difference between 1 LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

**Offset error (LSB)**

The difference between the transition point of the ideal 0x0000h output code and the actual 0x0000h output code.

**Gain error (LSB)**

The difference between the transition point of the ideal 0x7FFFh (or 0x8000h) output code and the actual 0x7FFFh (or 0x8000h) output code.

The definitions of an LSB are shown in Equation 1 and 2, and the output range of A/D conversion result is shown in Table 3.

Single-ended Input Mode

$$\text{Equation 1: } 1\text{LSB} = \frac{(VREFH0 - VREFHL0)}{2^{15}}$$

Differential Input Mode

$$\text{Equation 2: } 1\text{LSB} = \frac{2 \times (VREFH0 - VREFHL0)}{2^{16}}$$

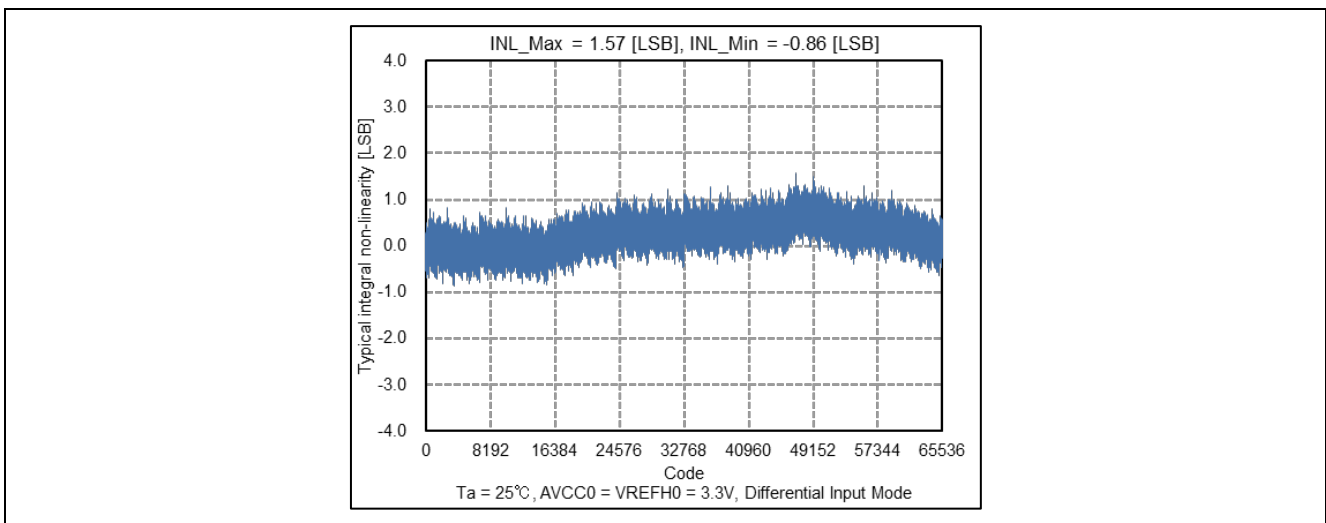
For example, 1 LSB is 100.7  $\mu\text{V}$  at  $VREFH0 = 3.3\text{ V}$  and  $VREFL0 = 0\text{ V}$  in differential input mode.

**Table 3. A/D Conversion Result Output Ranges**

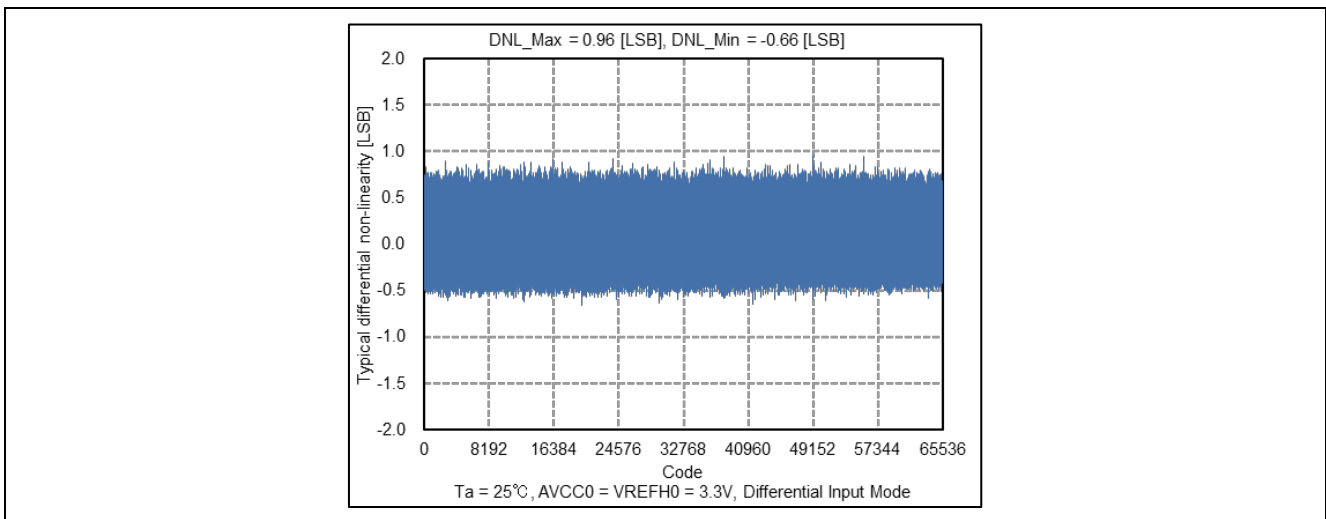
Input Mode	A/D conversion	ADCER.ADINV (Data Inversion)	Output Range
Single-end Input Mode	Temperature sensor	x	0 to $2^{15} - 1$
	Internal reference voltage		
	AN008, AN016 to AN023, SBIAS/VREFI		
	AN000, AN002, AN004, AN006	1	
	AN001, AN003, AN005, AN007	0	$-2^{15}$ to 0
Differential Input Mode	AN000, AN001, AN002, AN003, AN004, AN005, AN006, AN007	x	$-2^{15}$ to $2^{15} - 1$
-	Self-diagnosis	x	$-2^{15}$ to $2^{15} - 1$

x: Don't care

Note: A/D conversion result of odd channels AN000 to AN007 in single-ended mode can be inverted according to the ADCER.ADINV bit setting value. Therefore, the A/D conversion results can be stored in the A/D data registers in the same output range as even channels AN000 to AN008 or AN016 to AN023.



**Figure 4. INL versus Code**



**Figure 5. DNL versus Code**

## 2.4 Dynamic Parameters

SINAD or ENOB is very important in many applications because it describes the smallest input signal that the converter can resolve. In closed loop systems, detecting small changes in input signals allows better control loop performance.

SINAD: Signal-to-noise and distortion (dB)

RMS level of input signal/sum RMS value of all noise and distortion excluding DC

ENOB: Effective number of bits

$$\text{ENOB} = (\text{SINAD} - 1.76 \text{ dB}) / 6.02 \text{ dB}$$

THD: Total Harmonic Distortion (dB)

Root-sum-square (RMS) value of the harmonics produced by the A/D converter relative to the RMS level of a sinusoidal input signal near full-scale.

THD is calculated up to 5<sup>th</sup> order harmonic distortion.  $\text{THD} = \text{HD2} + \text{HD3} + \text{HD4} + \text{HD5}$ .

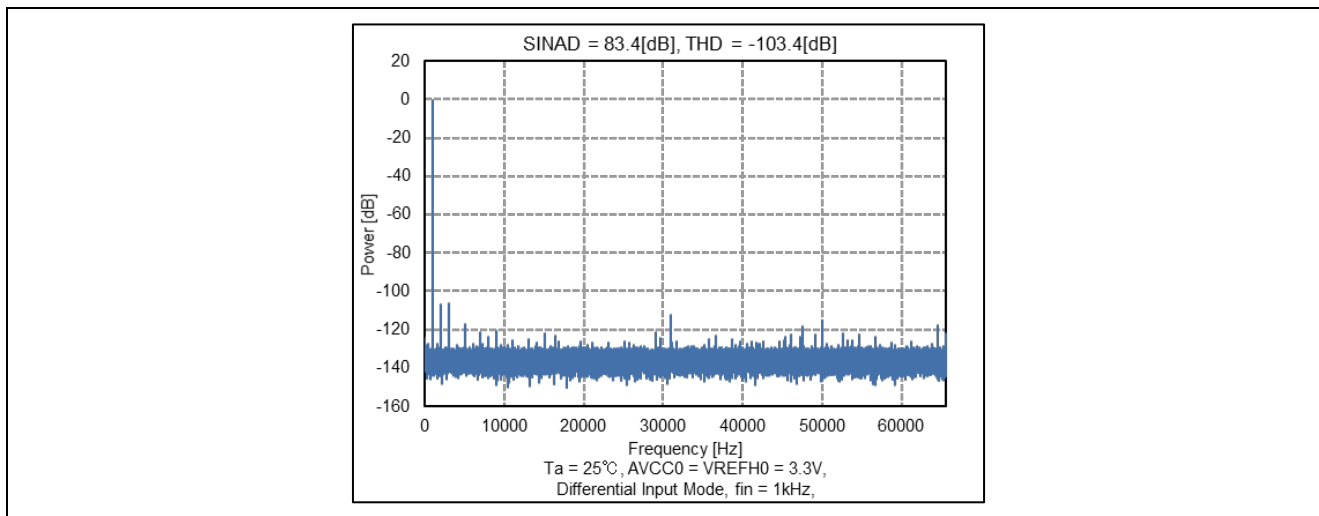
### 2.4.1 Improving Accuracy by Averaging A/D Conversion Result

The 16-Bit A/D Converter has a function for averaging the results of A/D conversion. A/D conversion is performed multiple times consecutively, and the result is averaged. This can suppress the influence of sudden noise and improve the accuracy of the conversion result.

**Table 4. SINAD and ENOB Characteristics Evaluation Results of 16-Bit A/D Converter**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = VREFH0 = 3.3 \text{ V}$  or  $5.0 \text{ V}$ ,  $V_{SS} = AVSS0 = AVSS1 = VREFL0 = 0 \text{ V}$ ,  $f_{in} = 1 \text{ kHz}$ , External clock input used.

Parameter	Symbol	Typ		Unit	Test Conditions
		AVCC0 = 3.3 V	AVCC0 = 5.0 V		
Signal-to-noise and distortion	SINAD	83.4	85.3	dB	Differential input, No averaging
		86.1	87.8		Differential input, 2 times average
		88.5	90.0		Differential input, 4 times average
		90.8	91.8		Differential input, 8 times average
		92.9	92.9		Differential input, 16 times average
		77.4	80.0		Single input, No averaging
		Effective number of bits	ENOB		13.6
14.0	14.3			Differential input, 2 times average	
14.4	14.7			Differential input, 4 times average	
14.8	15.0			Differential input, 8 times average	
15.1	15.1			Differential input, 16 times average	
12.6	13.0			Single input, No averaging	



**Figure 6. FFT of 8x Decimated ADC Output**

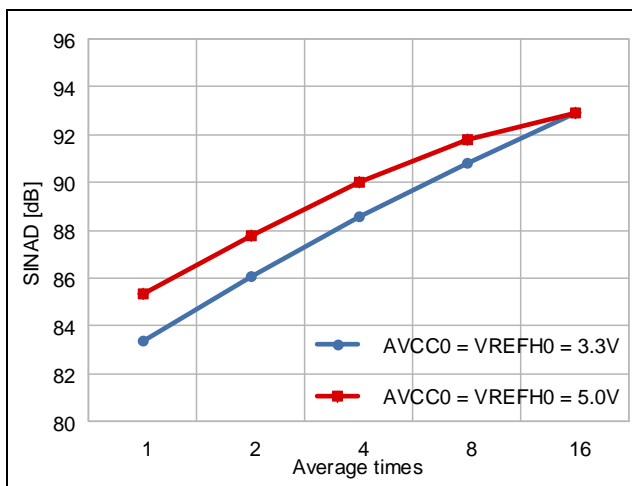


Figure 7. SINAD versus Average Times

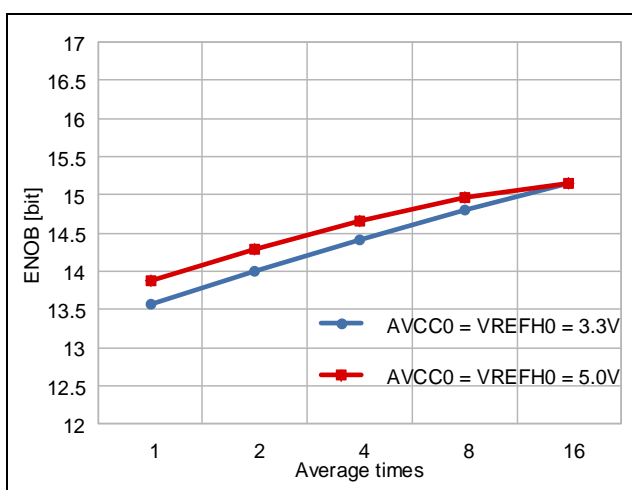


Figure 8. ENOB versus Average Times

## 2.5 Operating and Standby Current

Table 5 to Table 6 show operating current evaluation results of the A/D converter module stop state, A/D conversion wait state, and A/D conversion state.

**Table 5. Operating Current Evaluation Result in A/D Conversion Wait State**

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V, HOCO clock oscillation frequency = 32 MHz, PCLKD = 32 MHz, MSTPCRD.MSTPD16 = 0b, ADCSR.ADST = 0b

Parameter	Symbol	Typ	Unit	Test Conditions
Analog power supply current	I <sub>AVCC0</sub>	598	μA	-
Reference power supply current	I <sub>VREFH0</sub>	17.2	μA	-

**Table 6. Operating Current Evaluation Result in A/D Conversion State**

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V, HOCO clock oscillation frequency = 32 MHz, PCLKD = 32 MHz, MSTPCRD.MSTPD16 = 0b, ADCSR.ADST = 1b

Parameter	Symbol	Typ	Max	Unit	Test Conditions
Analog power supply current	I <sub>AVCC0</sub>	989	1204	μA	-
Reference power supply current	I <sub>VREFH0</sub>	37.5	67.3	μA	-



### 3. Calibration Function

Calibration allows high-precision A/D conversion by obtaining the capacitor array D/A converter (C-DAC) linearity error correction coefficient and gain (offset) error correction coefficient from the internally generated analog input under usage conditions.

All correction coefficients are derived using special ultra-high-precision equipment for 16-bit A/D converter only and are stored in the microcontroller's flash memory at the time of factory shipment. ADC16 characteristics described in the *MCU User's Manual* are realized by automatically loading the correction coefficient at microcontroller startup.

There are two additional ways to improve the characteristic:

1. Correct offset error and gain error.
2. Re-derive all correction coefficients.

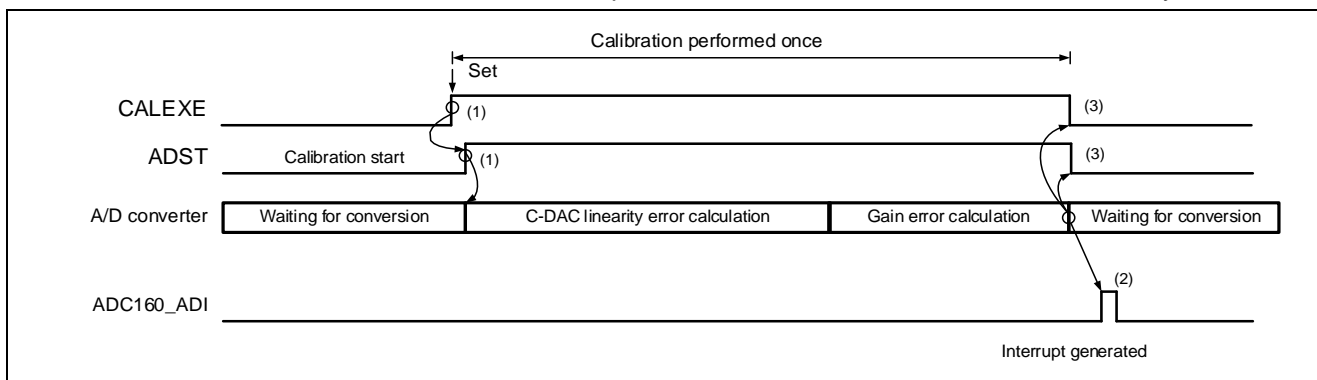
When temperature and supply voltage change, it is possible to correct offset error and full-scale error by using 3 level self-diagnostic A/D conversion results. The offset is obtained by `ADRST.DUAGST=10` and the gain error by `ADRST.DUAGST= 01` or `11`. The linearity errors of the C-DAC are not dependent on temperature and voltage. Since one-time self-diagnostic conversion results fluctuate, average the conversion results of several tens or more values to obtain the accurate offset error and full-scale error.

In order to re-derive all correction coefficients, the `ADCALEXE.CALEXE` bit is set to 1 and calibration starts. Calibration time is a little longer, about 24 ms at `ADCLK = 32 MHz`. When using the calibration function, be sure to perform in an environment where the analog block power supply, reference power supply, and `ADCLK` are stable. If calibration is performed in an unstable environment, A/D conversion accuracy might deteriorate more than at the time of shipment.

#### 3.1 Calibration Flow

Figure 9 shows the calibration operation.

1. When the `ADCSR.ADST` bit becomes 1 (A/D conversion start) by writing 1 to `ADCALEXE.CALEXE` bit with software, the correction values for C-DAC linearity error and GAIN error are calculated.
2. When calculation of all correction values completes and the `ADICR.ADIC[1:0]` bits are set to 11b (`ADC16_ADI` interrupt due to calibration end enabled), an `ADC16_ADI` interrupt request is generated.
3. The `ADCSR.ADST` bit remains 1 (A/D conversion start) during calibration and is automatically cleared to 0 when calculation of all correction values completes and the A/D converter enters the standby state.



**Figure 9. Calibration Operation (C-DAC Linearity Error Calculation and Gain Error Calculation) Example**

Figure 10 shows the software flow and an operation example.

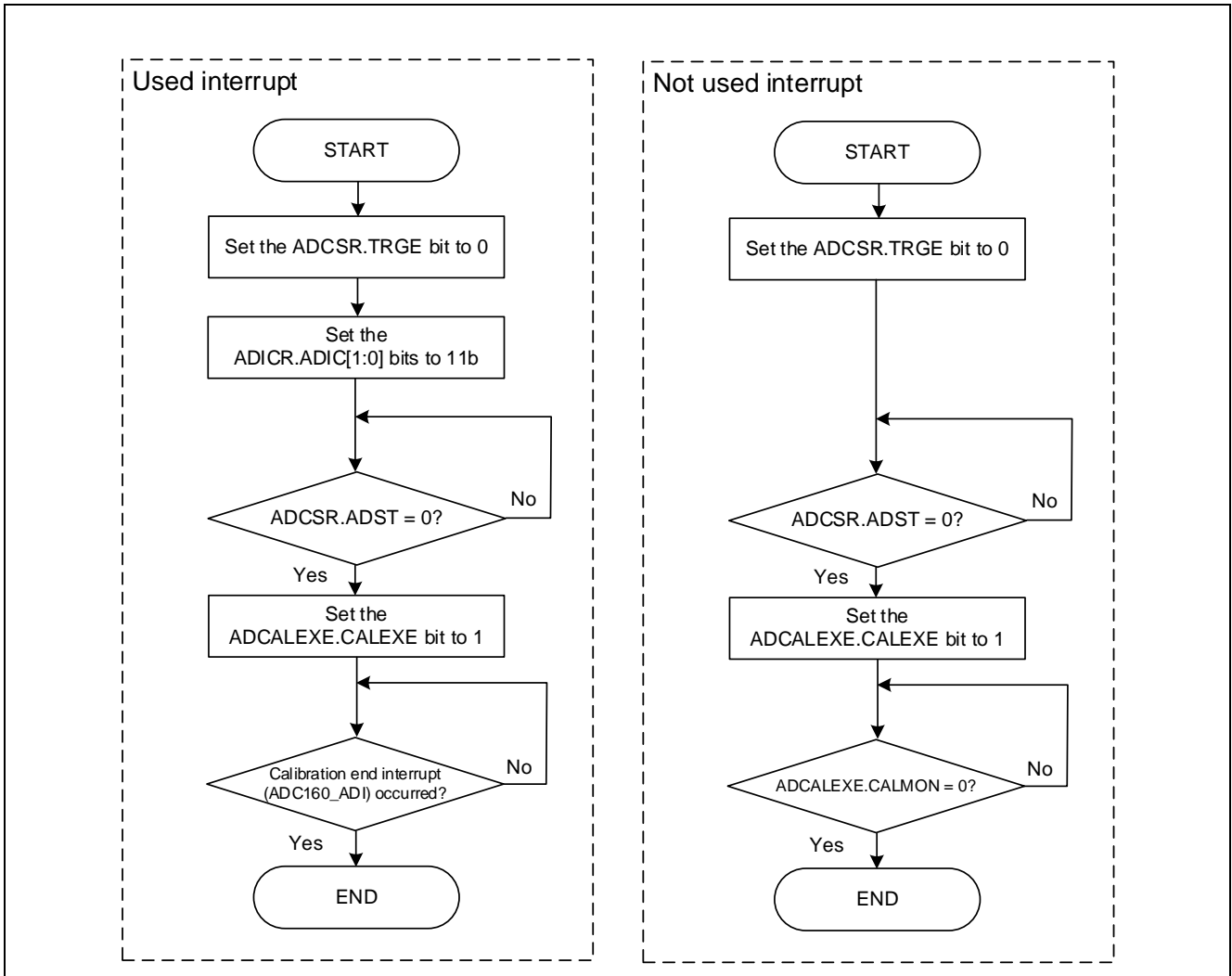


Figure 10. Software Flow and Calibration Operation Example

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**Revision History**

Rev.	Date	Description	
		Page	Summary
1.00	Dec.19.19	—	Initial release

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