Achieving Compatibility Between the Intel i960 and the RC32364 Embedded Microprocessor

Application Note AN-155

RISController

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Introduction

The IDT79RC32364 is a new low-cost, low-power member of the Integrated Device Technology, Inc. (IDT) RISController™ series of Embedded Microprocessors. The RC32364 is a 32-bit architecture with a flexible bus interface, allowing the CPU to interface with low-cost memory and I/O systems which facilitates simple, low-cost designs.

This application note reviews signal compatibility between the RC32364 and the Intel i960 processor family and is provided for those interested in using i960 interface chips with the RC32364 device.

Address/Data Bus Compatibility

The i960 family includes the 80960JA/JF and 80960CA 32-bit embedded processors as well as the 80960HA/HD/HT 32-bit superscalar processors. For these devices, both the Address and Data bus interfaces are as follows:

- 80960JA/JF: Multiplexed
- 80960CA: De-multiplexed
- 80960HA/HD/HT: De-multiplexed

Because the RC32364 has a 32-bit Multiplexed Address and Data bus, the greatest similarity exists between the RC32364 and the 80960JA/JF processors.

Signal Compatibility

Most of the signals generated by the RC32364 and the i960 processors are compatible. Any signal incompatibilities are a result of architectural differences and can, in most cases, be corrected by workarounds implemented through minimal glue logic functions, which are included in the signal discussions that follow.

Note: Equations are in AHDL syntax.

AD[31:0] Address/Data Bus

RC32364: During the Address phase, the processor asserts Address A[31:4] on AD[31:4] and transfer size information on AD[3:0]. During the data phase, the processor asserts/samples Data D[31:0] on AD[31:0].

AD[3:0]	Total Bytes Transferred	Number of Transfers for Various Bus Widths		
		8-bit	16-bit	32-bit
0000	16	16	8	4
0001	1	1	1	1
0010	2	2	1	1
0011	3	3	2	1
0100	4	4	2	1
All other combinations are reserved for future use.				

Table 1. RC32364 AD[3:0] Byte Transfer Size for 8-, 16-, and 32-bit Bus Widths

i960JA/JF: During the address phase, the i960JA/JF asserts Address A[31:2] on AD[31;2] and Transfer Size Information on AD[2:0]. During the data phase, the processor asserts/samples Data D[31:0] on AD[31:0].

AD[1:0]	Transfers	Total Bytes Transferred for Various Bus Widths		
		8-bit	16-bit	32-bit
00	1	1	2	4
01	2	2	4	8
10	3	3	6	12
11	4	4	8	16
Irrespective of the bus width, the i960JA/JF always specifies the number of transfers,				

Table 2. i960 AD[1:0] Byte Transfer Size for 8-, 16-, and 32-bit Bus Widths

Differences: With regards to the size and number of transfers, there is an incompatibility between the RC32364 and the i960: The i960 does 1 to 4 transfers, irrespective of the bus-port width. The RC32364 does 1 to 16 transfers, irrespective of the bus-port width.

Workaround: This is an architectural difference. The RC32364 does offer the additional capability of 16 transfers for each available bus width.

Note though that all of the RC32364's interface logic state machines can make use of the signal Last*, to determine the size of the transfer or detect the last transfer of the burst. However, the i960CA or i960HA/HD/HT processors make use of the BLAST/ signal, to determine the last transfer of the burst access.

ALE (Address Latch Enable)

The Address Latch enable signal is used to latch the address during the Address phase of the transfer.

RC32364: During the Address phase, the processor asserts Address A[31:4] on AD[31:4], and Transfer Size information on AD[3:0] and the ALE signal.

i960JA/JF: These processors have the ALE signal in two polarities, ALE and ALE/.

Differences: The RC32364 has only the ALE signal. If ALE/ is required, it can be inverted. But care must be taken with regard to the hold time of Address.

ADS* (Address Strobe)

RC32364: Indicates valid address and the start of a new transfer. ADS* is asserted for the entire Address cycle.

i960JA/JF, i960CA or i960HA/HD/HT: The address strobe signal has the same definition in these processors.

Differences: None.

Workaround: None required.

A[3:2] (Address[3:2])

RC32364: Non-Multiplexed address lines that are used during the data phase of Burst transfers provide partial address increments during the burst data phase.

i960JA/JF: This signal has the same definition in these processors.

Differences: None.

Workaround: None required.

BE[3:0]* (Byte Enables)

RC32364: Byte Enable is used to validate the bytes during the data phase. This information depends upon the memory region's bus size as follows:

32-bit bus:
BE3* enables data on AD31:24
BE2* enables data on AD23:16
BE1* enables data on AD15:8
BE0* enables data on AD7:0

16-bit bus:
BE3* enable data on AD15:8
BE2* is not used (state is undefined)
BE1* becomes Address Bit 1 (A1)
BE0* enables data on AD7:0

8-bit bus:
BE3* is not used (state is undefined)
BE2* is not used (state is undefined)
BE1* becomes Address Bit 1 (A1)
BE0* becomes Address Bit 0 (A0)

i960JA/JF: This signal has the same definition in these processors.

i960CA or i960HA/HD/HT: This signal has the same definition in these processors.

Differences: None.

Workaround: None required.

Width[1:0] (Bus Width)

RC32364: Indicates the I/O or Memory port width encodings for a transfer. The valid sizes are as follows:

Width[1:0]	Bus Size
00	8-bit
01	16-bit
10	32-bit
11	Reserved

Table 3. Transfer Bus Widths for RC32364

i960JA/JF: Indicates the I/O or Memory port width for a transfer. The valid sizes are as follows:

Width[1:0]	Bus Size
00	8-bit
01	16-bit
10	32-bit
11	Processor Halt

Table 4. Transfer Bus Widths for RC32364

Differences: Except for '11', all other encodings are compatible. The RC32364 reserves the '11' encoding, whereas '11' in the i960 processors specifies the processor HALT status.

Workaround: This is an architectural difference between the processors and no workaround exists. **Note:** The RC32364 will not assert '11', which is reserved for future 64-bit mode.

D/C* (Data/Code)

RC32364: Indicates instruction fetch or data transfer:

0 - Data transfer.
1 - Instruction fetch.

i960JA/JF: Indicates an instruction fetch or data transfer:

0 - Instruction fetch.

1 - Data transfer.

Differences: A signal inversion.

Workaround: A simple inverter can be used to invert this signal.

i960CA or i960HA/HD/HT: Same as i960JA/JF.

W/R* (Write/Read)

RC32364: This processor has separate Rd* and Wr* signals, to indicate whether the current transfer is a Read or a Write.

i960JA/JF: This processor has dual function R/W* signal.

0 - Read transfer.

1 - Write transfer.

Differences: one signal verses two.

Workaround: Rd* can be used as W/R* of i960.

i960CA or i960HA/HD/HT: Same as i960JA/JF.

DT/R* (Data Transmit/Receive)

RC32364: Indicates the direction of data transfer to and from the address/data bus.

i960JA/JF: This signal has the same definition.

i960CA or i960HA/HD/HT: This signal has the same definition.

DEN* (DataEnable)

RC32364: Indicates data phase during the bus transfer.

i960JA/JF: This signal has the same definition.

i960CA or i960HA/HD/HT: This signal has the same definition.

BLAST* (Burst Last)

RC32364: Last* Indicates that the current data transfer is the last data transfer of the burst.

i960JA/JF: This signal has the same definition.

i960CA or i960HA/HD/HT: This signal has the same definition.

RDYRCV (Ready/Recover)

RC32364: This processor has ACK* signal that is functionally equal. This input is used to terminate the current transfer.

i960JA/JF: This is a dual function signal that is used to terminate the current bus transfer and to insert additional bus turnaround cycles, after the completion of the current bus access.

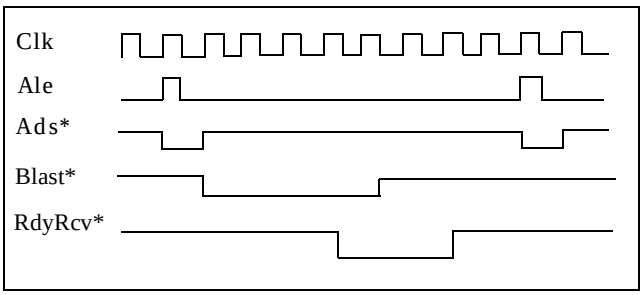

Figure 1. Timing Diagram of the i960JA/JF Ready/Recover Signal

i960CA or i960HA/HD/HT: This pin has the same definition as the RC32364.

Workaround: Because the RC32364 and i960CA or i960HA/HD/HT processors have the same pin definitions, this signal can be directly connected. However, in the case of interfacing an i960JA/JF I/O, to avoid spurious termination of the next new bus cycle, the RC32364's Bus TurnAround (BTA) Control Register must be properly programmed, as stated in the RC32364 user's manual.

LOCK*/ONCE* (Bus Lock)

RC32364: This processor does not have any equivalent signals.

i960JA/JF: This signal should be tied high in the interface logic.

i960CA or i960HA/HD/HT: This signal should be tied high in the interface logic.

HOLD/HOLDA, BSTAT (Hold/Hold Acknowledge, Bus Status)

RC32364: This processor has BusReq* and BusGnt* signals, to arbitrate sharing of the local bus with the External agent.

i960JA/JF: This processor has HOLD, HOLDA and BSTAT signals for the same purpose. These signals are not compatible.

Workaround: An extra logic function is required to make them compatible.

(Equations are in AHDL)

```
-- RC32364 signals

BusReq*: OUTPUT;
BusGnt*: INPUT;
CLK: INPUT;

-- i960JA/JF signals

HOLDA, BSTAT: OUTPUT;
HOLD: INPUT;
```

```
-- Equations

BusReq*     = !HOLD;
BusReq*.CLK = CLK;
HOLDA       = !BusGnt* & HOLD #
HOLDA & HOLD;
HOLDA.CLK   = CLK;

BSTAT = HOLD & HOLDA & BusGnt*;
BSTAT.CLK = CLK;
```

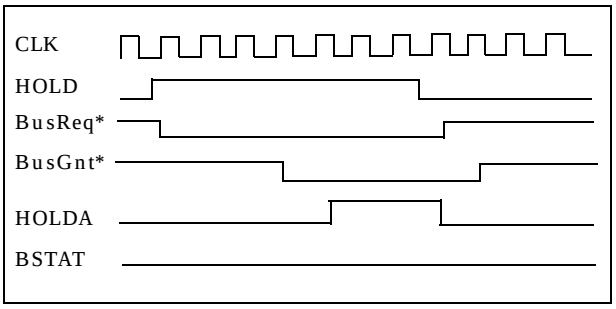

Figure 2. Normal Protocol

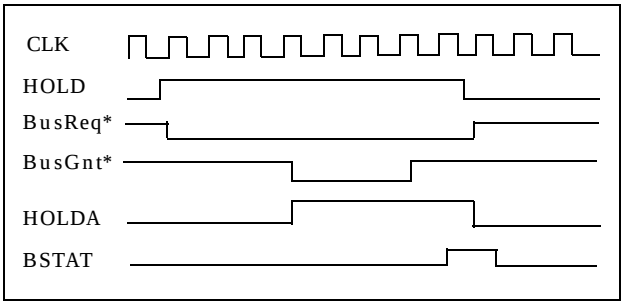

Figure 3. CPU Initiated Bus Grant Deassertion

i960CA or i960HA/HD/HT: These processors have HOLD, HOLDA and BREQ signals for the same purpose. These signals are not compatible.

Workaround: (Equations are in AHDL)

```
-- RC32364 signals

BusReq*: OUTPUT;
BusGnt*: INPUT;
CLK: INPUT;

-- i960CA or HA/HD/HT signals

HOLDA, BREQ: OUTPUT;
HOLD: INPUT;

-- Equations

BusReq*     = !HOLD;
BusReq*.CLK = CLK;
HOLDA       = !BusGnt* & HOLD  #
HOLDA & HOLD;
HOLDA.CLK   = CLK;

BREQ = HOLD & HOLDA & BusGnt*;
BREQ.CLK= CLK;
```

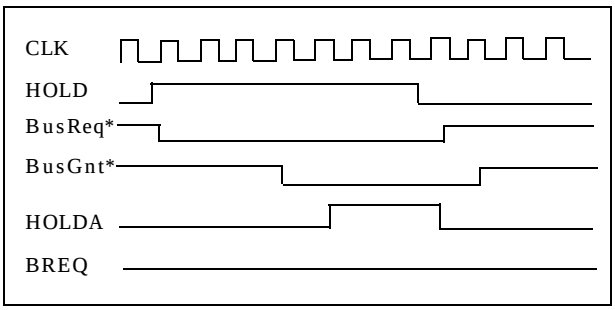

Figure 4. Normal Protocol

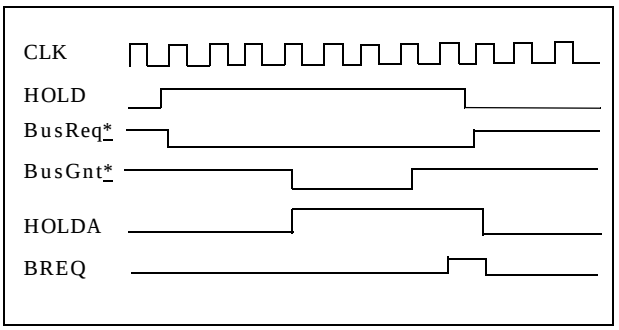

Figure 5. CPU Initiated Bus Grant Deassertion

CLKIN (Clock Input)

RC32364: In the RC32364, the Masterclock signal is a bus input clock and provides the timing base.

i960JA/JF or i960CA or i960HA/HD/HT: These processors have the CLKIN signal, which provides their timing base.

Workaround: None necessary. These signals are compatible.

RESET* (RESET)

RC32364: The RC32364 has two RESET signals: ColdReset*—used only for power-on reset—and Reset*—used for both power-on and warm resets. During power-on, processor initialization settings are implemented through the boot-mode configuration settings listed in Table 5.

For more detailed information on these two RESET signals, refer to the RC32364 Data Sheet, available from IDT.

i960JA/JF: These processors have only one RESET signal. The RESET* pin has an internal synchronizer. During power-on, both Vcc and the RESET* signal must be stable for a minimum of 10,000 CLK cycles. On a warm reset, the RESET* signal should be asserted for a minimum of 15 cycles.

Workaround: No simple workaround is possible. It is better to design separate logic functions using an EPLD. For more details, refer to the RC32364 data sheet.

Boot-Mode Configuration Settings

Pin	Mode Bit	Description	Value	Mode Setting	Logic
PCST[2:0]	2:0	Pipe-line clock Multiplier X Mclk	0 1 2 3 4 5 6 7	x2 x3 x4 x5 x6 x7 x8 Reserved	Pull-up or Pulldown resistors
PCST[3]	3	Endian	0 1	Little Big	Pull-up or Pull-down Resistor
PCST[4]	4	PLLDIS Disable PLL	0 1		Pull-up or Pull-down Resistor
BusGnt*	5	VCOCAP Slow down PLL	0 1		Pull-up or Pull-down Resistor
Int[1:0]*	7:6	Timer Int Enable	10 11 00 01	100% strength (fastest) 83% strength 67% strength 50% strength (slowest)	Wired or logic with Interrupt0
Int[3:2]*	9:8	Boot PROM Width	00 01 10 11	8 bit 16 bit 32 bit Reserved	Wired or logic with Interrupt 2 and 3

Table 5. RC32364 Boot-Mode Configuration Settings

i960CA or i960HA/HD/HT: For these processors, the RESET* signal is not compatible, and it is better to design separate logic functions using an EPLD.

INTERRUPTS

RC32364: The RC32364 has six active low interrupt inputs.

i960JA/JF or i960CA or i960HA/HD/HT: These processors have eight interrupt inputs that operate in the following three modes:

- Dedicated Mode. In this mode, each pin can be programmed to be level(low) or edge(falling) sensitive.
- Expanded Mode. All eight pins act as vectored interrupt sources.
- Mixed Mode. The XINT[7:5]* acts as a dedicated source, and the XINT[4:0]* acts as the five most significant of a vectored source. The least significant bits of the vectored source are set to 010 internally.

Workaround: Only the dedicated mode with the level sensitive option is possible. The two additional inputs must be wired-ored.

NMI (Non Maskable Interrupt)

This pin is compatible between the i960 processors and the RC32364, and it can be connected directly.

STEST (Self Test)

RC32364: The RC32364 has Cache Test mode input, which can be connected to the Self Test pin of the i960JA/JF or i960CA or i960HA/HD/HT processors; however, this signal is not completely compatible. For more details, refer to the RC32364 data sheet.

i960JA/JF or i960CA or i960HA/HD/HT: The self test signal causes the processor's internal self-test feature to be enabled or disabled at initialization.

Workaround: None required.

FAIL* (FAIL)

RC32364: The RC32364 does not have an equivalent pin.

i960JA/JF or i960CA or i960HA/HD/HT: Fail* indicates that a failure of the processor's built-in self test occurred during initialization.

Workaround: The FAIL* signal of the i960 support chip can be tied high.

JTAG SIGNALS

RC32364: The RC32364 has an Enhanced JTAG (EJTAG) interface feature, which is a superset of the standard JTAG debugging system.

i960JA/JF or i960CA or i960HA/HD/HT: The i960 processors have the standard JTAG interface feature.

Workaround: None required.

ONCE* (On-Circuit Emulation)

RC32364: The RC32364 has its own version of enhanced JTAG, with an on-chip In-Circuit Emulation (ICE) feature.

Workaround: None required.

BTERM* (Burst Terminate)

RC32364: The RC32364 has the RETRY* input signal that forces the processor to retry the bus cycle, during the beginning of a read cycle or at any stage of a write.

I960JA/JF or i960CA or i960HA/HD/HT: The BTERM* signal is used to terminate the burst access in progress. When BTERM* is asserted, the current cycle is terminated and a new Address cycle begins.

Workaround: With the exception that an i960 Read Burst can only be terminated if no data is supplied to the processor, the signals are similar.

WAIT*

RC32364: The RC32364 does not have a signal that provides this information.

i960JA/JF or i960CA or i960HA/HD/HT: The Wait* signal indicates internal wait-state generator status.

Workaround: None possible or required.

LOCK* (Bus Lock)

RC32364: The RC32364 does not have a Read-Modify-Write Instruction, to generate this signal.

i960JA/JF or i960CA or i960HA/HD/HT: The LOCK* signal indicates that an atomic read-modify-write operation is in progress.

Workaround: None possible.

BOFF* (Bus Backoff)

RC32364: The RC32364 does not have any comparable signals, and the BusReq* and BusGnt* operations are the only way to relinquish bus control.

i960JA/JF or i960CA or i960HA/HD/HT: The BOFF* signal suspends the current access and causes the bus pins to float.

Workaround: None possible.

DMA*, DREQ3:0, DACK3:0, EOP/TC3:0

RC32364: The RC32364 does not have an on-chip DMA controller.

Workaround: None possible.

SUP* (Supervisor Access)

RC32364: The RC32364 does not indicate SUPERVISORY or USER mode implementation.

i960JA/JF or i960CA or i960HA/HD/HT: The Supervisor Access signal indicates whether or not the bus request is issued while in supervisor mode.

Workaround: A31 of the RC32364 processor can be inverted to connect to the SUP* signal of the i960 interface chip. To achieve this feature, program the UM, EXL, and ERL fields of the RC32364's Status Register. For more details, refer to the RC32364 user's manual.

CLKMODE (Clock Mode)

RC32364: During RESET in the RC32364, various Clock Mode selections can be made through the Mode Bits.

i960CA: CLKMODE selects the division factor to be applied to the external clock's input (CLKIN) frequency.

Workaround: None required.

PCLK2:1 (Processor Output Clocks)

RC32364: No clock outputs are provided from the internal PLL of the RC32364.

i960CA: This signal provides a timing reference for all processor inputs and outputs.

Workaround: None possible.

DP3:0 & PCHK (Data Parity & Parity Check)

RC32364: Parity check operations can not be performed in the RC32364.

i960HA/HD/HT: Data Parity carries parity information for the data bus, and Parity check indicates the result of a parity check operation.

Workaround: None possible.

CT3:0 (Cycle Type)

RC32364: In the RC32364, information on bus cycle types is not provided.

i960HA/HD/HT: The cycle type signal indicates the type of bus cycle currently being started or the processor state.

Workaround: None possible.

Conclusion

In this application note, interface signal compatibility has been compared between the Intel i960 processor family and the IDT79RC32364 MIPS RISC processor.

As has been shown, many of the interface signals between these processors are completely compatible and no changes are required; however, to resolve the incompatibility issues that do exist, some glue logic is necessary, which has also been provided.

Therefore, use of the implementations discussed can eliminate incompatibility issues, so depending upon function requirements, using the i960 support chips with the IDT79RC32364 processor should be relatively simple.

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