THE MYTH OF GROUND BOUNCE MEASUREMENTS AND COMPARISONS

APPLICATION NOTE AN-147

By Stanley Hronik

INTRODUCTION

Ground Bounce is one of the primary causes of false switching in high speed components and is a major cause of poor signal quality. While ground bounce is easily measured on CMOS components, an accurate measurement is somewhat elusive on bipolar or BiCMOS components. For components with a bipolar or BiCMOS output structure, any reading obtained through standard ground bounce tests will be several hundred milivolts low. This is due to the inability of these components to hold a solid logic low level with low impedance.

The accompanying characteristic of Vcc bounce is less troublesome than ground bounce, but will have a greater influence as Vcc levels drop to 3.3V, 2.5V and lower. Vcc bounce is easily measured only on components that have a CMOS rail swing output. Since there is no direct connection to Vcc in any component except components with CMOS rail swing outputs, the measurement of Vcc bounce is not directly possible in many standard logic families.

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GROUND BOUNCE DESCRIPTION

Ground Bounce is a voltage oscillation between the ground pin on a component package and the ground reference level on the component die. Essentially it is caused by a current surge passing through the lead inductance of the package. The effect is most pronounced when all outputs switch simultaneously, (hence the alternate name, Simultaneous Switching Noise). While the inductance is the combined effect of the package lead, the package lead frame, the bond wire and the inductance in the die pad, most of the inductance is caused by the bond wire.

Figure 1 shows a typical waveform for a high speed CMOS component with TTL level outputs. Shown directly above the signal waveform on the same time scale is the voltage seen on the ground of the die relative to the external ground. Directly above that is the voltage seen on the die Vcc relative to the external Vcc on the board.

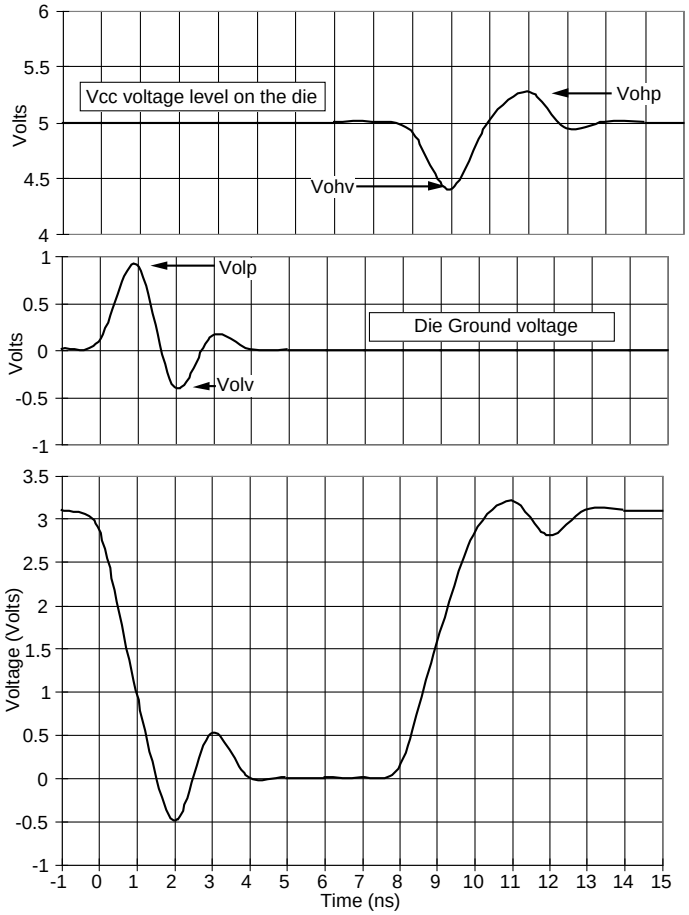

Figure 1, Ground Bounce

As shown in Figure 1, ground bounce and Vcc bounce cause signal degradation in the output waveform of the device. This consists of an undershoot and overshoot on both the rising and falling edges of the waveform.

There are four parameters for measuring ground bounce and Vcc bounce which are identified in Figure 1. In the order of significance they are:

Volp — peak voltage of the ground bounce,
Volv — valley voltage of the die ground during bounce
Vohv — negative voltage change in Vcc during bounce
Vohp — peak voltage change in Vcc during bounce

When reading specifications for ground bounce, the parameter most often used to identify the ground bounce level is Volp. In statements such as "Ground Bounce = XX volts", this is the parameter being referenced.

Ground Bounce levels are typically more pronounced than Vcc Bounce levels because of the HIGH to LOW transition is trying to quickly bring a HIGH signal down to a narrow window of <400mV for a logic LOW. A low output impedance is required to complete the transition quickly. In the LOW to HIGH, the only requirement is that the output be above 2.4V. 5V is available as a driving voltage. A much lower pull up impedance is required to make the transition quickly.

The Ground Bounce Effect in CMOS

The output structure for a CMOS component with TTL level outputs is shown in Figure 2. In addition to the structure shown, the output contains resistors in most components which will dampen the output waveforms and reduce the effects of ground bounce and Vcc bounce. In order to simplify the drawings and discussion, these have been eliminated from the drawing.

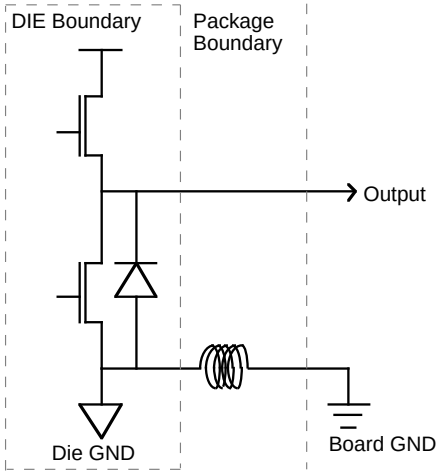

Figure 2, CMOS Device Output Structure

There is a clamp diode between the device output and the Die GND on all CMOS components. In ground bounce discussions, this clamp diode can be ignored. During HIGH to LOW transitions, the pull down FET will be at a very low impedance from drain to source. Transitions of the Output below ground will be caused by a voltage drop across the lead inductance and will not forward bias the clamp diode.

Figure 3 shows the VI curve for a typical FCT High Drive CMOS component with TTL output levels. The curve is very flat at 6.5Ω throughout the operating region around zero volts. This flatness continues below zero until the effect of the clamp diode to Die GND takes effect at about -0.7V.

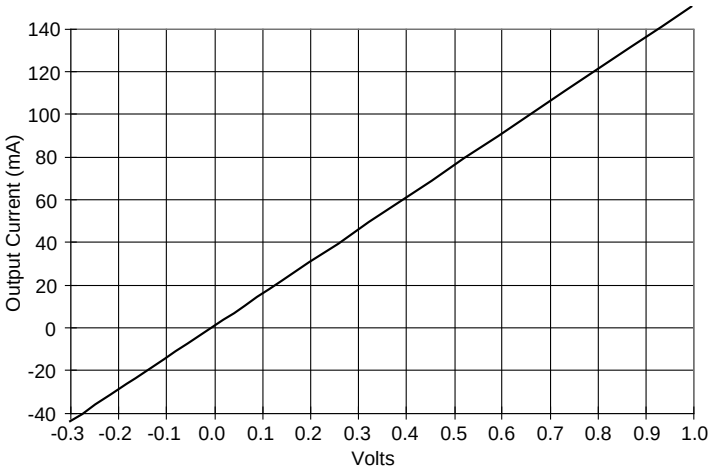

Figure 3, FCT Output VI Curve for Vol

As a CMOS component makes a transition from a HIGH to a LOW as shown in Figure 4, the pull down FET will lock (6.5Ω impedance) the device output to Die GND in Figure 2. To accomplish this task, the pull down FET will be required to discharge the internal capacitances of the die. This causes a sudden surge of current from the Die GND to the Board GND. The current surge then causes a voltage drop across the ground lead inductance. If all device outputs switch simultaneously, the instantaneous current through the ground lead inductance can be significant.

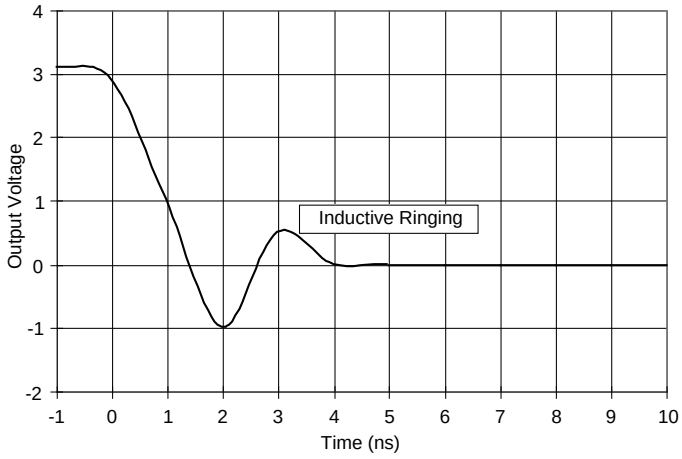

Figure 4, Undershoot in CMOS from Ground Bounce

Figure 4 shows the waveform visible to the outside world from a HIGH to LOW transition. The transition is clean from the Voh level to zero, but the lead inductance continues to cause ringing. With an N-Channel FET pull down, the output will be tied closely to the Die GND regardless of whether the Die GND is above or below the Board GND.

The Ground Bounce Effect in BiCMOS

BiCMOS components have a different output structure than CMOS components and have significantly higher ground bounce than CMOS due to a much faster edge rate, lower output impedance, and the lack of a control on signals that overshoot. As a result the noise generated has different effects than CMOS components.

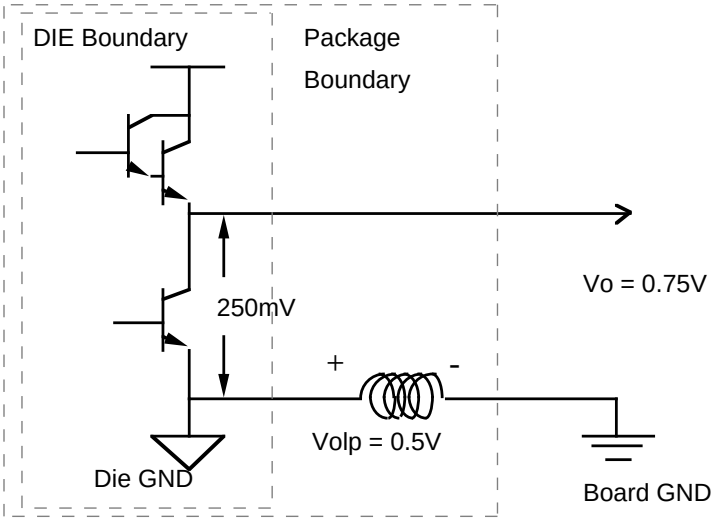

Figure 5, Output Structure of BiCMOS

Figure 5 shows the output structure for a BiCMOS component with a darlington pull up and a bipolar NPN pull down. The VI curve for the pull down is shown in Figure 6. Unlike the very linear characteristics of CMOS (Figure 3), the NPN pull down of BiCMOS will pull the output to a minimum of about 200 to 250 mV and then shut off. If the output transitions below this value, no current will flow into or out of the device output. Because of this, the lowest that a BiCMOS component can guarantee pulling a very light load is about 250mV. This causes a lack of noise immunity in high speed circuits.

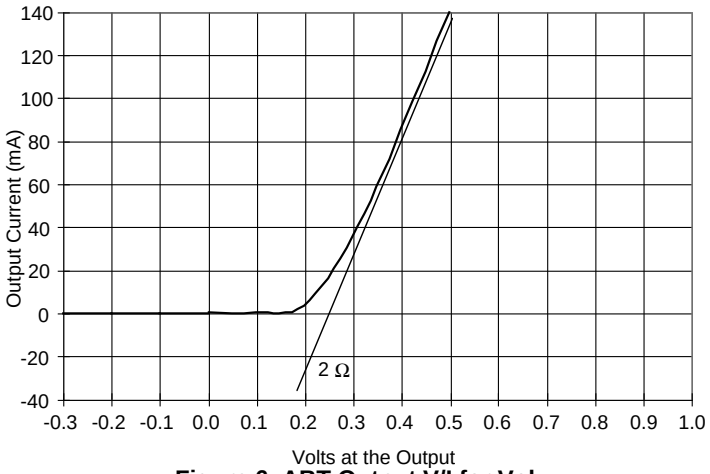

Figure 6, ABT Output V/I for Vol

Another characteristic of BiCMOS is the steepness of the VI curve once it passes the 200mV output level. In order for a component like ABT to guarantee 64mA current at 0.55V, the slope of the VI curve goes to about 2Ω above 300mV. This very low output impedance causes extremely fast edge rates and significant line termination problems.

As shown in Figure 7 a BiCMOS component has a strong negative undershoot caused by the inductive kick of the package. Unlike CMOS components there is no recovery from the negative undershoot and the output does not try to pull back to zero. The plot of Figure 7 is into a standard 50pF/ 500Ω load and it is the 500Ω to GND that causes the signal to return to ground.

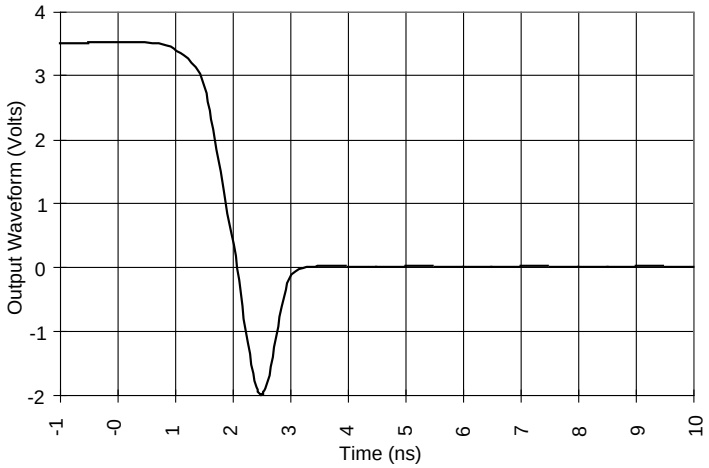

Figure 7, Undershoot in BiCMOS

Figure 8 shows how the same component as in Figure 7 would respond if the 500Ω load was significantly reduced (higher resistance value). When the output of a component such as ABT or LVT is tied to a device with a CMOS or BiCMOS input, the input clamp diode will draw the undershoot of the BiCMOS quickly back close to zero, giving a quick undershoot blip and then a steady state at -0.7V.

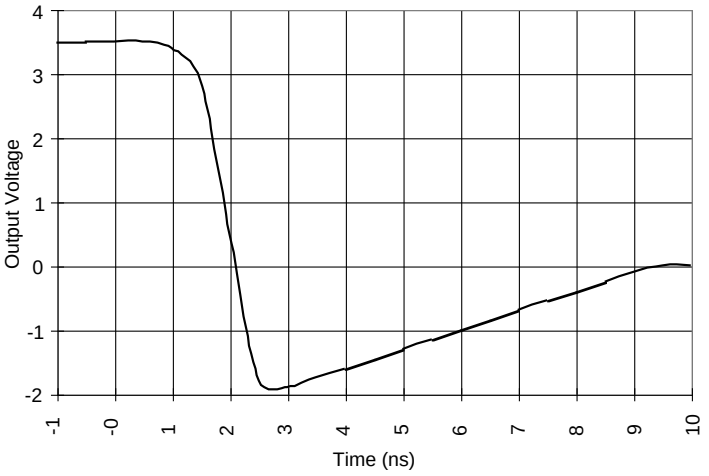

Figure 8, BiCMOS response, low resistive load

PROBLEMS CREATED BY BOUNCE

The problems created by ground bounce fall into two related categories, namely false switching and poor signal quality. Both of these problems are the result of the die ground moving relative to the external device ground.

False Switching

False switching may occur when the die ground or die Vcc reference voltage bounces enough to cause the input toggle point of the die to shift enough to pass through a guaranteed logic threshold.

For 5 volt components, the toggle point is about 1.5V and the guaranteed thresholds are 800mV and 2.0V for a logic LOW and HIGH. As shown in the following examples, it is fairly easy for violate a threshold with Ground Bounce. The Vcc level of 5V is not close to the toggle point of 1.5V and

proportional shifting of the toggle point relative to Vcc has a minimal effect on false switching. Therefore for 5V components, Ground Bounce has a distinct possibility of causing false switching where Vcc Bounce is much less of a problem.

For 3.3V components that can operate with voltages as low as 2.7V, Vcc is much closer and has more influence in output and input levels. In 3.3V components Vcc bounce can become a significant factor.

BiCMOS components such as ABT which have a high internal bounce due to a very fast output edge rate are very likely to false switch unless the input signals are maintained with HIGHs well above the threshold and LOWs near GND. Special caution must be taken with driving BiCMOS with BiCMOS because BiCMOS cannot maintain a solid LOW near zero and BiCMOS requires an input low which is near zero to avoid false switching.

Figure 9 demonstrates how a ground bounce level as low as 0.5V can cause device upset. If the input voltage is sitting at the minimum guaranteed high of 2.0V, and the input toggle point is at the nominal 1.5V point, and the die bounces 0.5V, the combined bounce and toggle point voltages equal the input voltage and could cause the device to toggle. Obviously, as the ground bounce increases, the input voltage will have to increase in equal amounts to avoid toggling due to ground bounce.

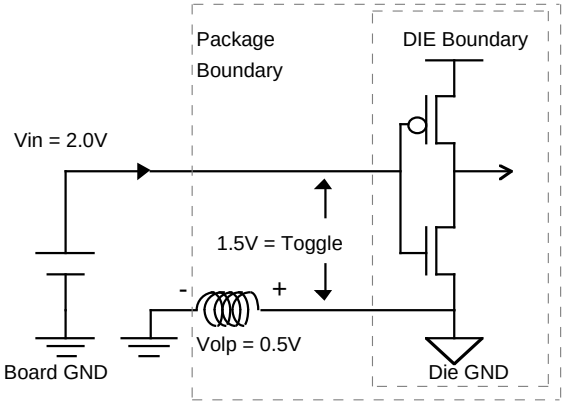

Figure 9, How 1/2 Volt GB can cause upset

Figure 10 demonstrates a similar problem, this time caused by Volv. As shown in the figure, if Volv is 0.7V and the toggle point is still 1.5V, the combination of the two can bring the input threshold below the guaranteed low point of 0.8V on the input. Increasing Volv lowers the point at which a logic low will cause false switching. Guaranteeing a lower input voltage provides more forgiveness to high Volv levels.

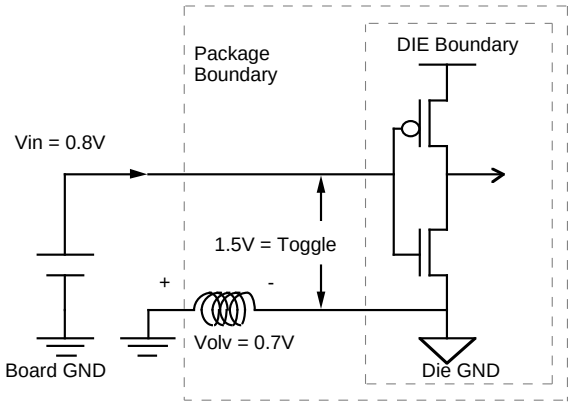

Figure 10, Volv = 0.7V can cause false switching

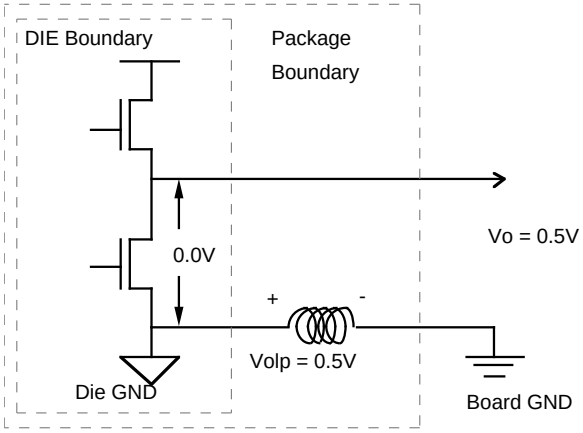

Figure 11, Output Problems with Volp on CMOS

Figure 11 shows how 0.5V Volp can cause the output to rise an equal amount. A situation like this may be significant if the output is attempting to hold a clock signal at a quiet steady state voltage. The problem is compounded with BiCMOS as shown in Figure 12 where the BiCMOS is not capable of holding the output at the Die GND level. In this case, the output voltage can easily rise above the guaranteed output LOW level of 0.55V. Increasing levels of Volp could easily take the output voltage above 800mV (logic LOW level).

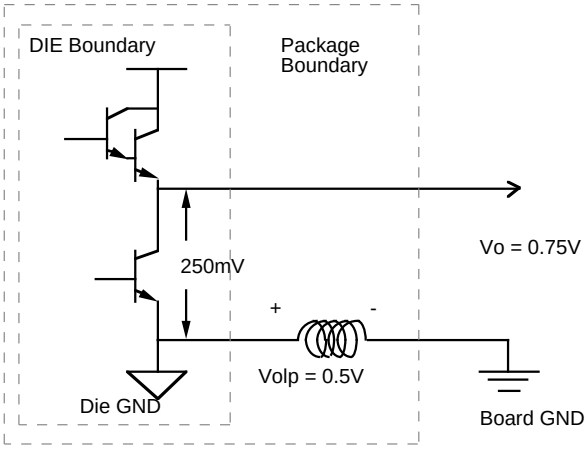

Figure 12, Output Problems with Volp on BiCMOS

Poor Signal Quality

The first effect that a designer will see from a component with high ground bounce is poor signal quality as shown in Figure 1. In CMOS components, the output is tied directly to the Die GND through the pull down FET. If the die is bouncing and ringing, this noise will extend directly to the device output and into the signal path. The effect of the Ground Bounce will be enhanced if the transmission line is inductive and the inductive kick extends the peaks and valleys of the noise..

In BiCMOS components, the bouncing die will have less influence on the output signal because the pull down will be in a high impedance state as the output approaches and goes below zero. The effect seen will be the BiCMOS component pulling the output very low (typically around -2.0V for ABT) and then going into a high impedance state, allowing the line to control the rebound if any. It is not uncommon to see ABT with severe Ground Bounce driving a bus with a clean waveform, except the Vol is running at a voltage below zero because ABT cannot rebound.

BOUNCE MEASUREMENTS

There is a traditional method for measuring both Ground Bounce and Vcc Bounce on a component without changing the test setup between the two tests. While this test is fairly accurate for measuring Ground Bounce on CMOS type components, the results are up to several hundred milivolts low for BiCMOS devices. The Vcc Bounce measurements are improperly taken and do not reflect Vcc Bounce, but rather another phenomena that will be discussed when discussing Vcc Bounce measurements.

Traditional Ground Bounce Measurements

The traditional method of measuring ground bounce is shown in Figure 13. All outputs are connected to a standard load of 50pF/500Ω. The plan is to force all outputs except one to toggle from a logic HIGH to a logic LOW simultaneously causing ground bounce to occur. The remaining one output is solidly held at a logic LOW. The philosophy is that the output help at a logic LOW has a low impedance path to the Die GND and therefore will accurately show the voltage swings of the Die GND relative to the ground level on the external pin.

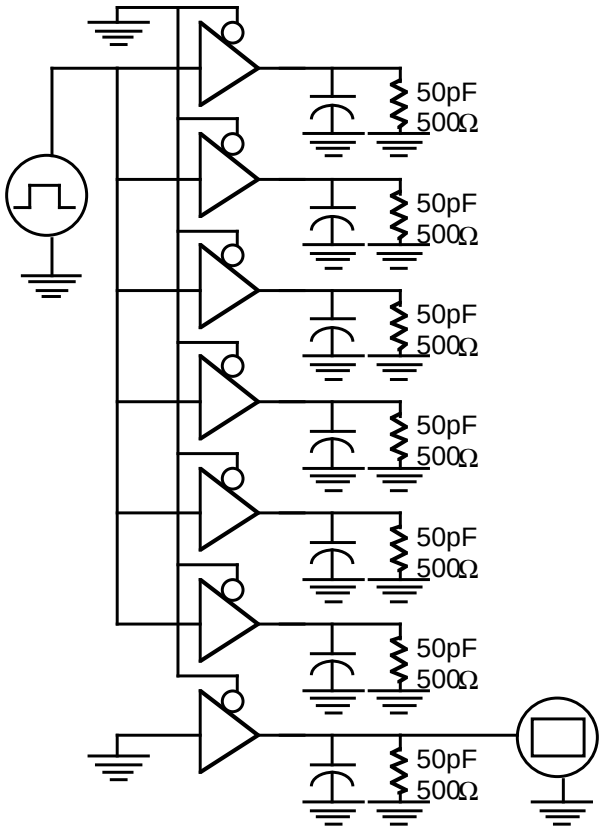

Figure 13, Standard Ground Bounce Measurement

Since there is little switching current in the “quiet” output, the lead inductance for that output should have very little voltage drop and not significantly affect the measurement. This becomes less true as the ground bounce level increases.

The lead inductance in each of the loaded outputs that are switching has only a small effect on the die voltage. The common ground pin must pass the combined currents from all of the switching outputs and therefore will exhibit the greatest voltage drop.

Improvements in the measuring technique for CMOS could be accomplished by using the standard set up, but removing the output load on the “quiet” output. This would reduce the damping factor of the load. When using a high impedance fast oscilloscope, these ground bounce measurements should be fairly accurate.

This measurement technique is fairly accurate for components with FET output drivers such as FCT and ACT.

BiCMOS components with bipolar NPN output drivers have a very high impedance when the output is held near zero. For BiCMOS the stabilizing effect of the load on the output will kill the accuracy of the test, even if the load is only the test fixture and scope probe. The BiCMOS high impedance output will not track the Die GND until the bounce has exceeded approximately 300mV.

Accurate Ground Bounce Measurements

While there is no proven technique for measuring ground

bounce in BiCMOS, there needs to be a common test that can be used for component comparison regardless of whether the component is CMOS or BiCMOS.

One possibility is a threshold toggle test. This could use the present test set up. With all outputs quiet, a single input would be slowly raised from zero through the threshold to determine the toggle point. Once the toggle point is determined, standard ground bounce testing takes place except the quiet input would be slowly raised to identify the point of switching again. Approaching the toggle point from both the HIGH and LOW and then multiplying the results by the scale factor of Figure 14 would give an approximation for Volv and Volp.

$$\text{Scale Factor} = \frac{5V}{3.5V} = 1.43$$

Figure 14, Scale Factor For Ground Bounce Threshold Test

This test would identify the false switching levels caused by ground bounce and may actually be of more interest to the designer than the traditional ground bounce numbers.

An additional possibility for testing BiCMOS would be to simply add the offset voltage of 200 or 300mV to the undershoot of one of the switching outputs from the traditional test to arrive at Volv. This cannot be added to the low going blip on the quiet pin because of the turn on time of the pull down transistor (CMOS is always “on”, bipolar shuts off). There is no way to use this method to identify Volp because the output is completely shut off during Volp and cannot be used to drive any signal.

Measuring Vcc Bounce

Vcc Bounce is the reverse of Ground Bounce and is the amount the die Vcc fluctuates relative to the external Vcc when all outputs switch from a logic LOW to a logic HIGH simultaneously. Vcc bounce is directly measurable only in CMOS rail swing components which have a fairly strong pull up structure. Vcc bounce cannot be directly measured in any TTL level CMOS or BiCMOS components.

The traditional Vcc Bounce measurement is done with the same test set up as Ground Bounce in Figure 13, Except the “quiet” output is held HIGH. The theory is that the quiet output will be held to die Vcc by the output structure in the component and any movement in Die Vcc will be reflected in this measurement. This is true only for rail swing CMOS components that have the P-Channel pull up. Any TTL level component will have a high impedance as the output approaches Vcc, killing the results of the test. CMOS rail swing components that have Power-off Disable or 5V tolerant 3V outputs will also have a high impedance state above Vcc, killing the Vcc test.

$$\text{Scale Factor} = \frac{5V}{1.5V} = 3.33$$

Figure 15, Scale Factor for Vcc Bounce Threshold Test

There is no accurate test for Vcc bounce used that exists as a standard in the industry today. The threshold test that was described for Ground Bounce could also be used to estimate Vcc bounce when used with a different scale factor as shown in Figure 15.

BOUNCE INFLUENCES

When designing with high speed logic, there are several items that have an influence on the bounce levels seen in high speed circuits. By considering these items during design, many of the bounce problems can be avoided.

Drive Level Effect on Ground Bounce

The ringing seen on the HIGH to LOW transition of a CMOS component is the ringing of the lead inductance caused by internal current surges caused by the switching of internal capacitances. The impedance of the pull down FET will dampen the switching action and lower the peak on the initial surge. The amount of damping is directly related to the impedance in the pull down stage and more damping lowers the Ground Bounce.

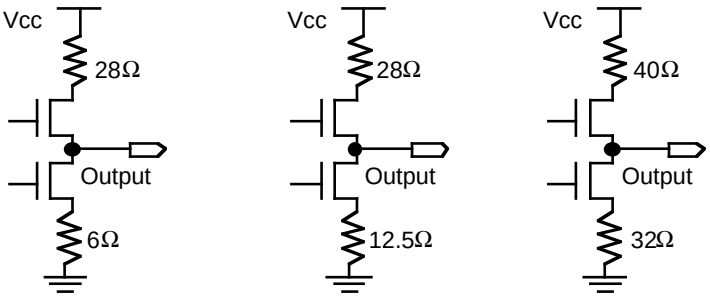

Figure 16, Double Density Output Structures

Figure 16 shows the output structures for IDT’s Double Density logic families. Each contains an impedance in the pull down structure of the device. In addition to the line driving and termination benefits of these resistors, they also help control ground bounce. Placing these in the source of the FET, any currents caused by the FET switching internal capacitances must be through these resistors.

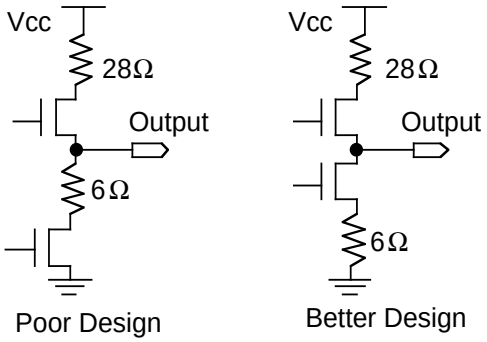

Figure 17, Lowering Device Ground Bounce

If the pull down FET is tied directly to the Die GND as shown in Figure 17, when the FET switches, the charge from internal capacitances is dumped more directly into the Die GND without passing through the resistor. This will increase the device ground bounce. Therefore of the components shown in Figure 16, the FCT16xxxT will have the highest ground bounce of the three and the FCT166xxxT will have the lowest. Approximate values of ground bounce for these devices are:

FCT166xxxT = 200mV
FCT162xxxT = 600mV
FCT16xxxT = 900mV

When looking at BiCMOS components as shown in Figure 18, the drive level is non linear, but is extremely strong once the 250mV threshold is exceeded for a LOW. This low impedance causes significant levels of bounce. For an ABT type component, the impedance is close to infinite until the 250mV threshold is crossed. Once the threshold is crossed, the impedance drops to about 2Ω.

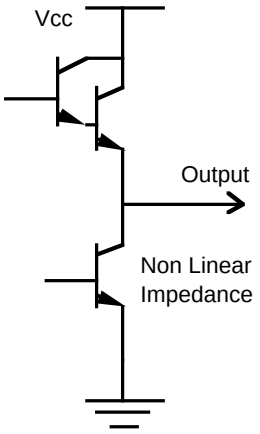

Figure 18, BiCMOS Output Structure

The darlington pull up has very high gain until the output voltage exceeds the Voh level. A rising edge will see a low impedance from the darlington and rise quickly until the pull up driver shuts off and goes into a high impedance mode. This sudden change in drive current will cause an overshoot and recovery on a LOW to HIGH transition. The N-Channel pull up of CMOS has a very linear impedance which is higher than BiCMOS and will arrive at the correct Voh with far less overshoot.

Fast Edge Rates

Ground Bounce is caused primarily by the lead inductance of the ground pin of the component package. The Ground Bounce is the voltage drop across this inductance. The voltage equation for an inductor is shown in Figure 19.

$$V = L\frac{di}{dt}$$

Figure 19, Equation for the Voltage across an inductor

Basically the equation states that the Ground Bounce voltage (voltage on the Die GND) is a direct result of the surge in current in the lead inductance between the die and external ground. To avoid the surge in current, the edge rate of the logic level change should be held to a minimum. From Ohms law we see V=RI. Modifying the equation for dynamic conditions and grossly simplifying the situation we arrive at:

$\Delta V = R\Delta I$

From this we can see that the edge rate ΔV is proportional to the change in current ΔI. Using TTL level components as an example, the change in voltage is set at about 3.2V (simplified). The surge in current ΔI is controlled by the attenuation of R (simplified). Since R is the output impedance of the component, the ground bounce is directly proportional to the output impedance (simplified). Therefore a component with 2Ω output impedance will have a significantly higher ground bounce level than one with a 32Ω output impedance (solid fact).

Crossover Current

In order for high speed logic to achieve the fastest possible speeds, it is necessary for the internal stages of the component to respond as fast as possible to a transition. To accomplish this, high speed components are designed to respond early and quickly to changes on the input. This results in a brief internal contention as the component is attempting to pull itself both up and down at the same time. As both pull up and pull down stages are active, a leakage from Vcc to GND through the component will result as shown in Figure 20. ΔIcc is a measure of the input crossover current and Iccd is a measure of the total crossover current during switching. Both parameters are specified in the Logic Data book. IDT FCT logic has the lowest crossover currents in the industry.

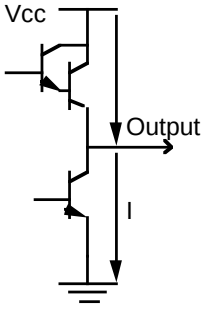

Figure 20, The Path of Crossover Currents

Crossover currents will add slightly to the Ground Bounce and Vcc Bounce of a component. There is no effective test to identify the bounce caused by crossover currents for a HIGH to LOW transition, but for the LOW to HIGH, the standard Ground Bounce test for CMOS is effective for CMOS. During the HIGH to LOW transition of the test, the “quiet” output will exhibit Ground Bounce while the LOW to HIGH transition will exhibit bounce due to crossover currents. As a logic transition occurs, the crossover current will begin to short the Vcc and GND on the die. This will be seen as a bounce on the Die GND during the transition.

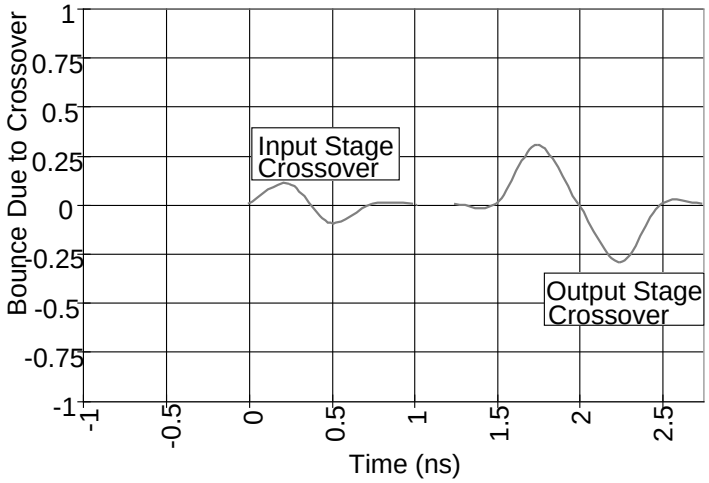

Figure 21, Crossover Bounce

Low crossover currents will help reduce noise from bounce. Most manufactures are fairly loose with their specifications for Iccd and ΔIcc to prevent failing during final test due to these parameters. As a result the best place for a designer to find actual values is in application notes such as IDT's Application Note 146 for Double Density.

Package Effect on Ground Bounce

When scientists and engineers designed the packaging concept for standard eight bit components, they chose the worst case arrangement for the power and ground pins when they selected the corner pins. Fortunately, by the time 16 bit Double Density components were developed, the designers were keenly aware of the ground bounce problems.

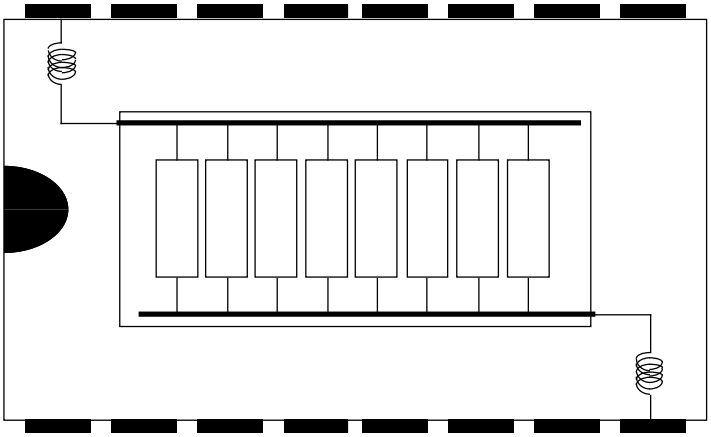

Figure 22, Typical Octal Package Arrangement

Traditional DIP logic packages contain several distinct pieces. The external package holds the pins and makes contact with the outside world. An internal leadframe brings the contact from the external pin to a point very near the die. A bond wire is then attached from the leadframe to the die, completing the contact from the outside pin to the silicon.

Unfortunately, each of the package contact components has a small amount of inductance (especially the bond wire) which accumulates to create an inductance for the package. Each package type has its own lead inductance and each pin has a lead inductance depending upon where it is located on the die. These values can be found in the SPICE models for each component and fall in a range around 3nh.

While this inductance has an influence on all pins, the pin of greatest concern is the GND because all internal circuits switch their currents through the GND pin, possibly simultaneously. These combined currents cause the ground bounce effect.

The optimum packages for low ground bounce are the smallest SSOP and QSOP while large packages such as side braze and large DIPs will be noisier. Components with multiple grounds and Vcc pins such as Double Density (16 bit logic) will give significantly better low noise performance because of the multiple current paths reducing the inductance of the package. In the equation in Figure 19, if the inductance of the package lead (L) is reduced the voltage drop across the inductance will be reduce, meaning Ground Bounce is reduced.

Octal Packaging

Figure 22 shows a greatly simplified package diagram for an octal component with a huge overgrown die. The combined effect of the pin, leadframe and bond wire are shown as an inductor for the Vcc and GND pins. In DIP type components, the die is a small piece of silicon in the center of the package. The power and ground must be brought from the corner of the package into the die near the center. This long path increases the inductance on the corner pins and amplifies the ground bounce of the component. Smaller packages such as QSOP avoid such long distances and reduce the lead inductance.

Double Density Packaging

Double Density components have multiple GND and Vcc pins distributed evenly on both sides of the package. With the close proximity to the center of the die, these multiple paths significantly reduce the combined lead inductances of the GND and Vcc paths. It is the device outputs that switch and cause current surges. Because of this, the output pins are positioned near the ground and Vcc pins on Double Density. The corner pins in the package are reserved for control signals which act as inputs only. Components such as the FCT162344T which has 32 outputs take special care to utilize all sides of the package and avoid piling up the outputs in one area.

Load Effect on Ground Bounce

The load capacitance on a component must be discharged through the output structure of the die to complete a logic transition. This current must be passed through the lead inductance of the die and will cause additional ground bounce as the load increases. There is an upper limit on the saturation current of the output driver which will put a top limit the effect that load will have on Ground Bounce.

DESIGN CONSIDERATIONS

There are rules which should be followed to avoid problems with ground bounce in high speed circuit designs. By following these rules, most false switching and line noise problems can be cured or significantly reduced.

Choose the Right Driver

Choose components with the highest output impedance that will drive the circuit. High drive components such as FCT16xxxT should not be used in applications where FCT166xxxT components are optimum. The noise and ground bounce add nothing to the design.

BiCMOS components such as ABT16xxx have a lower output impedance than FCT16xxxT and should be reserved for applications where undershoot is not a concern. An example of an application where ABT is not appropriate is driving memory arrays. Memory upset and data loss can be caused by undershoot. These would be transient errors that occur only when the driving component is making an address boundary change and undergoing Ground Bounce. An example would be an address change from 0FFFFH to 10000H for a Widebus, or 0FFFFH to 0FF00H for an octal component. In addition, some memories and some high speed processors may be damaged by excessive undershoot.

Double Density components such as FCT16xxxT have better packaging and lower ground bounce than components like FCTxxxT. The multiple ground and Vcc pins of Double Density reduce the ground lead inductance on the die and reduce ground bounce.

Avoid Pull Up Resistors on BiCMOS

BiCMOS components cannot hold a logic LOW near zero volts. It takes 200 to 250mV for BiCMOS to begin sinking current in a logic LOW state. Adding a pull up resistor will draw this level up beyond the 250mV level as shown in Figure 23. This reduces the input noise immunity on the input of the next component and may allow false switching if the next component should undergo ground bounce. If BiCMOS components are used, only pull down resistors should be used.

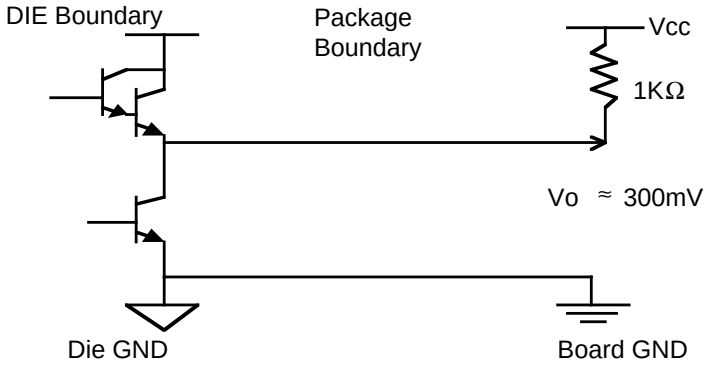

Figure 23, BiCMOS with Pull Up Resistors

CMOS components will pull a logic LOW to zero volts and do not suffer from the same problem as BiCMOS. Therefore CMOS is compatible with either pull up or pull down resistors.

OE with Clock HIGH

This scenario combines the worst of all situations and can easily cause false clock triggering unless the designer takes precautions. The setup is as follows:

1. A clocked register (e.g. '374) has its outputs tied to an inactive bus.
2. The bus is pulled up to Vcc through pull up resistors(not pull down).
3. The internal state of the register is all LOW.
4. Clock input is stable HIGH at a marginal level (e.g. 2.4V)
5. The output enable OE is disabled.

Disaster may happen when OE is suddenly enabled. At this point all of the outputs switch from the Vcc rail to a logic LOW simultaneously causing ground bounce. The situation depicted in Figure 9 occurs relative to the CLK input pin and the clock will transition from a HIGH to LOW to HIGH, causing the register to toggle.

Things that can be done to reduce the likelihood of register upset include

1. Never do an OE with the clock input HIGH.
2. If the CLK must be HIGH during OE, pull it very HIGH.
3. Avoid pulling the bus to Vcc with resistors.

Slow Clock Edges

Clock inputs should have fast edge rates on all high speed circuits which have ground bounce. Double clocking will probably occur if the input clock is allowed to slowly rise through the input threshold as shown in Figure 24. Since the input threshold is a direct ratio between Die Vcc and Die GND, as the Die GND level fluctuates, the input threshold will also fluctuate.

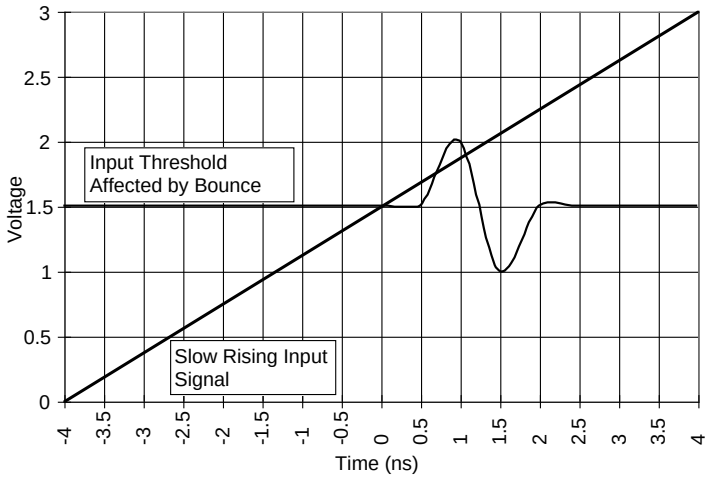

Figure 24, Fluctuations in Input Threshold

This problem can be avoided by insuring fast rising edges on all clocks. If clock lines need to be terminated, they should be terminated with an AC termination or some other end of the line termination rather than series termination.

Bus Inverting Components

Bus inverting components have the same problem as the slow clock of Figure 24. If all bus inputs rise simultaneously, it is highly likely that the subsequent switching of the output from all HIGH to all LOW will raise the input threshold sufficiently to cause the input to retoggle the threshold. This may cause a slight oscillation on the device output until the input level is well past the toggle point.

Use Bus-hold

Pull up and pull down resistors pull the bus one direction only. For a logic LOW state, a pull up resistor will draw current from the LOW state, raising the Vol level reducing the noise immunity of the logic LOW, For a logic HIGH state, a pull down resistor will reduce the Voh of the logic HIGH.

In addition, a pull up resistor will pull the bus to Vcc when the bus is HIGH. The subsequent transition to LOW then has a 5V transition instead of the normal 3.2V from Voh and will cause higher than normal Ground Bounce.

Bus-hold will pull LOWs to 0V (CMOS) and HIGHs to Voh (≈3.2V for TTL). This avoids the erosion of noise immunity by trying to pull the opposite state through the middle voltages.

Bus-hold retains the last state on the bus. Holding the last state significantly reduces simultaneous switching on the bus. As an example, an address bus that is pulled HIGH with pull up resistors, but operating in addresses near zero would toggle all outputs each cycle. The driver would output almost all zeros, then release the bus which would float HIGH. The

next address would pull it to LOWs again, causing switching noise. This would continue each cycle until the bus addresses were no longer near zero.

Bus-hold would retain the last random state on the bus and not attempt to pull the bus to a uniform direction. If the next data driven onto the bus was similar to the last data, there would be almost no switching and hence almost no switching noise.

Avoid Ground Bounce in Memory Arrays

Memory arrays are some of the most sensitive devices in common usage. With a high speed memory array, undershoot on input signals is very likely to cause data loss at random times when crossing address boundaries. If the undershoot is excessive, some memory components may be permanently damaged by undershoot.

When driving memories, use drivers with low undershoot and low ground bounce. Examples of these would be a BD-Lite FCT166244T for loads of less than 100pF. For larger loads, an FCT162244T would maintain the required speed with very low ground bounce. The Balanced Drive FCT162244T is very effective over a load range from 50pF to 250pF. Components like FCT16244T and ABT16244 should be avoided unless the load exceeds 250pF. An effective address driver for fannout is the FCT162344T.

Ground bounce is not the only cause of overshoot and undershoot, especially when driving a capacitive load with an inductive line. When undershoot is seen in these applications, another area of investigation should be proper line termination and matching the driver to the load. The Balanced Drive and BD-Lite components are very effective in reducing transmission line problems.

CONCLUSION

Ground Bounce and Vcc Bounce are very real phenomena but the testing techniques used to measure bounce are not accurate. If a component has a BiCMOS output structure, the measuring technique of observing a stable output will give a reading that has no correlation to actual bounce levels.

Ground bounce is caused primarily by the inductance in the component package lead of the ground and Vcc pins during switching. Faster edge rates and lower output impedances will create higher levels of ground bounce. Advanced BiCMOS components have the fastest edge rates and lowest output impedances in the industry. This creates high levels of ground bounce in these components.

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