DESIGNING WITH BUS HOLD

APPLICATION NOTE AN-143

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INTRODUCTION

Bus-hold retains the last active state on a bus when the bus is disabled or has no active driver. Bus-hold is a function of bus inputs only and is not present on control inputs or bus outputs (except designated I/O ports). Bus-hold components are pin and function compatible with standard Double-Density components, and can be identified by the H in the part number (e.g. FCT162H244T).

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ADVANTAGES OF BUS-HOLD

Bus-hold provides several advantages over competing design methodologies.

1. Prevents 'floating busses'.
2. Reduces part count (eliminates pull up resistors).
3. Reduces bus loading.
4. Doesn't toggle the bus when the bus is released.
5. Reduces power dissipation.
6. Improves device output hold time.

Bus-hold prevents a floating bus. Good design practice dictates that any bus that can transition to a high impedance state should be pulled up[1] to prevent the oscillations that may develop from noise pickup. Additionally a floating bus may increase power dissipation as inputs drift near the toggle region, causing internal device leakage.

The primary competing design practice is the use of pull up resistors on the device inputs. With bus-hold, the pull up resistors can be eliminated, significantly reducing the part count and assembly costs.

Adding a pull up resistor adds bus loading every time the bus toggles low. With bus-hold, once the transition has been made through the toggle point, the bus-hold input will be assisting the driver rather than fighting and causing a current drain.

When using pull up resistors, the bus will be pulled high when released, causing unnecessary transitions. Bus-hold components will always retain the last known state, avoiding transitions.

In very power sensitive applications, the current leakage of the pull up resistor (when the bus is low) can be avoided with a bus-hold input. Also, since the input will avoid unnecessary transitions through the input threshold, the device power dissipation will be reduced (ΔIcc).

In applications where it is desirable to maintain a longer hold time when a bus goes 3-state (usually memory applications), bus-hold may provide the needed, added margin required.

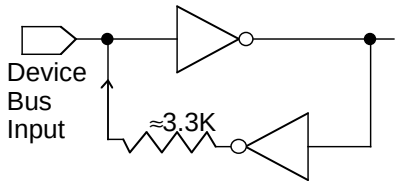

Figure 1, Bus-hold Block Diagram

HOW BUS-HOLD WORKS

Bus-hold is a small positive feedback current on device inputs. When an input changes logic state, the bus-hold circuit will return a small current back to the device input, effectively adding to the transition of the input. This positive feedback will then hold the final logic level until an active driver toggles the input voltage to the opposite logic state, where bus-hold will then again hold the logic state. A block diagram of a bus-hold input is shown in Figure 1 and the schematic representation is shown in Figure 2.

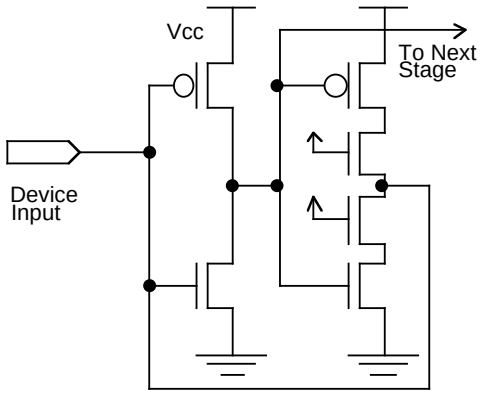

Figure 2, Bus-hold Schematic Representation

BUS-HOLD SPECIFICATIONS

Bus-hold specifications identify the strength of the sustain (hold) current at the TTL logic threshold levels of 2.0V and 0.8V and the overdrive current at the input toggle point (typically 1.5V). Input current levels on a bus-hold circuit should approach zero when the input voltage approaches zero or Vcc as shown in Figure 3. The specified maximum limit on overdrive current has not yet been established.

Symbol	Parameter	min.	max.	unit
I_{BHL}	Bus-hold LOW Sustaining Current(1)	50	—	µA
I_{BHH}	Bus-hold HIGH Sustaining Current(2)	-50	—	µA
I_{BHLO}	Bus-hold LOW Overdrive Current(3)		tbd	µA
I_{BHHO}	Bus-hold HIGH Overdrive Current(4)	—	tbd	µA

NOTES:
1. The minimum current the bus-hold circuit is guaranteed to sink if a logic LOW input is raised to 0.8V.
2. The minimum current the bus-hold circuit is guaranteed to source if a logic HIGH input is lowered to 2.0V.
3. The maximum current required from an external driver to switch a bus-hold input from a logic LOW to a logic HIGH.
4. The maximum current required from an external driver to switch a bus-hold input from a logic HIGH to a logic LOW

BUS-HOLD CURRENT LEVELS

Figure 3 shows the typical input current level as the input voltage transitions from zero to 5V (Vcc). It should be observed that the current levels are the highest near the input toggle point of 1.5V as the bus-hold circuit attempts to pull the voltage away from the threshold region. As the input voltage reaches the steady state logic levels of 0.0V for a LOW or 3.5V for a HIGH, the current levels approach zero.

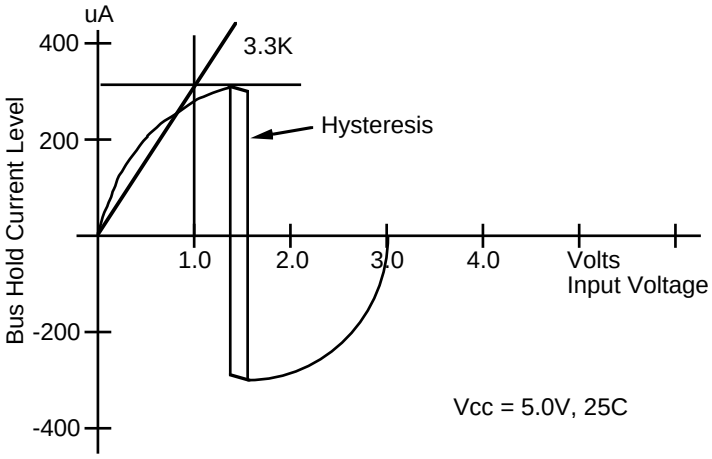

Figure 3, VI Characteristics for Bus-hold

HOLD CHARACTERISTICS

Examining Figure 3, it can be seen that the slope of the VI curve is approximately 3.3Ω for voltages of less than 1.5 volts (logic low). Therefore, for a logic LOW condition, bus-hold is typically equivalent to a 3.3Ω resistor to ground. For voltages of greater than 1.5 volts (logic HIGH), the curve resembles an impedance from Voh (rather than Vcc as in the case of a resistor). For a rough comparison, this may be compared to a 3.3Ω resistor to 3.5V (typical).

OVERDRIVE CHARACTERISTICS

The current necessary to overcome the bus-hold current during an input transition can reach 500µA near the input toggle voltage of 1.5V. At 1.5V, most bus drivers are capable of driving a large current, meaning that bus-hold does not affect the bus loading significantly. For example if a Double-Density Balanced-Drive component were driving a bus-hold component, the Balanced-Drive output drives 115mA I_{ODL}/I_{ODH} typically at 1.5V. Comparing this to the bus-hold overdrive current of less than 500µA, it can be seen that the bus-hold input (or several bus-hold inputs tied together) would not have a significant loading effect on the driver. It is easier to overdrive a bus-hold input than to drive a pull up resistor of equivalent value to a logic LOW.

HYSTERESIS

All of IDT's logic components have input hysteresis including bus-hold components as shown in Figure 3. The addition of bus-hold to an input amplifies the effect of input hysteresis by driving the bus-hold current back into the source impedance of the driving circuit. The amplitude of this effect is dependent upon the source impedance of the driver.

DESIGNING WITH BUS-HOLD

Bus-hold can be used in most applications in place of a pull-up resistor. When bus-hold is used, there is no need to tie unused device inputs high or low, but doing so has no adverse effects. One bus-hold component on a bus is all that is required to hold the bus, but as many bus-hold inputs as desired can be tied to the same bus. If large quantities (100s) of bus-hold inputs are tied together, the designer must insure that the bus driver has sufficient drive capability to drive the components beyond the 1.5V threshold.

CONCLUSION

Components with bus-hold offer several advantages over the use of external pull up or pull down resistors. With the cost of bus-hold components at parity with standard components, most applications can benefit from the use of bus-hold components.

NOTES

1. References to "pull-up" also imply "pull down" with the necessarty adjustments throughout the document.

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