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SH7211 Group

12-Bit A/D Converter: Example of Settings for A/D Conversion on a Single Channel

Introduction

This application note describes an example of settings for A/D conversion on a single channel as an example of application of the 12-bit A/D converter of the SH7211.

Target Device

SH7211

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1. Preface

1.1 Specifications

- A/D conversion in single-cycle scan mode on a single channel by the 12-bit A/D converter
- Three rounds of A/D conversion are performed on analog input channel 0 (AN0), and the converted data are stored in RAM.

1.2 Module Used

- 12-bit A/D converter (12-bit A/D)

1.3 Applicable Conditions

• MCU	SH7211 (R5F7211)
• Clock operating mode	6
• Operating frequency	Internal clock: 160 MHz Bus clock: 40 MHz Peripheral clock: 40 MHz
• C compiler	SuperH RISC Engine Family C/C++ Compiler Package Ver.9.0.3.0 from Renesas Technology
• Compiler options	Default settings by the High-performance Embedded Workshop -cpu = sh2a -debug -gbr = auto -global_volatile = 0 -opt_range = all -inifinte_loop = 0 -del_vacant_loop = 0 -struct_alloc = 1

1.4 Related Application Note

None

2. Description of the Sample Application

The sample program employs the 12-bit A/D converter to perform three rounds of A/D conversion on a single channel, and then stores the converted data in RAM.

2.1 Operational Overview of Module Used

The 12-bit A/D converter has two operating modes: single-cycle scan mode and continuous scan mode. To perform A/D conversion on a single channel, a single channel is selected in single-cycle scan mode.

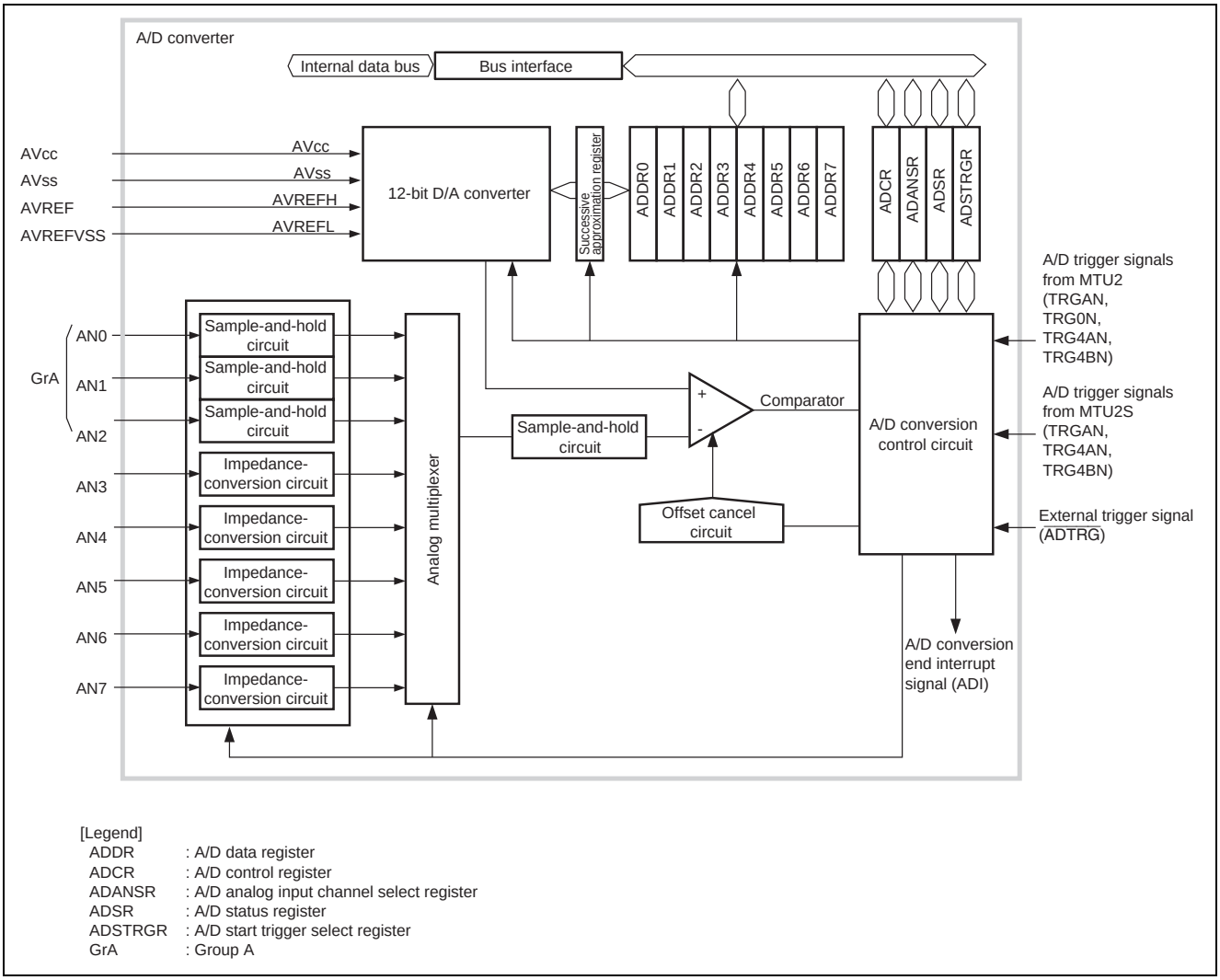
There are three methods for starting A/D conversion.

1. Software: Setting of the ADST bit
2. Timers: TRGAN, TRG0N, TRG4AN and TRG4BN signals from the MTU2 module, and TRGAN, TRG4AN and TRG4BN signals from the MTU2S module
3. External trigger: Falling edge of $\overline{\text{ADTRG}}$

Additionally, channels 0, 1, and 2 have dedicated sample-and-hold circuits, so multiple channels are capable of simultaneous sampling. Table 1 gives an overview of the 12-bit A/D converter and figure 1 is a block diagram of 12-bit A/D converter. For details on the 12-bit A/D converter, see the section on the A/D converter in the *SH7211 Group Hardware Manual*.

Table 1 Overview of 12-Bit A/D Converter

Item	Description
Resolution	12 bits
Minimum conversion time	1.25 μs per channel
Number of modules	1
Input channels	8
Operating modes	Single-cycle scan mode Continuous scan mode
Sample-and-hold function	Common to all channels: 1 circuit Dedicated for individual channels, 1 circuit each for ch0, ch1, and ch2 (3 in all)
Sources for activation of A/D conversion	Software: Setting of the ADST bit Timers: TRGAN, TRG0N, TRG4AN, and TRG4BN signals from the MTU2 module TRGAN, TRG4AN, and TRG4BN signals from the MTU2S module External trigger: $\overline{\text{ADTRG}}$



[Legend]
ADDR : A/D data register
ADCR : A/D control register
ADANSR : A/D analog input channel select register
ADSR : A/D status register
ADSTRGR : A/D start trigger select register
GrA : Group A

Figure 1 Block Diagram of the 12-Bit A/D Converter

2.2 Procedure for Setting Module Used

Figure 2 shows an example of the initialization sequence for A/D conversion on a single channel. For details on the settings of individual registers, see the *SH7211 Group Hardware Manual*.

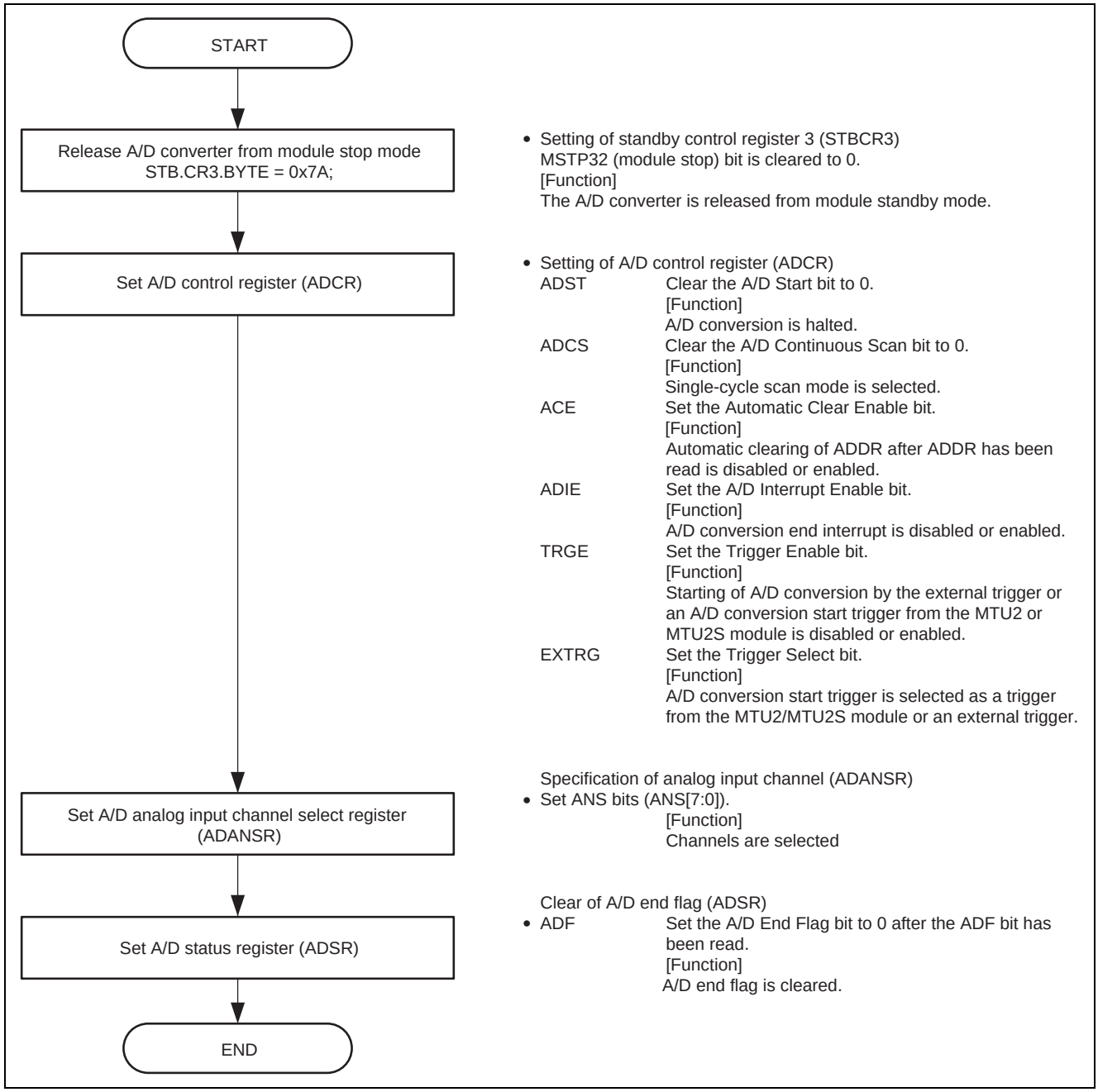


Figure 2 Initialization Sequence for 12-Bit A/D Conversion

2.3 Operation of the Sample Program

In this sample program, A/D conversion is performed on channel 0. The A/D converter is activated by software and converted data are stored in RAM. This processing is repeated three times.

Table 2 gives a description of RAM usage in this sample program.

Table 2 RAM Used in the Sample Program

Label Name	Description	Area	Name of Employing Module
AD_data[0-2]	Array for storing A/D-converted data (2 bytes/datum)	On-chip RAM	io_ad_conv (void)

2.4 Sequence of Processing by the Sample Program

Table 3 gives settings for registers used in the sample program and figure 3 shows the flow of handling the sample program.

Table 3 Settings for Registers Used in Sample Program

Register Name	Address	Setting	Description
A/D control register (ADCR)	H'FFFFE800	H'00	• ADCS = 0: Single-cycle scan • ACE = 0: Disables automatic clearing of ADD after having read ADDR • ADIE = 0: Disables A/D conversion end interrupt • TRGE = 0: Disables starting of A/D conversion by an external trigger or by the MTU2 and MTU2S modules
A/D analog input channel select register (ADANSR)	H'FFFFE820	H'01	• Selects AN0

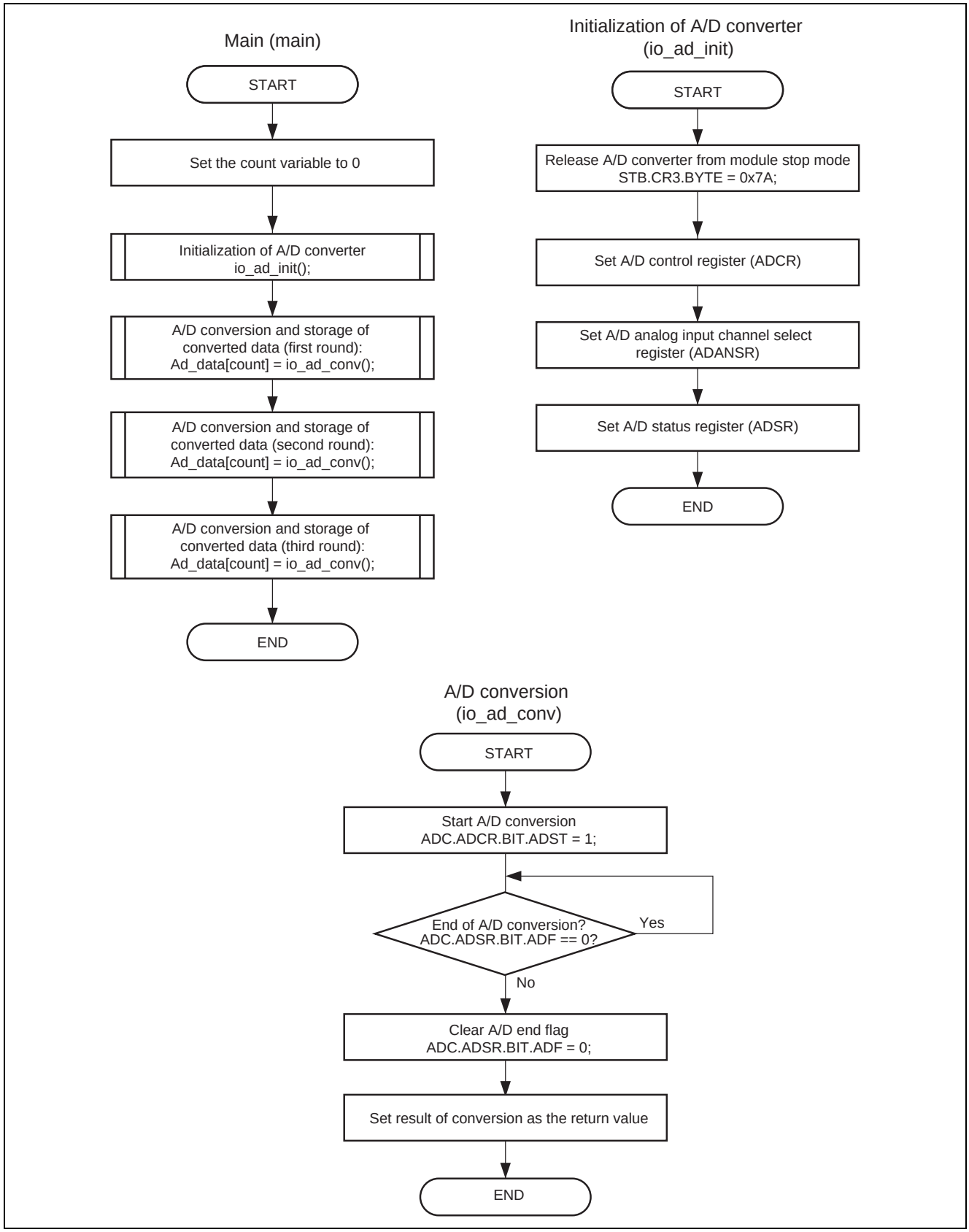


Figure 3 Flow of Handing the Sample Program

3. Listing of Sample Program

1. Sample Program Listing: "main.c" (1)

```
1   /*""FILE COMMENT""*******************************************************************************
2   *
3   *       System Name    : SH7211 Sample Program
4   *       File Name      : main.c
5   *       Contents       : Sample program for A/D conversion on a single channel
6   *       Version        : 1.00.00
7   *       Model          : M3A-HS11
8   *       CPU            : SH7211
9   *       Compiler       : SHC9.0.3.0
10  *       note           : The A/D converter employs a single channel for A/D conversion in
11                           single-cycle scan mode. Three rounds of A/D conversion on
12                           analog input channel 0 (AN0) proceed, and the converted data are
13                           stored in RAM.
14  *
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22  *
23  *       history        : 2007.08.31 ver.1.00.00
24  *""FILE COMMENT END""*************************************************************************/
25  #include <machine.h>
26  #include "iodefine.h"     /* SH7211 iodefine  */
27
28
29  /* ==== prototype declaration ==== */
30  void main(void);
31  void io_ad_init(void);
32  unsigned short io_ad_conv(void);
33
34  /* ==== symbol definition ==== */
35  #define AD_COUNT 3
36
37  /* ==== RAM allocation variable declaration ==== */
38  unsigned short Ad_data[AD_COUNT];
39  unsigned char count;
40
```

2. Sample Program Listing: "main.c" (2)

```
41  /*""FUNC COMMENT""*****************************************************
42  * Outline      : main
43  *-------------------------------------------------------------------------
44  * Include      : #include "iodefine.h"
45  *              : #include <machine.h>
46  *-------------------------------------------------------------------------
47  * Declaration  : void main(void);
48  *-------------------------------------------------------------------------
49  * Function     : A/D conversion on a single channel
50  *-------------------------------------------------------------------------
51  * Argument     : non
52  *-------------------------------------------------------------------------
53  * Return Value : non
54  *-------------------------------------------------------------------------
55  * Notice       : non
56  *""FUNC COMMENT END""*************************************************/
57  void main(void)
58  {
59
60      count = 0;
61
62      /* ==== Initial setting of ADC  ==== */
63      io_ad_init();
64
65      /* ==== A/D conversion ==== */
66      Ad_data[count] = io_ad_conv();
67      count++;
68      Ad_data[count] = io_ad_conv();
69      count++;
70      Ad_data[count] = io_ad_conv();
71
72      while(1){
73          /* loop */
74      }
75
76  }
77
```

3. Sample Program Listing: "main.c" (3)

```
78  /*""FUNC COMMENT""*****************************************************************
79  * Outline      : Initial setting of ADC
80  *-------------------------------------------------------------------------------
81  * Include      : #include "iodefine.h"
82  *-------------------------------------------------------------------------------
83  * Declaration  : void ad_init(void);
84  *-------------------------------------------------------------------------------
85  * Function     : Initial setting of ADC
86  *-------------------------------------------------------------------------------
87  * Argument     : non
88  *-------------------------------------------------------------------------------
89  * Return Value : non
90  *-------------------------------------------------------------------------------
91  * Notice       : non
92  *""FUNC COMMENT END""*************************************************************/
93  void io_ad_init(void)
94  {
95      /* ==== Release of module standby(ADC) ==== */
96      STB.CR3.BYTE = 0x7A;
97
98      /* ==== Setting of ADC ==== */
99      /* ---- A/D Control Register(ADCR) ---- */
100     ADC.ADCR.BYTE = 0x00;
101         /* 7    = b'0      : A/D Start Flag                                */
102         /* 6    = b'0      : Single-cycle scan                             */
103         /* 5    = b'0      : Automatic clearing of ADDR by its readout
104                               is disabled                                   */
105         /* 4    = b'0      : Generation of A/D conversion end
106                               interrupt is disabled                         */
107         /* 3-2  = b'0      : reserve                                       */
108         /* 1    = b'0      : A/D conversion start by the external trigger
109                               or an A/D conversion start trigger from
110                               the MTU2 or MTU2S is disabled                  */
111         /* 0    = b'0      : A/D converter is started by the A/D conversion
112                               start trigger from the MTU2 or MTU2S          */
113
114     /* ---- A/D Analog Input Channel Select Register(ADANSR) ---- */
115     ADC.ADANSR.BYTE = 0x01;
116
117     /* ---- A/D Status Register(ADSR) ---- */
118     ADC.ADSR.BIT.ADF = 0;             /* ADF clear */
119 }
120
```

4. Sample Program Listing: "main.c" (4)

```
/*""FUNC COMMENT""*************************************************
* Outline      : A/D conversion
*-----------------------------------------------------------------------
* Include      : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration  : unsigned short ad_conv(void);
*-----------------------------------------------------------------------
* Function     : Clearing of A/D end flag (ADF), and storing of conversion data
*-----------------------------------------------------------------------
* Argument     : void
*-----------------------------------------------------------------------
* Return Value : ad_buf ; Buffer which stores A/D conversion data
*-----------------------------------------------------------------------
* Notice       :
*""FUNC COMMENT END""*********************************************/
unsigned short io_ad_conv(void)
{
    unsigned short ad_buf;

    ADC.ADCR.BIT.ADST = 1;        /* A/D conversion start */

    while(ADC.ADSR.BIT.ADF == 0){
    /* A/D conversion completion waiting */
    }

    ADC.ADSR.BIT.ADF = 0;         /* ADF clear */
    ad_buf = ADC.ADDR0;

    return(ad_buf);
}

/* End of File */

```

4. Documents for Reference

- Software Manual
  SH-2A/SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7211 Group Hardware Manual
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