AN-1187 High Efficiency Adjustable Buck Converter

In this application note, we'll use a GreenPAK™ IC to construct a buck converter with an adjustable output voltage. The output voltage range will be 2-5 V and the input range will be 5-10 V. The main advantage of this design is efficiency. The converter will be able to step down the input voltage at up to 97% efficiency, which is superior to both low-dropout regulators (LDOs) and ordinary DC-DC converters. The maximum supported output current will be 2 A.

Solution

The main challenge of this application is to generate the proper control pulse-width modulation (PWM) signals. Because efficiency is an important criterion for this application, a synchronous configuration is preferred, so the diode from the classic configuration will be replaced by another transistor. Consequently, two control signals are involved. The top level schematic is presented in Figure 1.

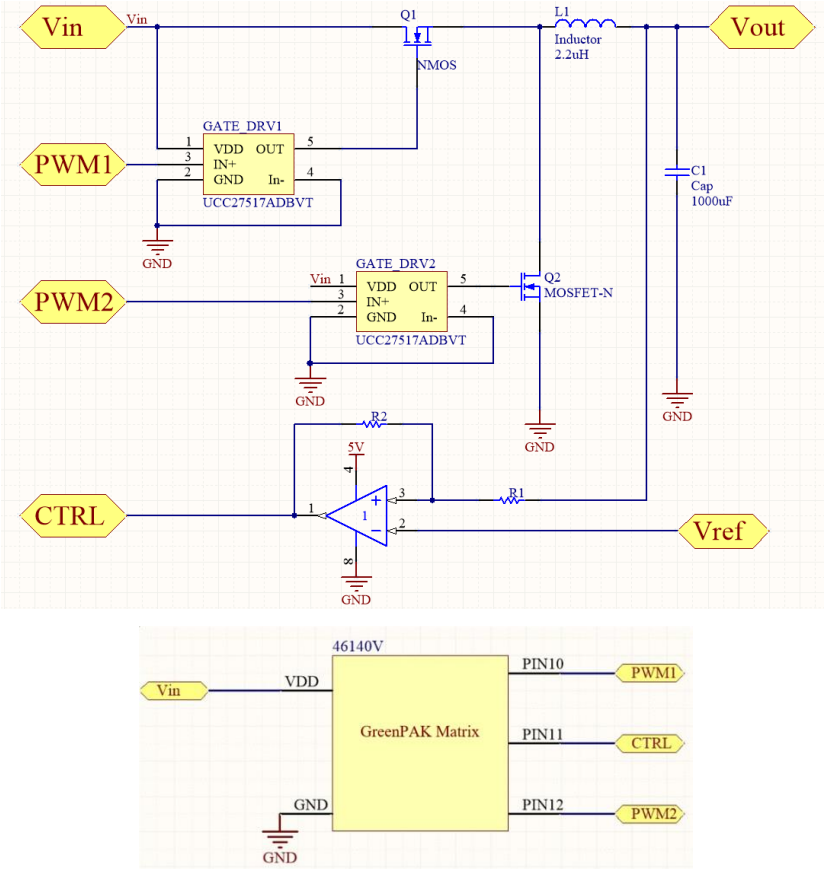

Figure 1. Top level schematic

PWM1, PWM2 and CTRL are outputs of the GreenPAK Matrix. PWM1 and PWM2 are responsible for transistor control. Because power transistors have a high gate capacitance, two gate drivers were introduced to avoid high transient currents being pulled from the GreenPAK circuit. In this way, its outputs are protected. However, the gate drivers also have a level shifter function. Because the source of Q1 is not grounded like the source of Q2, it can reach a very high potential. For this reason, higher amplitude pulses should be generated for controlling this transistor. The amplitude of the gate driver output is equal to the input voltage. The coil value was calculated according to the maximum desired output current, which is 2 A.

In order to maintain the fixed output voltage at any current consumption within range, a feedback mechanism was introduced. This is based on an ordinary comparator (bandwidth > 5 MHz).

The GreenPAK VDD power can be supplied directly from the input, provided it does not exceed 5.5 V. If it does, an intermediary LDO is required. This won't affect the global efficiency, because the current consumed by the GreenPAK is low. Alternatively, a resistor and a Zener diode would be sufficient to decrease the input voltage to 5.1 V and supply the GreenPAK IC.

The Control Algorithm

The output voltage of the converter depends on how much time transistor Q1 stays on for (its duty cycle). The approximative value of the output voltage is:

$$V_{out} = \tau \cdot V_{in}$$

Where τ is the duty cycle of the control signal that commands Q1. In this case, the on-off control technique was used. This means that the GreenPAK can generate two types of PWM, one with a 20% duty cycle and another with 70%. If the input voltage is equal to 10 V, the output will be able to equal 2 V or 7 V. The feedback mechanism tells the GreenPAK controller how to properly generate these signals, as summarized below:

$$\begin{cases} V_{out} > V_{ref} + 0.1V, & PWM_{duty} = 20\% \\ V_{out} < V_{ref} - 0.1V, & PWM_{duty} = 70\% \end{cases}$$

So, if the output goes below a threshold, the controller generates a larger duty cycle PWM to increase it. The opposite applies for the other case. V_ref+0.1V and V_ref-0.1V are the thresholds for this hysteresis mechanism, and are set by adjusting the comparator's positive feedback resistances. In this case, we're talking about a 200 mV hysteresis, so the ratio will be:

$$\frac{R2}{R1} = 25$$

The comparator has a wide bandwidth, so it will switch these values very quickly. Because this process is so fast and a capacitor was connected to the output, the output value will be established in the interval (V_{ref} - 0.1V, V_{ref} + 0.1V). This is called hysteretic control. The ripple was considered to be 200 mV (its value should be similar to the hysteresis width).

The Q1 control signal controls the output voltage, but is not the only signal that counts; the control of Q2 is important, too. To achieve a maximum efficiency, it has to be somewhat complementary to that of Q1. This means that when PWM1 is HIGH, PWM2 has to be LOW, and when PWM1 is LOW, PWM2 has to be HIGH. Of course, the transition between these two signals shouldn't be sudden. If the transistors are both open at the same time (even for a very small time) then cross conduction will occur (which is actually a short circuit).

The GreenPAK Design

The control signals should look like those shown in Figure 2. The red one is PWM1, and the purple one is PWM2. The complementarity between them is clear. The transition between edges is delayed by a dead time to Figure 2 avoid cross conduction. The purpose of the GreenPAK design is to generate such signals, starting from a 50% duty cycle square wave. In the following example, this process will be described and applied in the GreenPAK Design.

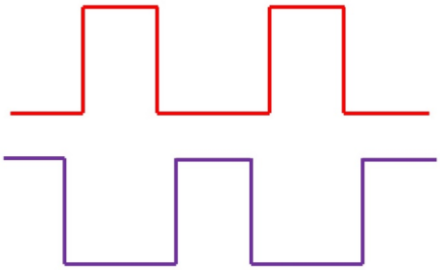

Figure 2. The control signals

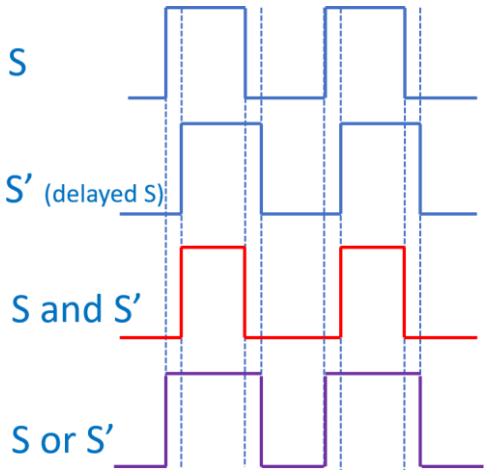

Figure 3. The logical operations

Obtaining the two required control signals from an ordinary clock signal is not hard. We'll denote the input signal S. First, S has to be delayed, obtaining the S' signal. Applying a logical AND operation between S and S', we obtain the control signal of Q1. Then, by doing the same with a logical OR, and passing S OR S' through an inverter, we obtain the control signal for Q2.

In the GreenPAK design, a square signal can be generated using a counter and a comparator. For this application, the counter clock was 27 MHz, and the overflow data was set to 60. The comparator threshold was set to 15 using the internal register.

$$f_{switching} = \frac{27Mhz}{60} \cong 450KHz$$

$$DutyCycle = \frac{15}{60} = 25\%$$

The square signal is passed through a GreenPAK delay block and then input to the AND and OR gates to obtain the desired waveforms. Because of this algorithm, the ON time of the PWM decreases with the delay value. As the chosen delay is 125 ns, the final duty cycle will be around 20%. In order to obtain the 70% duty cycle signal, the output of the comparator will be negated and then passed through logic gates. By negating the 25% PWM, a 75% PWM is obtained. Then, by decreasing the delay time, the final value of 70% is obtained. A multiplexer switches between two signals according to the output of the comparator.

Note: The measurements were done with a Tektronix MDO3034, for accuracy and repeatability.

How to Test the Circuit

The circuit is tested by applying a fixed voltage at the input (for instance, 10 V). The desired output voltage should be applied at the Vref pin (a Zener diode or a voltage divider can be used).

Pin 18	PWM1
Pin 20	PWM2
Pin 12	CTRL

Table 1. Pins and their corresponding outputs

The waveforms in Figure 4 are PWM1 (yellow) and PWM2 (blue). The left side depicts the 70% duty cycle, and the right side depicts the 20% duty cycle.

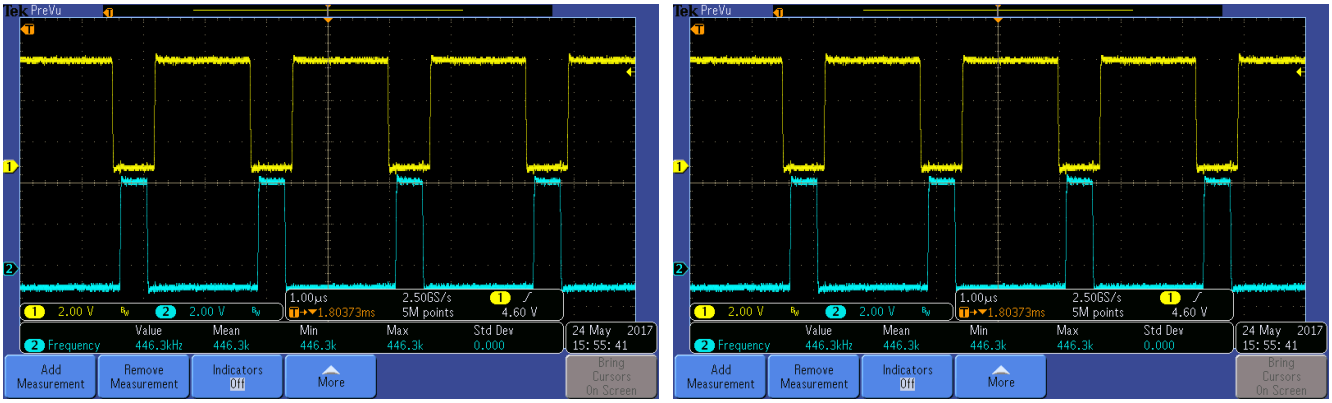

Figure 4. The output waveforms of the GreenPAK matrix

Figure 5 demonstrates the converter's functionality. The source was supplied at 10 V, and the reference voltage was set to 4 V using a resistive divider. As expected, the output voltage was 4 V.

The test circuit was realized on a test board.

Conclusion

This type of buck converter is a very efficient and a low cost solution for DC-DC conversion. There is no need for any particular types of transistors or comparators – even a general purpose operational amplifier would work (that's why no particular part numbers were mentioned in this application note). The only restrictions for transistors is to operate at 500 kHz and to sustain at least 2 A.

Figure 5. The prototype

Efficiency

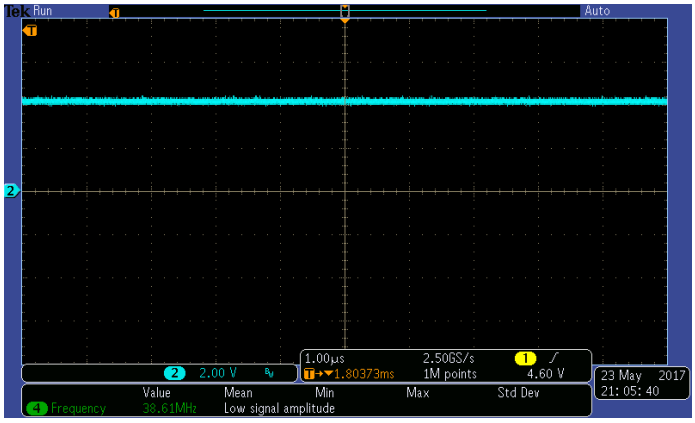

Figure 6. The output voltage

The efficiency (as a percent) of the converter was measured as the ratio between the output power and the input power. All measurements were done with an input voltage of 5 V. The input power was calculated as the product between the input voltage and the input current. The input current was determined using an ammeter in series with the input. In order to vary the output current, multiple resistors were put at the output. The output power was measured as:

$$P_{Load} = \frac{U_{out}^2}{R_{Load}}$$

The output voltage was set to 2.5 V, using a 20k-20k resistor divider supplied from the input. Important note: to achieve a high efficiency, it is very important to choose transistors with a low on resistance (< 0.08 Ω).

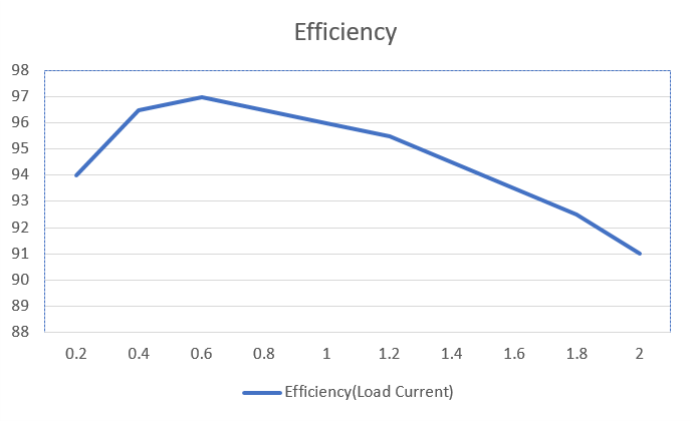

Figure 7. The efficiency curve

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.