Author: Roger Liang
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Introduction

Set/Reset latches (RS latches) are very useful memory devices in digital logic design. A traditional RS latch is level triggered and is useful when the set and reset inputs holds its value high or low. When the set and reset inputs are one-shot pulses and their rising edges are needed as triggers, RS latch becomes ineffective because of potential timing conflicts at the input. An edge-triggered latch can be used to avoid such conflicts. The following application note uses a SLG46721 GreenPAK to construct an edge-triggered latch; any GreenPAK with two resettable digital flip-flops (DFF) and an inverter can be used.

Design 1: Level Triggered Latch and its Limitation

Before analyzing edge-triggered latch, let's first take a look at a RS latch and application cases in which it can fail. Figure 1 shows one way to implement an active high RS latch by using a look-up-table (LUT) with feedback. Table 1 in the appendix shows the LUT's properties. The power-on-reset (POR) input makes sure the latch will start with a low output. A high on SET sets the output to high. A high on RESET resets the output to low. A low on both SET and RESET latches the output to its previous state. In figure 1's example, RESET takes higher priority over SET, so a high on both SET and RESET resets the output to low.

Figure 2 shows the RS latch's timing waveform. Since the output is hardwired to low when both SET and RESET are high, the RS latch's limitation is its inability to distinguish SET and RESET edges and which edge comes first. Looking at figure 2 waveforms at the orange vertical line, when SET goes high, output is still low because RESET is high. This could create a problem when the latch's inputs are one-shot pulses with pulse widths that overlap each other.

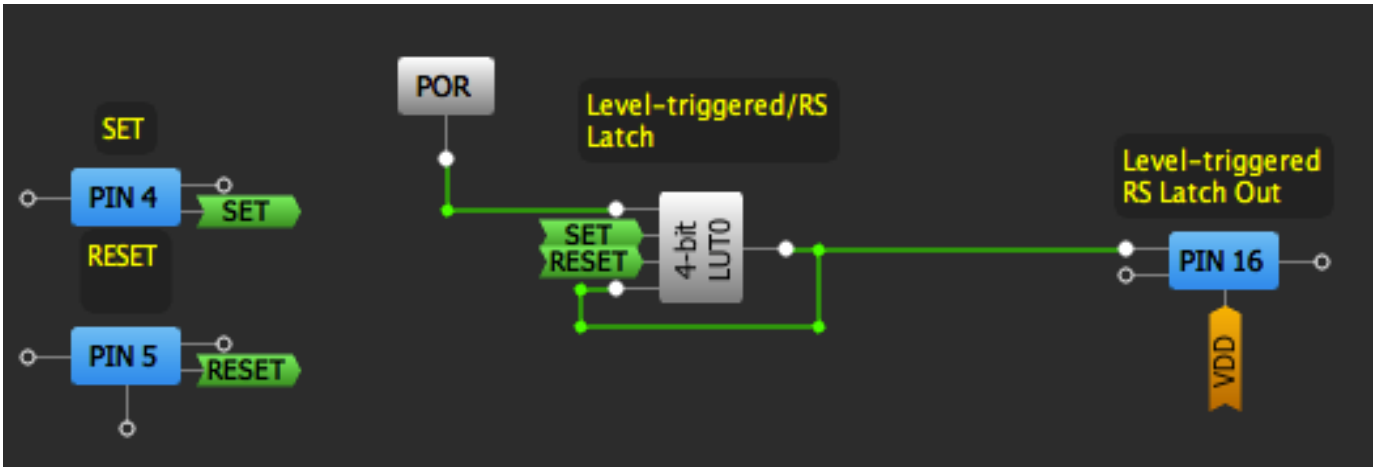

Figure 1. Level Triggered RS Latch

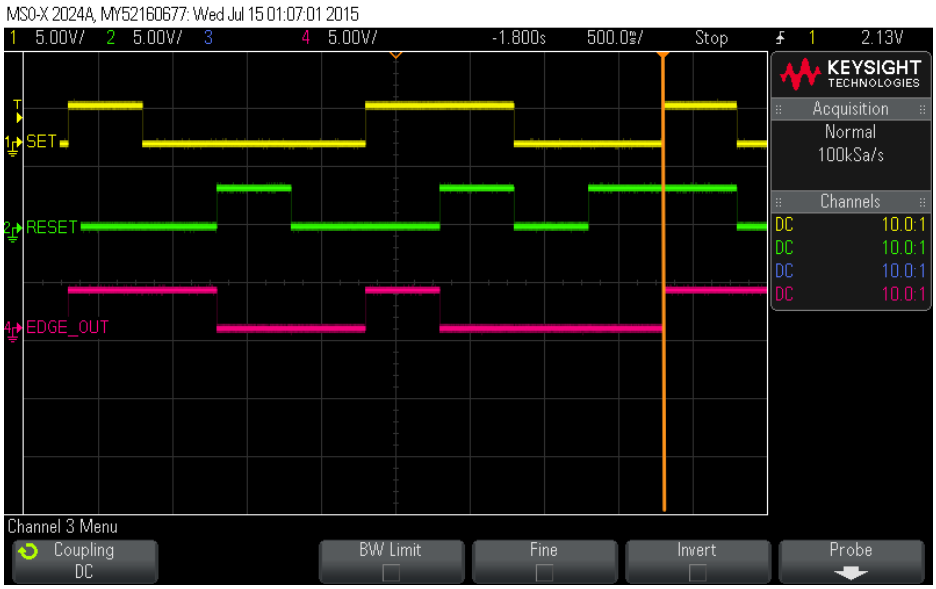

Figure 2. Level Triggered RS Latch Timing Diagram

Design 2: Edge Triggered Latch and its Versatility

Digital flip-flops (DFFs) are the perfect building blocks to make latches edge sensitive. This is because the output of a latch follows the input (R/S) when CLK is high (level sensitive), while the output of a DFF follows the input (D) when the CLK switches from low to high (edge triggered).

Figure 3 shows how to connect 2 DFFs together with an inverter to construct an edge-triggered latch. Tables 2 and 3 in the appendix show DFF2 and DFF3's properties respectively. Since both DFFs' inputs are GND (logic low), the rising edges of the SET and RESET inputs will clock the DFFs' outputs low. The outputs will be held low until the DFFs are being set by an active low signal on their nSET pins.

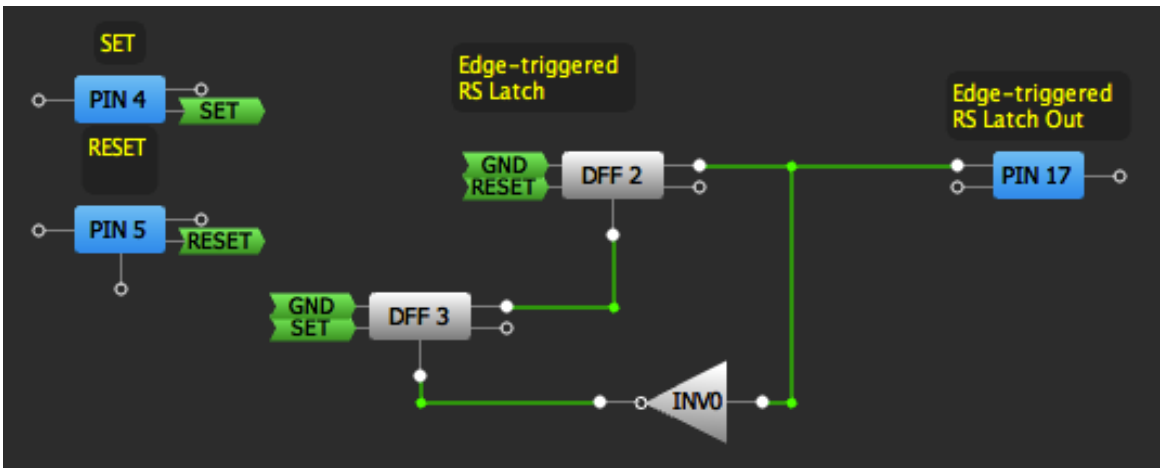

Figure 3. Edge Triggered RS latch

Essentially DFF3 will set the latch while DFF2 gets ready for the next RESET, and DFF2 will reset the latch while DFF3 gets ready for the next SET.

Some GreenPAK's DFF blocks have both a Q and a nQ output. If those resources are available, the inverter would not be needed.

Figure 4 shows the edge-triggered latch's timing waveform. It resolves conflict condition when both SET and RESET are high at the orange vertical line.

For edge and level trigger comparison, figure 5 lines up the two different latches' outputs together.

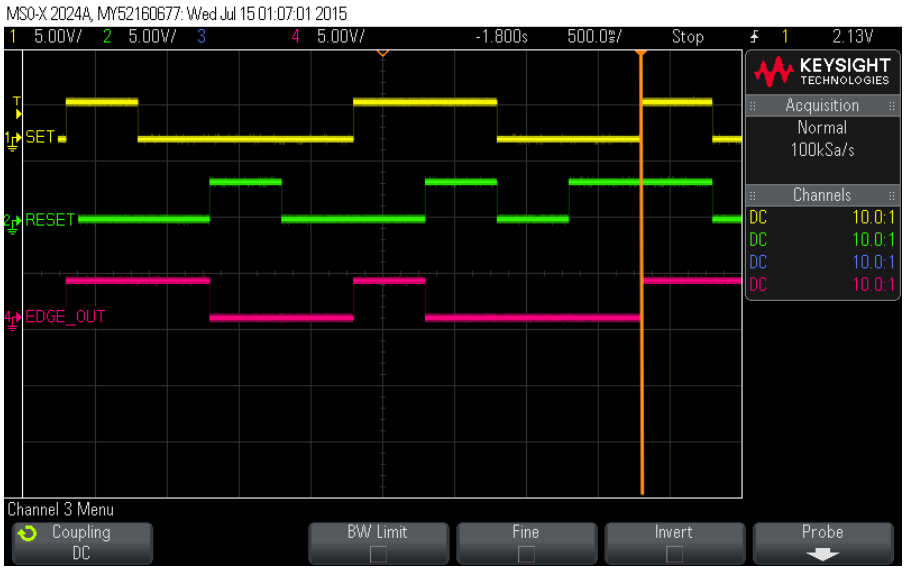

Figure 4. Edge Triggered RS Latch Timing Diagram

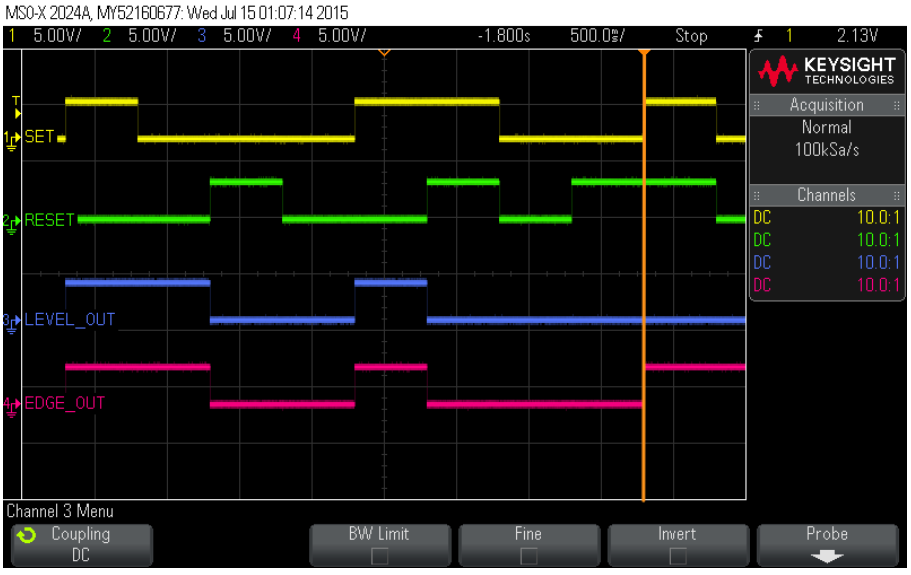

Figure 5. Edge and Level triggered RS latch timing diagram

Conclusion

With Renesas programmable mixed-signal ASICs technologies, a level-triggered latch can be very quickly converted into an edge-triggered latch and vice versa. Changing traditional discrete logic requires system-level board redesign; by using Renesas programmable mixed-signal ASICs, a change is now as simple as a few mouse clicks in the GreenPAK's Designer tool.

Appendix

The tables below show the properties of the resources used in this application note.

Table 1. LUT0

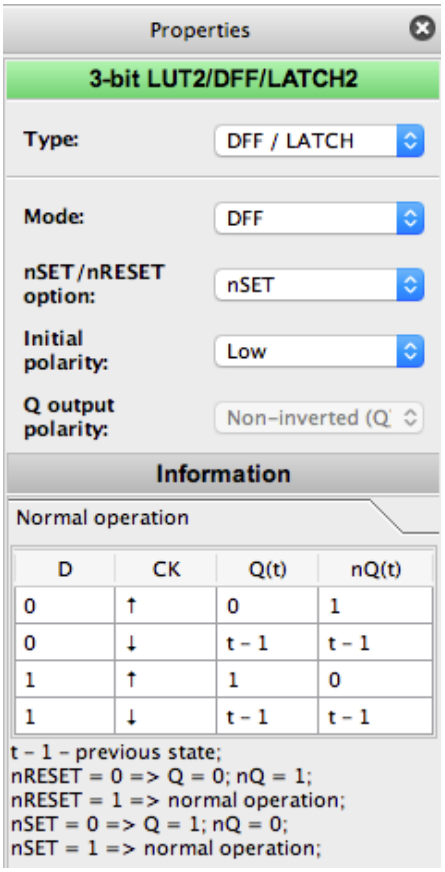

Table 2. DFF2

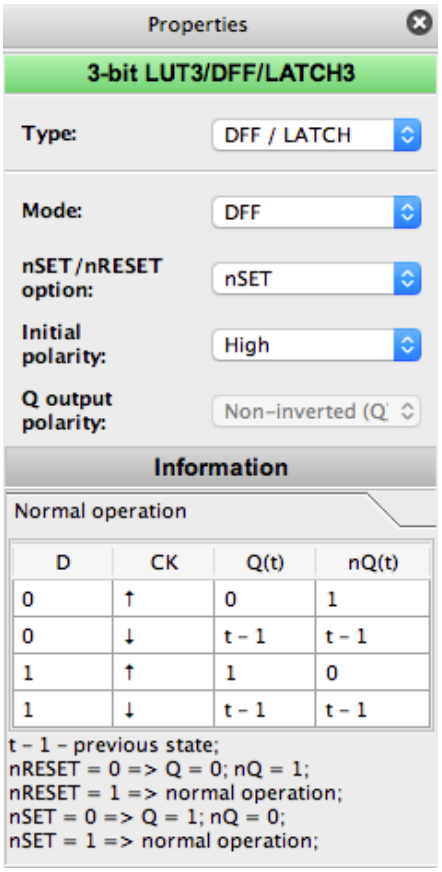

Table 3. DFF3

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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